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SEE IN SRAM

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OUTLINE

- Introduction
- The SRAM cells: 6T and 4T
- Single Event impact on CMOS inverter and SRAM cell: flipping the bit
- SRAM SEU:
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  - cross section
  - critical charge
- Scaling issues in SRAM SEU
- Conclusions

Introduction

Why SEE's on SRAM's?

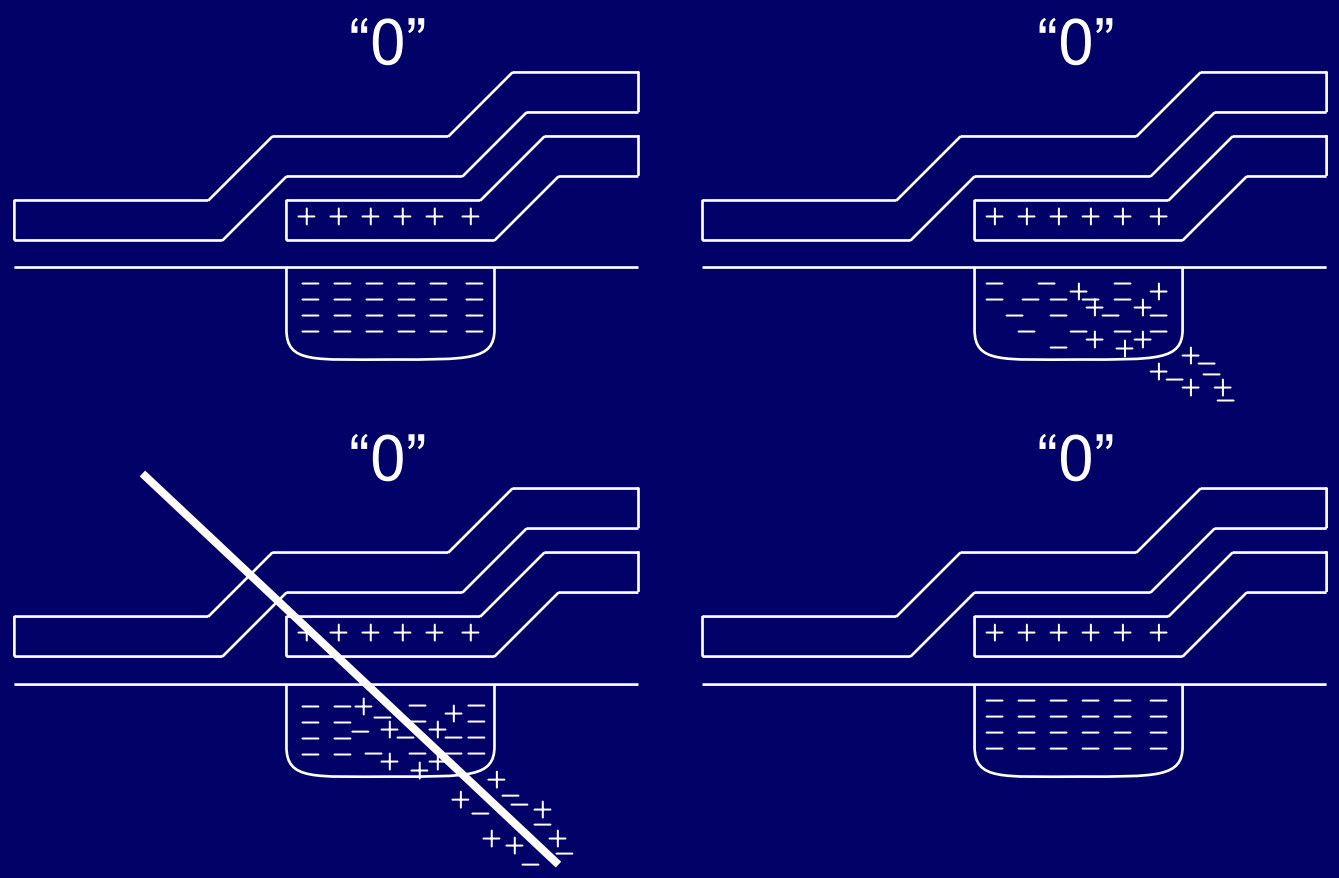
- The Static Random Access Memory (SRAM) is a benchmark to evaluate the SEE sensitivity of CMOS technologies
- SRAM is the easiest latch to be fabricated in standard CMOS technology (DRAM or FLASH need dedicated process steps)
- SRAM's are widely used in all logic circuits
- SRAM cell size scales with Moore's law
- SRAM cells can be simulated in detail
- Memories are easier to test than logic (such as DSP)
- SEE measurements are straightforward even on commercial parts

Early reports of SEE's in memories

- SEE's in memories typically refer to the loss of information from a memory cell caused by a single ionizing particle: Single Event Upset (SEU)
- In a Flip-Flop (Latch) the information corruption is associated to the bit flip: 0 → 1 or 1 → 0
- Memory arrays are organized in words and more than one SEU may affect a single word:
  - Single Bit Upset (SBU)
  - Multiple Bit Upset (MBU)
- Soft Error Rate (SER)
- First report on memories: a bipolar flip-flop circuit (Binder et al., 1975) affected by cosmic rays in satellites

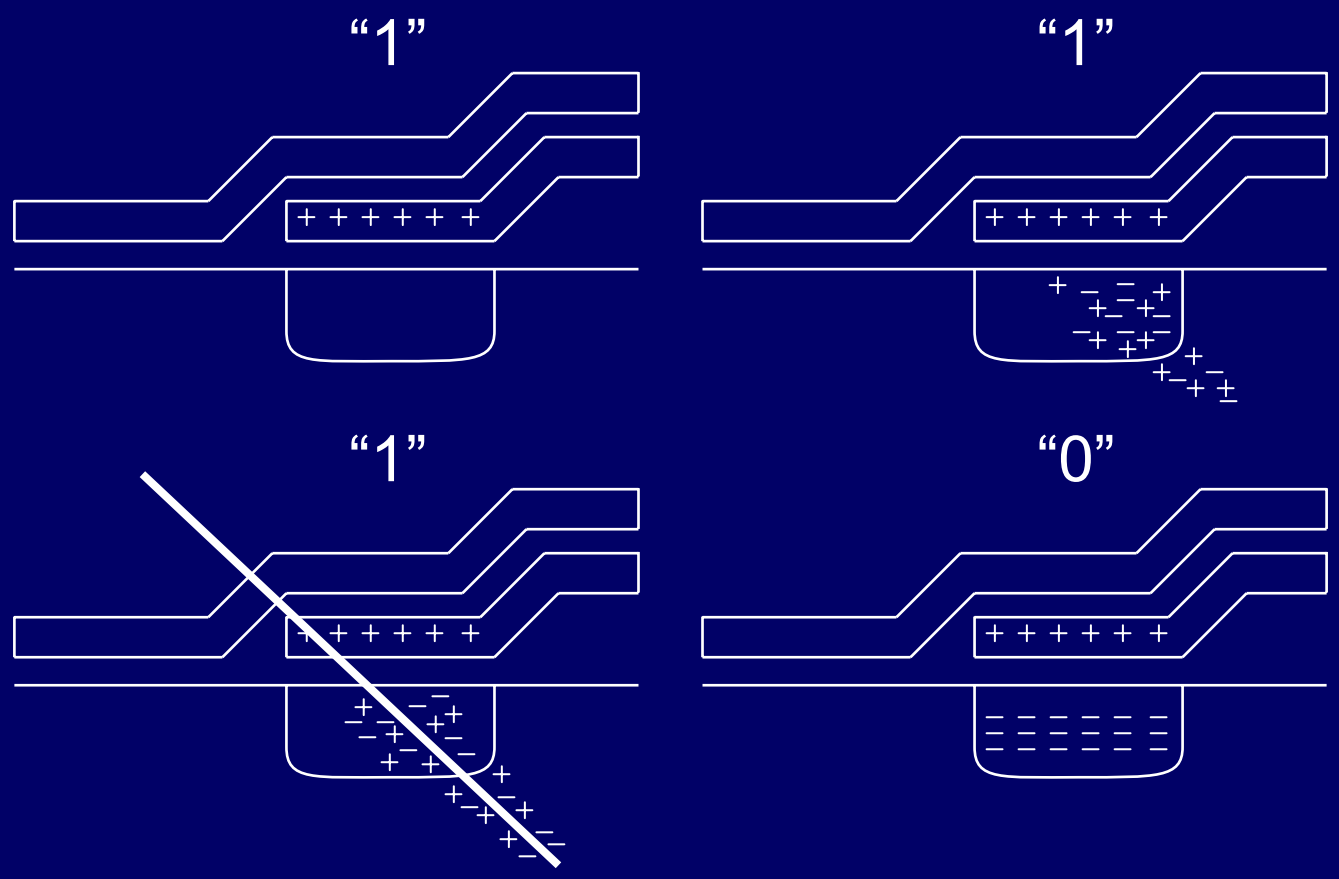
SEU in early DRAMs: no effect on “0”

The DRAM case: SEU’s observed at sea level in Intel 16K DRAM’s (1979) generated by alpha particles produced by radioactive contaminants



T.C. May and M.H. Woods, IEEE-TED26, 1979

SEU in early DRAMs: “1” flips

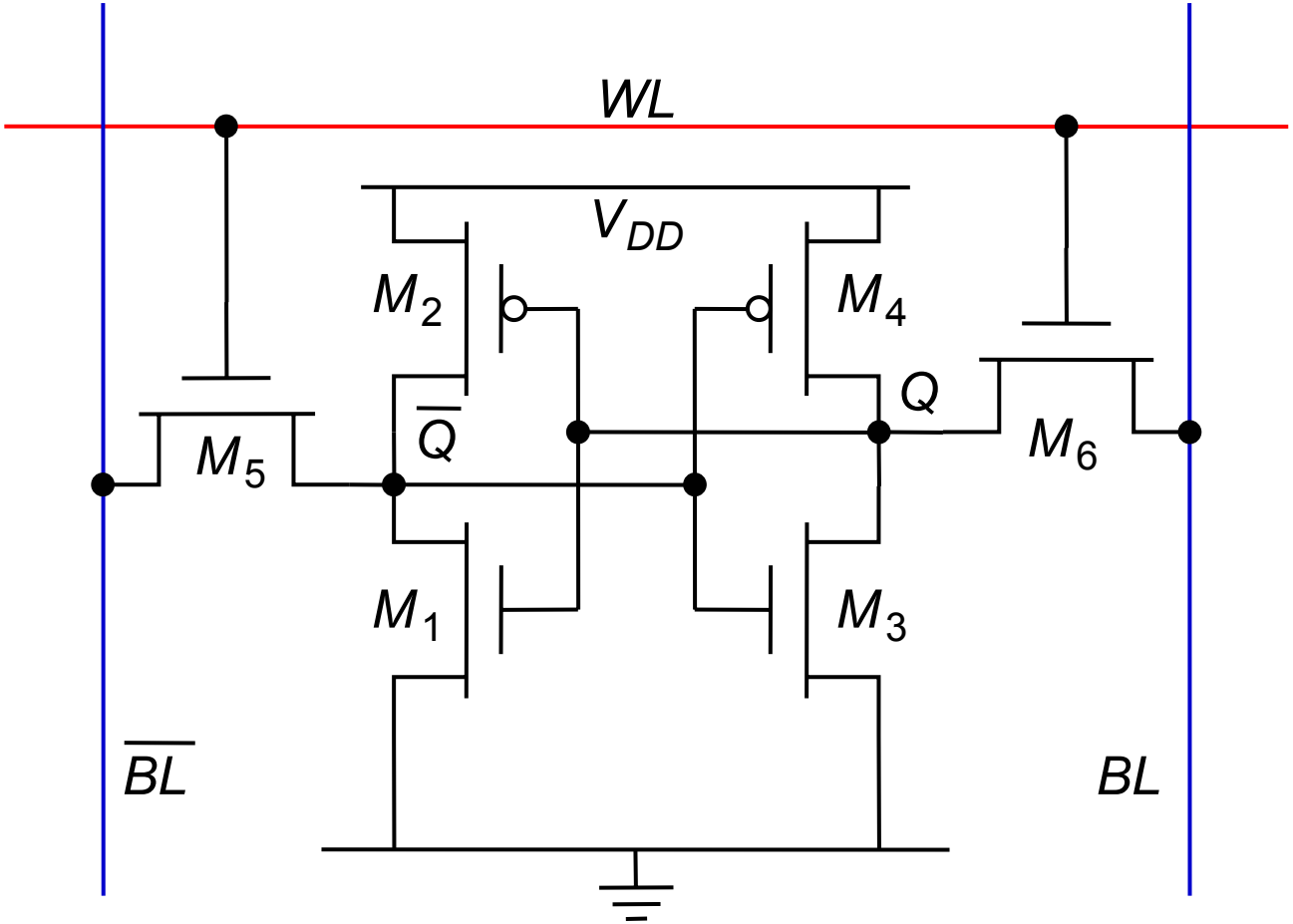


T.C. May and M.H. Woods, IEEE-TED26, 1979

Critical Charge in DRAM's

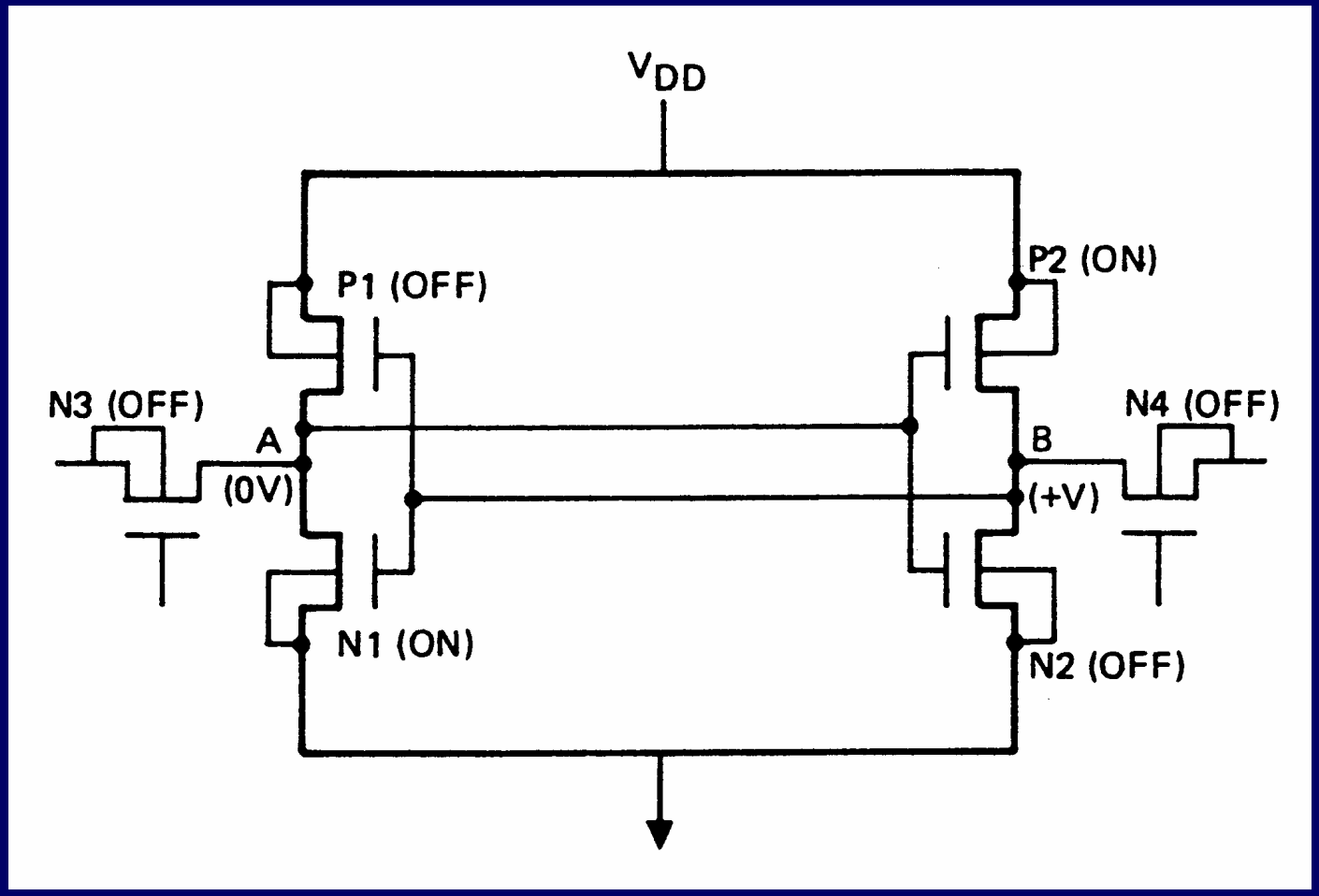
- Bit Flip may occur when a charge larger than a threshold value (Critical Charge) is collected at one sensitive node of the memory cell
- In DRAM's the Critical Charge is usually defined as $Q_{crit} = V_c \cdot C_s$, where C_s is storage capacitance
- Critical voltage, V_c, is typically half the power supply voltage
- In SRAM cells things may be substantially different…

6-Transistor (6T) CMOS SRAM cell



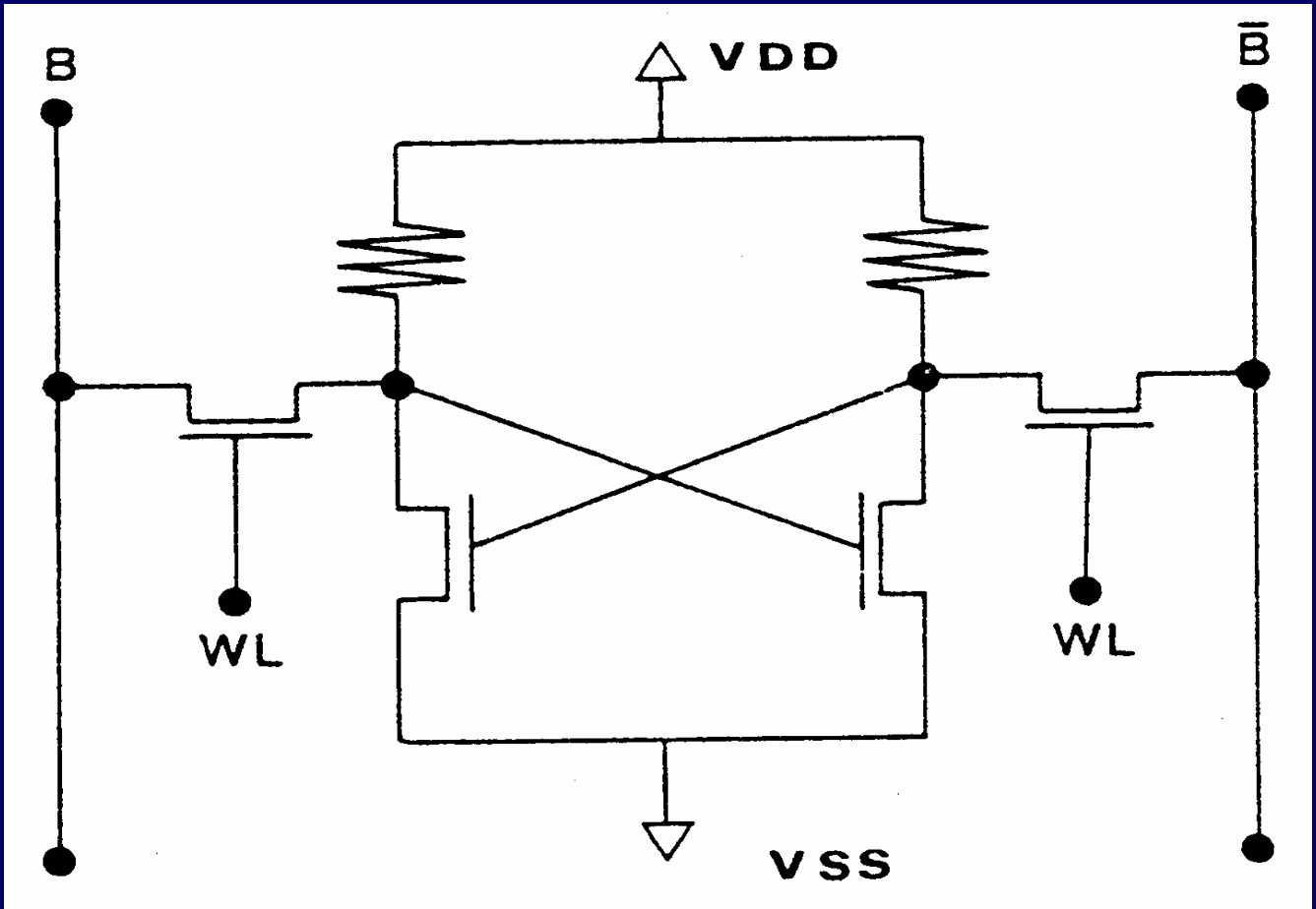
J.Rabey, Digital Integrated Circuits, Prentice Hall, 1996

6T SRAM cell: MOSFET status (hold condition)



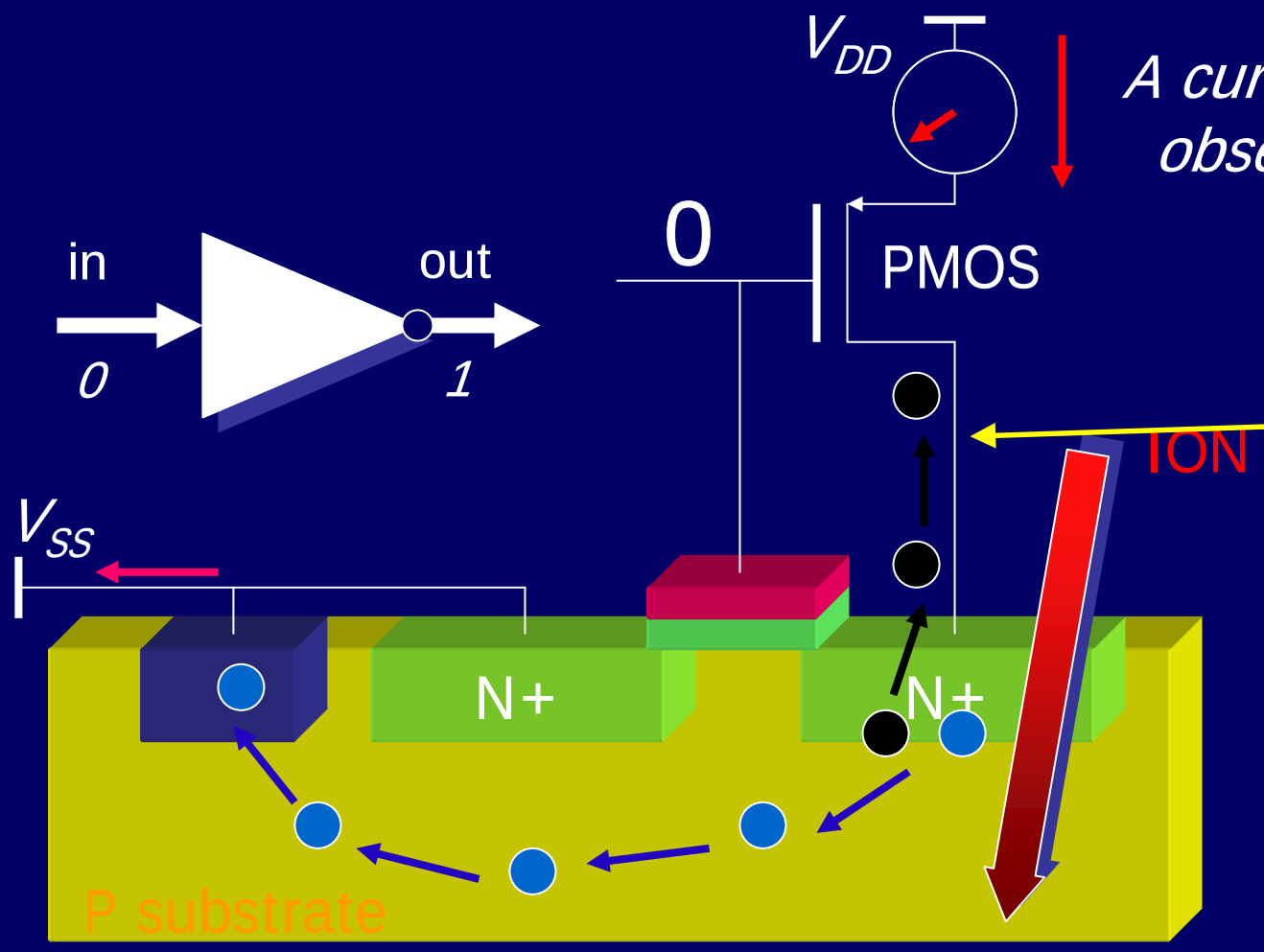
J.C. Pickel and J.T. Blandford, IEEE-TNS29, 1982

4T SRAM cell: a more compact design



S.E. Diehl-Nagle, IEEE-TNS31, 1984

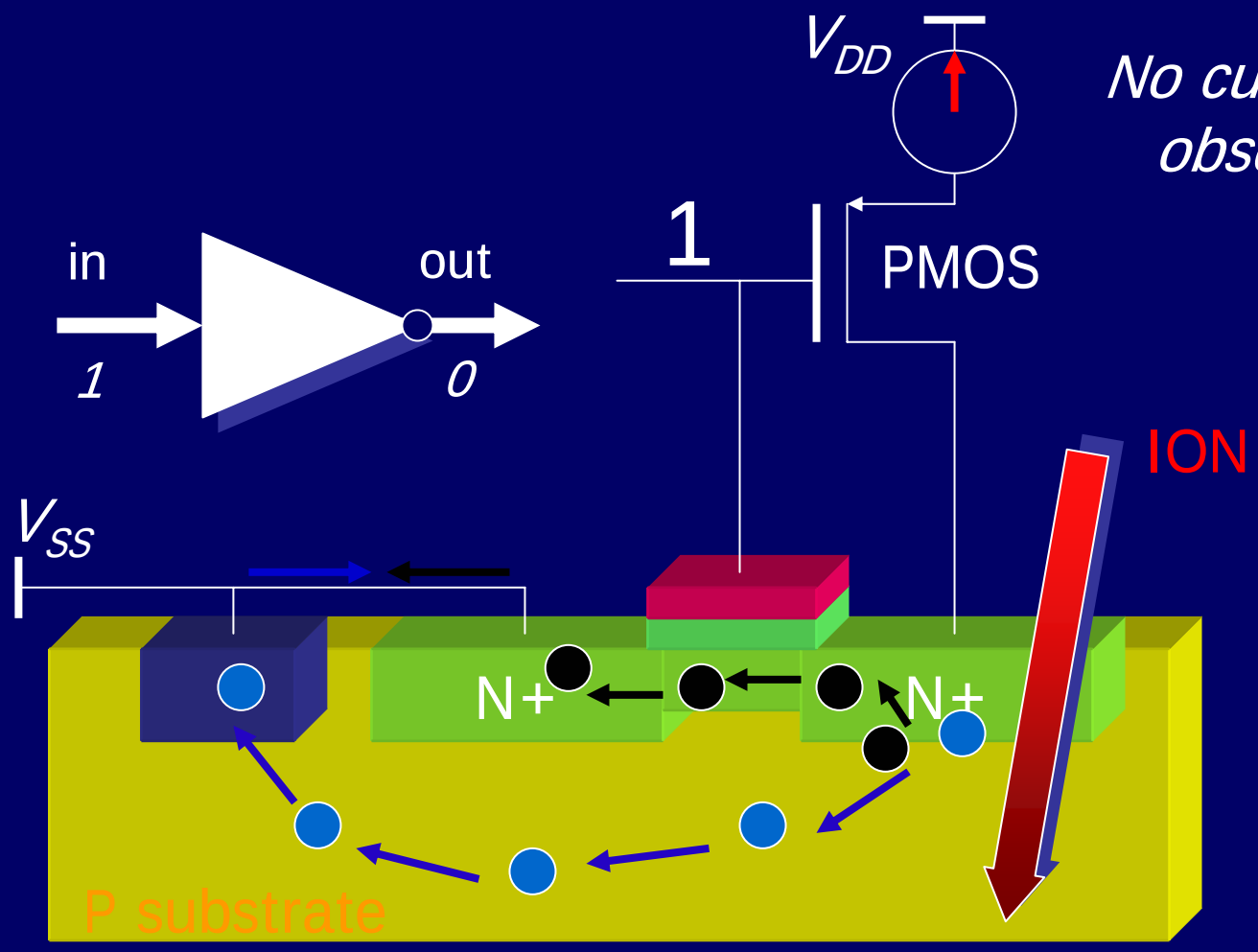
SE in CMOS inverter: OUT = 1



- The output node **out** is discharged
- A current is injected by the PMOSFET into the **out** node to **restore** the initial charge and logic value

P. Fouillat, EWRHE 2004

SE in CMOS inverter: OUT = 0

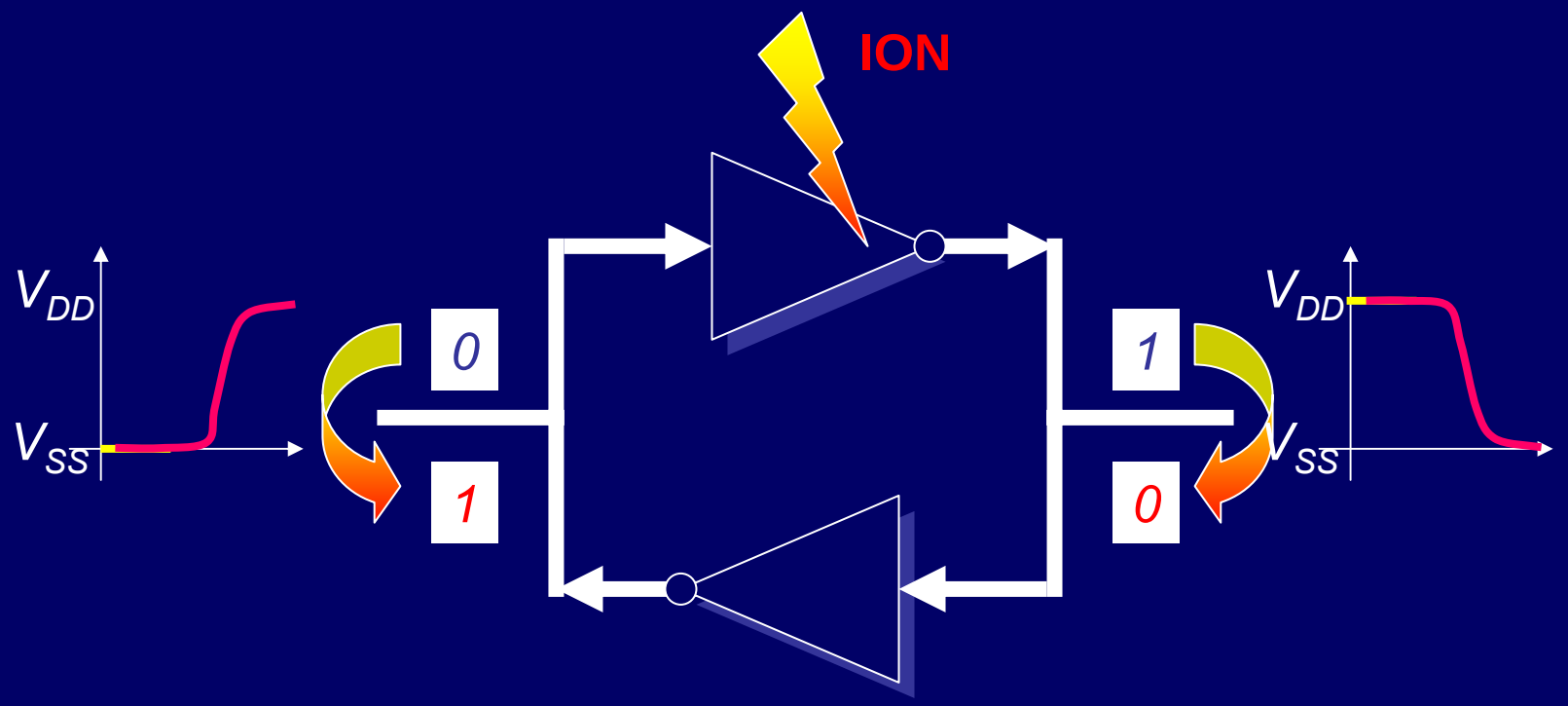


No current is observed

Only reversed biased junctions of off-state MOSFET drains may effectively collect charge and affect the **out** node voltage

P. Fouillat, EWRHE 2004

SEU in SRAM cell



Upsetting a memory cell

P. Fouillat, EWRHE 2004

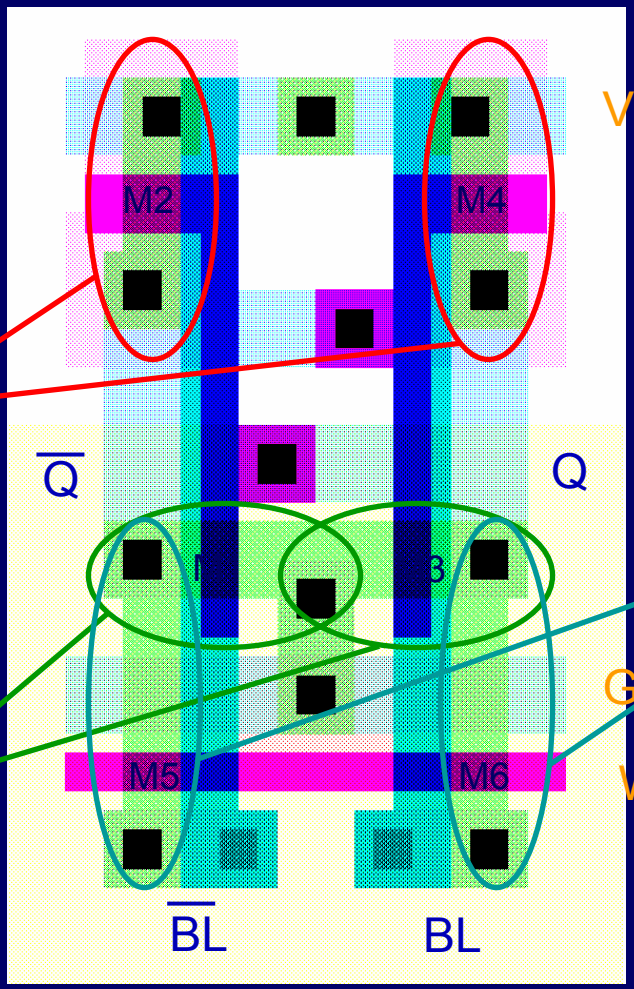
6T-SRAM — Layout

CMOS INVERTER:

PMOSFET's

NMOSFET's

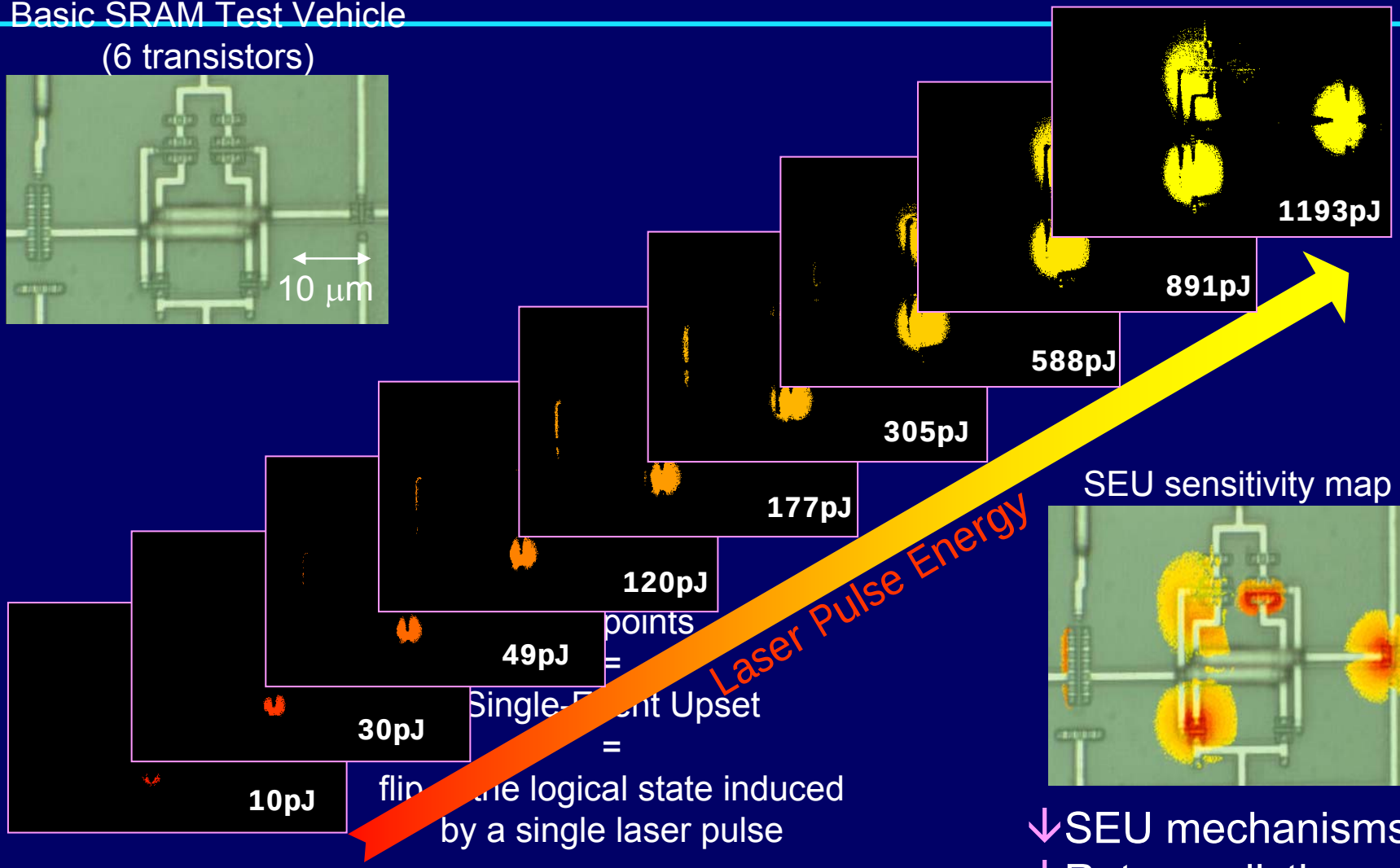
Pass-Transistors to Bit Lines



J.Rabey, Digital Integrated Circuits, Prentice Hall, 1996

SEU mapping in an SRAM cell

Basic SRAM Test Vehicle
(6 transistors)



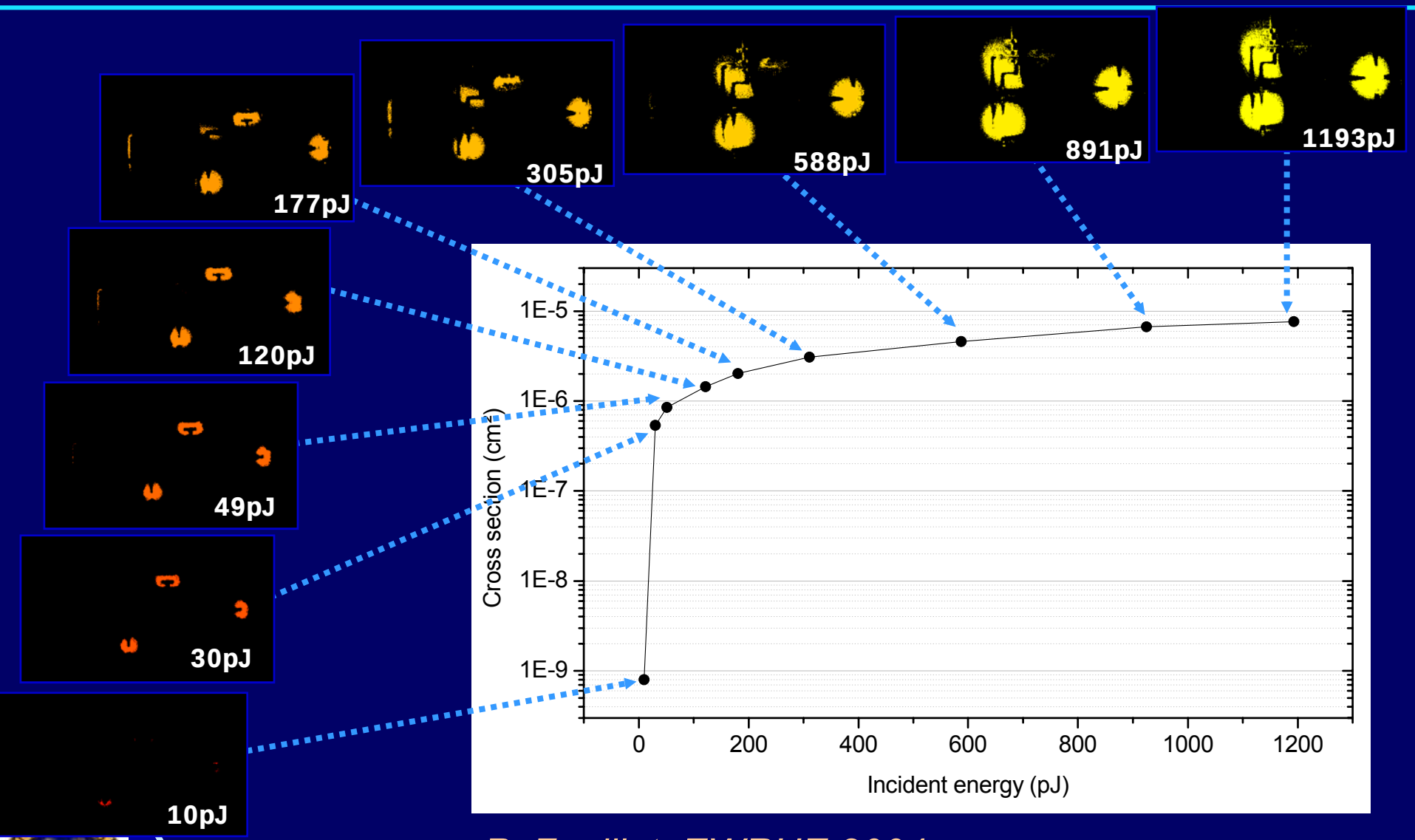
points
=
Single-Event Upset
=
flip the logical state induced
by a single laser pulse

SEU sensitivity map

↓SEU mechanisms
↓Rate prediction
↓Design optimisation

P. Fouillat, EWRHE 2004

SEU Laser cross section in SRAM



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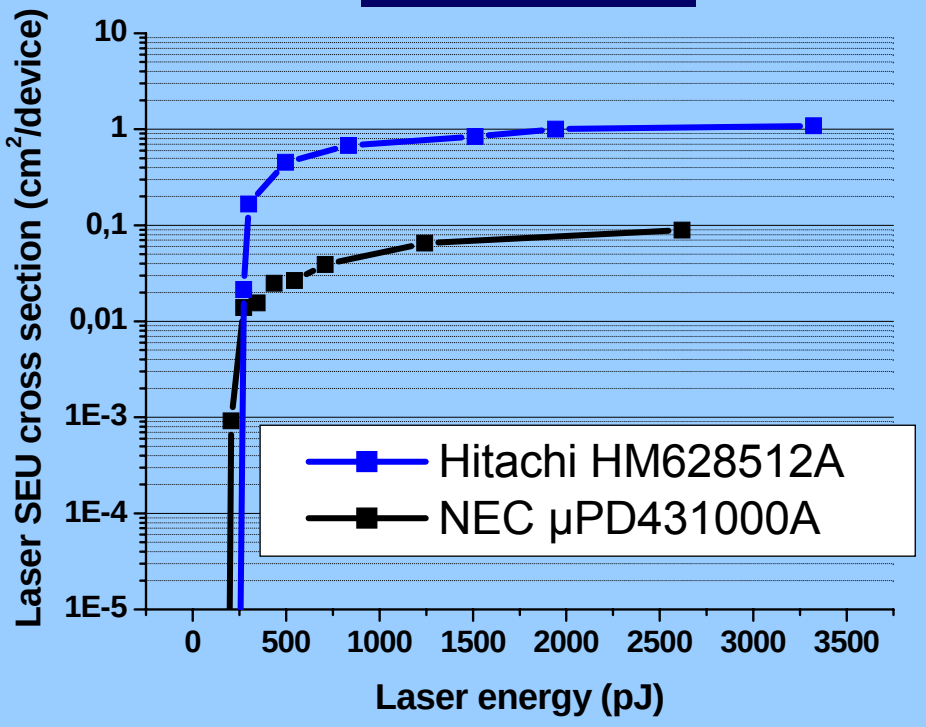
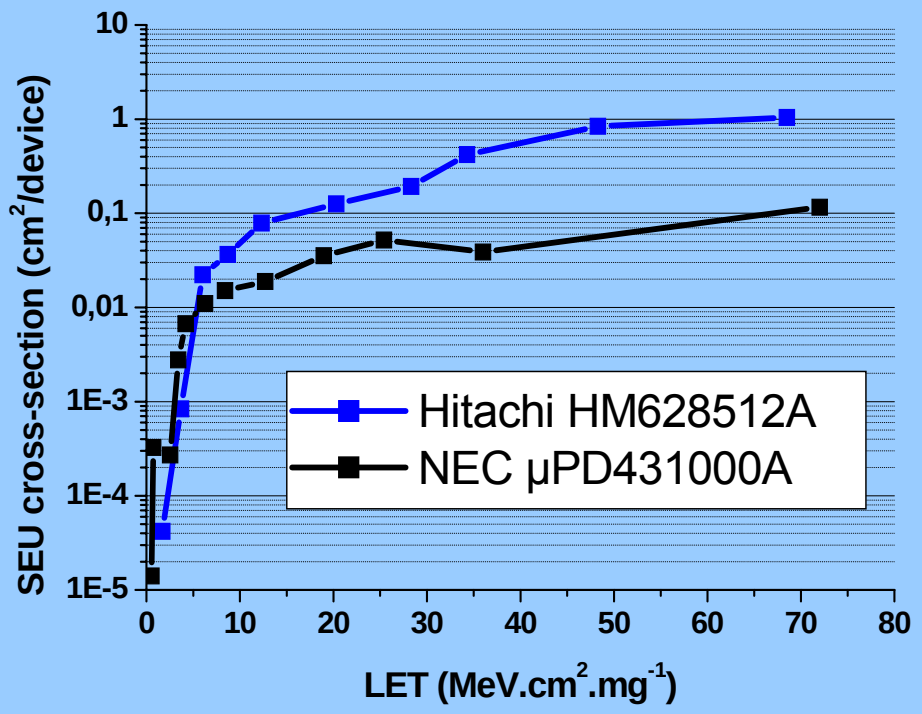
Testing SRAMs: heavy ions vs. laser

HITACHI A 4Mbits 0.5µm versus NEC 1Mbits 0.8µm

Laser Tests



Heavy ion Tests



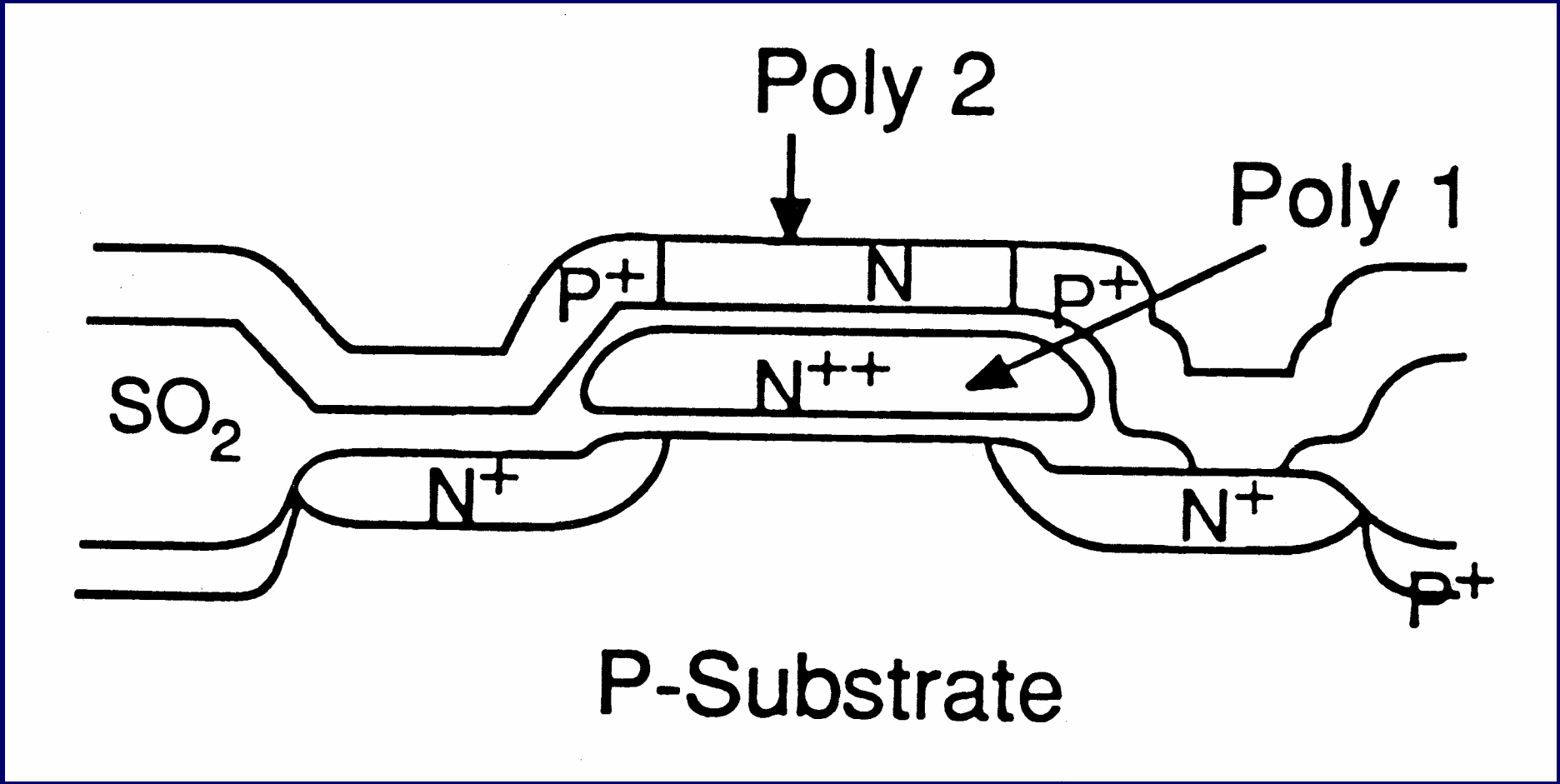
P. Fouillat, EWRHE 2004

Increasing SEU resistance of SRAM cells

Different technological steps may be realized to improve the SEU Resistance/tolerance of SRAM cells:

- Enhance storage capacitance (STMicroelectronics)
- Use 6T cell design with TFT load devices

Thin Film Transistor for 6T SRAM cell



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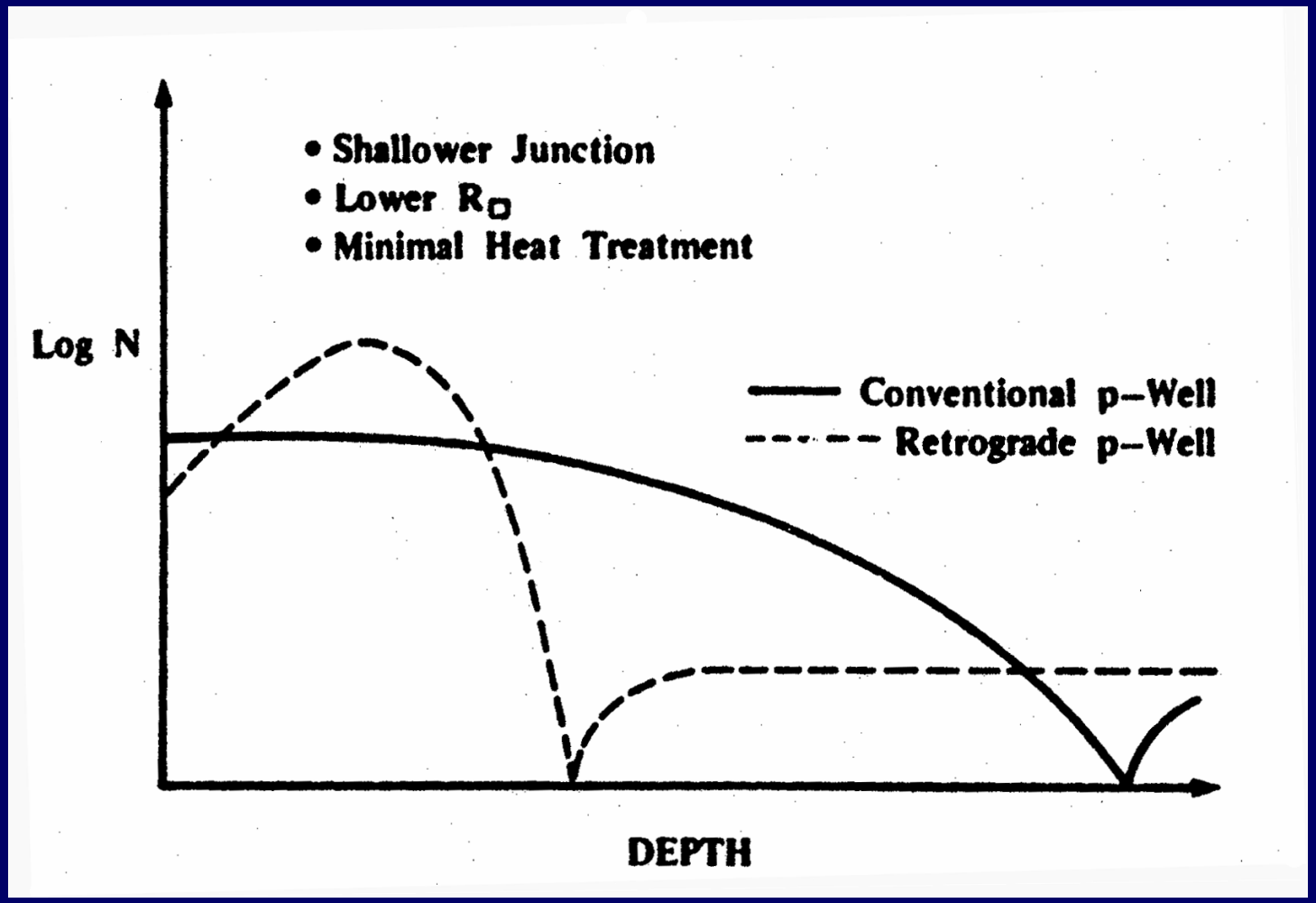
- Use retrograde wells, i.e., highly doped implanted layers in order to reduce charge collection at the drain nodes

Retrograde well doping profile



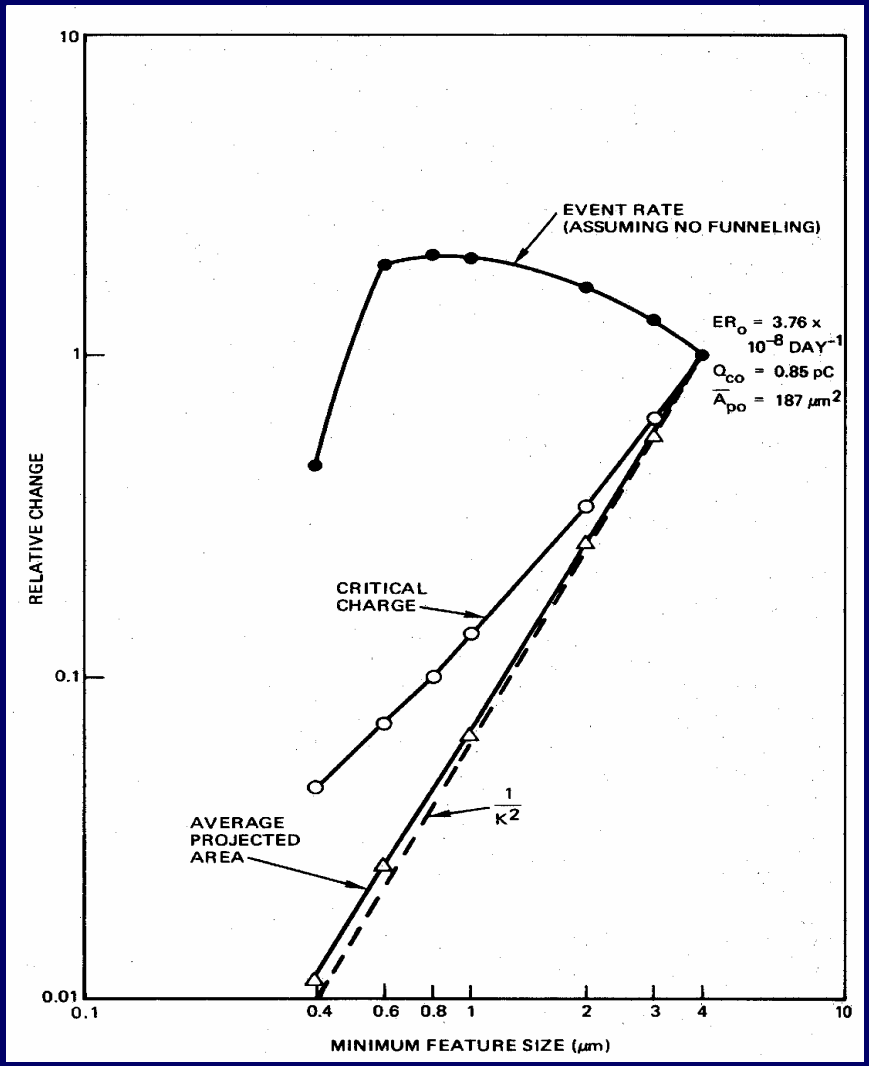
R.D. Rung et al., IEEE-TED28, 1981

Increasing SEU resistance of SRAM cells

Different technological steps may be realized to improve the SEU Resistance/tolerance of SRAM cells:

- Enhance storage capacitance (STMicroelectronics)
- Use 6T cell design with TFT load devices
- Use retrograde wells, i.e., highly doped implanted layers in order to reduce charge collection at the drain nodes
- Eliminate ^{10}B from the external passivation layers and internal p-doped B rich regions: nuclear reactions from thermal neutrons are suppressed
- Use plastic packaging instead of ceramic, reducing the amount of radioactive alpha emitters around the Si chip

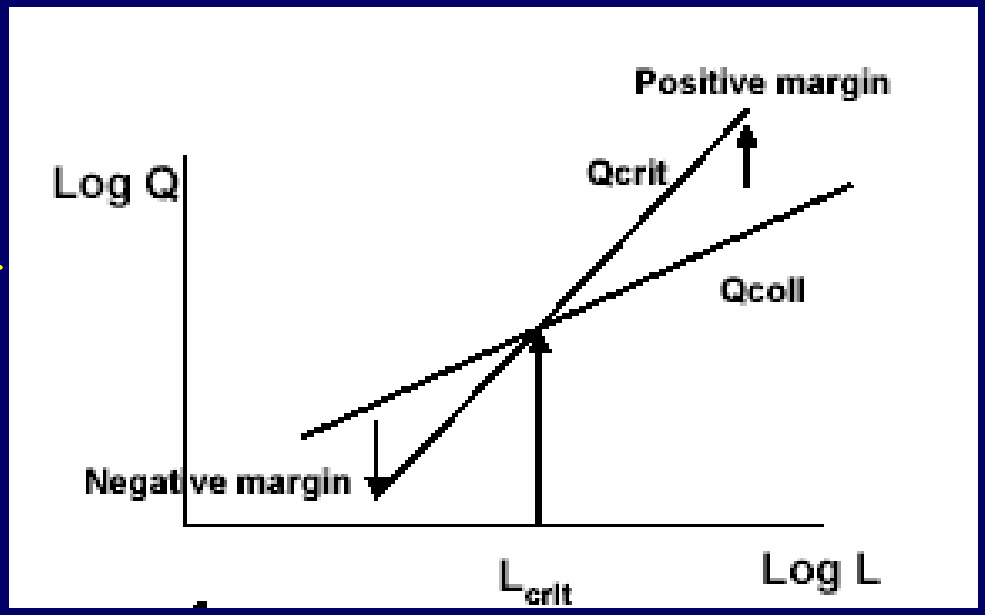
Forecasting the CMOS scaling effect on SEU



J.C. Pickel and J.T. Blandford, IEEE TNS29, 1982

Critical charge in SRAM: status of the art

- Usually, critical charge:
  - $Q_{crit} = V_c \cdot C_s$
  - $V_c \sim V_{DD}$ [/2]
  - $C_s \sim W \cdot L \cdot \varepsilon_{ox} / t_{ox}$
  - $Q_c \sim L^2$
- Collected charge:
  - $Q_{coll} \sim L$
- However in SRAM:
  - $Q_{crit} = V_c \cdot C_s + I_{restore} \cdot T_{flip}$
- Further, parasitic capacitance from Local Interconnections (LIC) may strongly increase C_s thus improving SEU immunity (*Samsung, IEDM2002*)



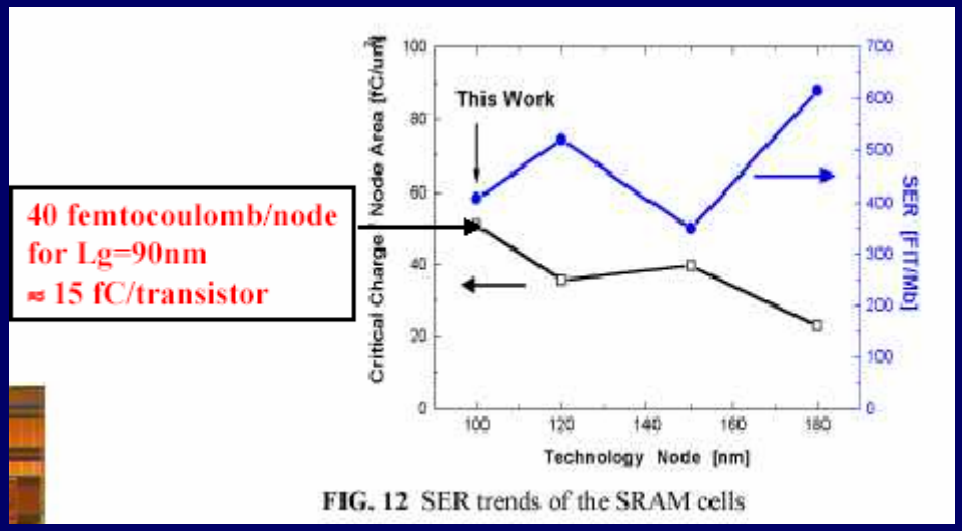
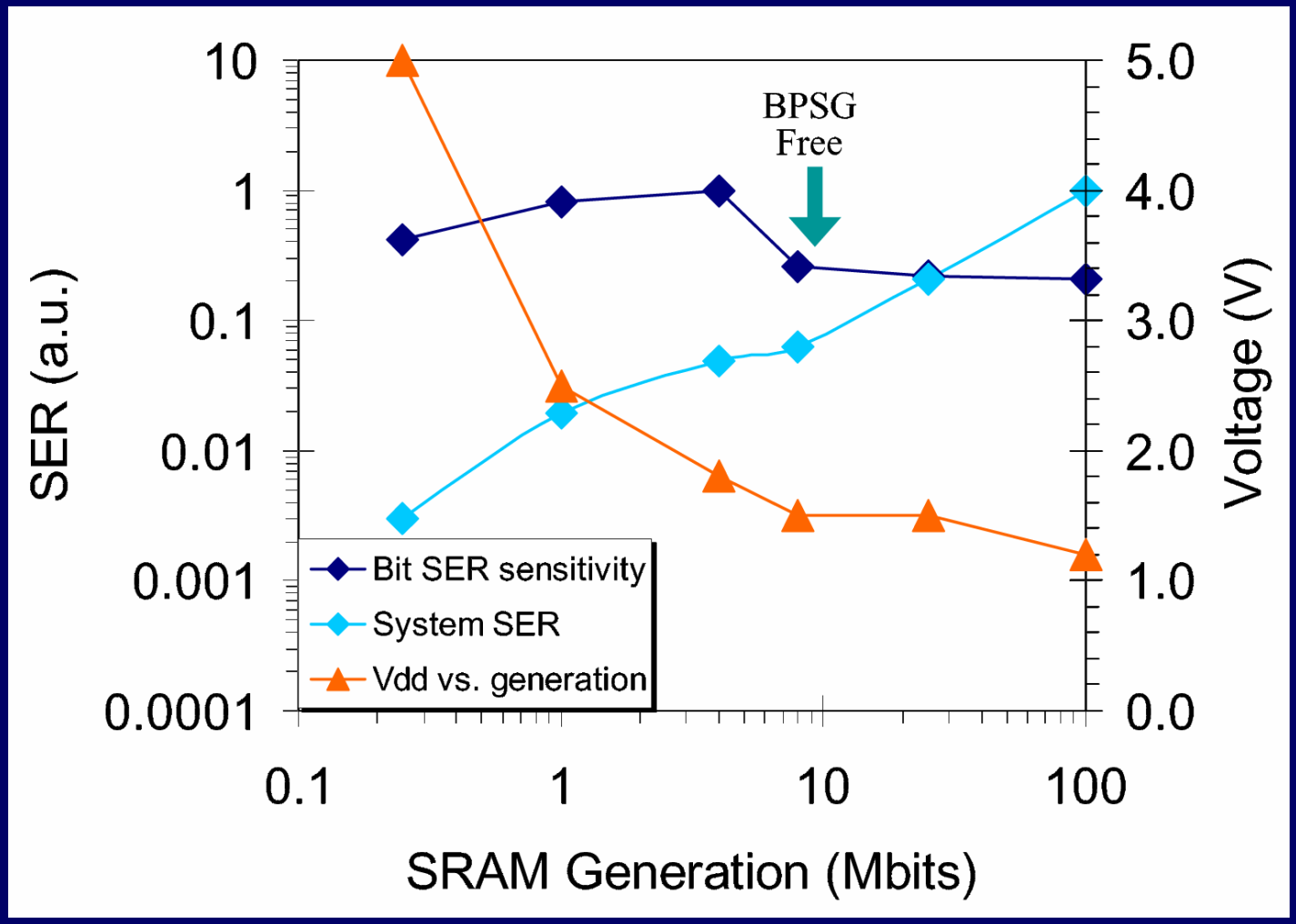


FIG. 12 SER trends of the SRAM cells

J.L. Leray, EWRHE 2004

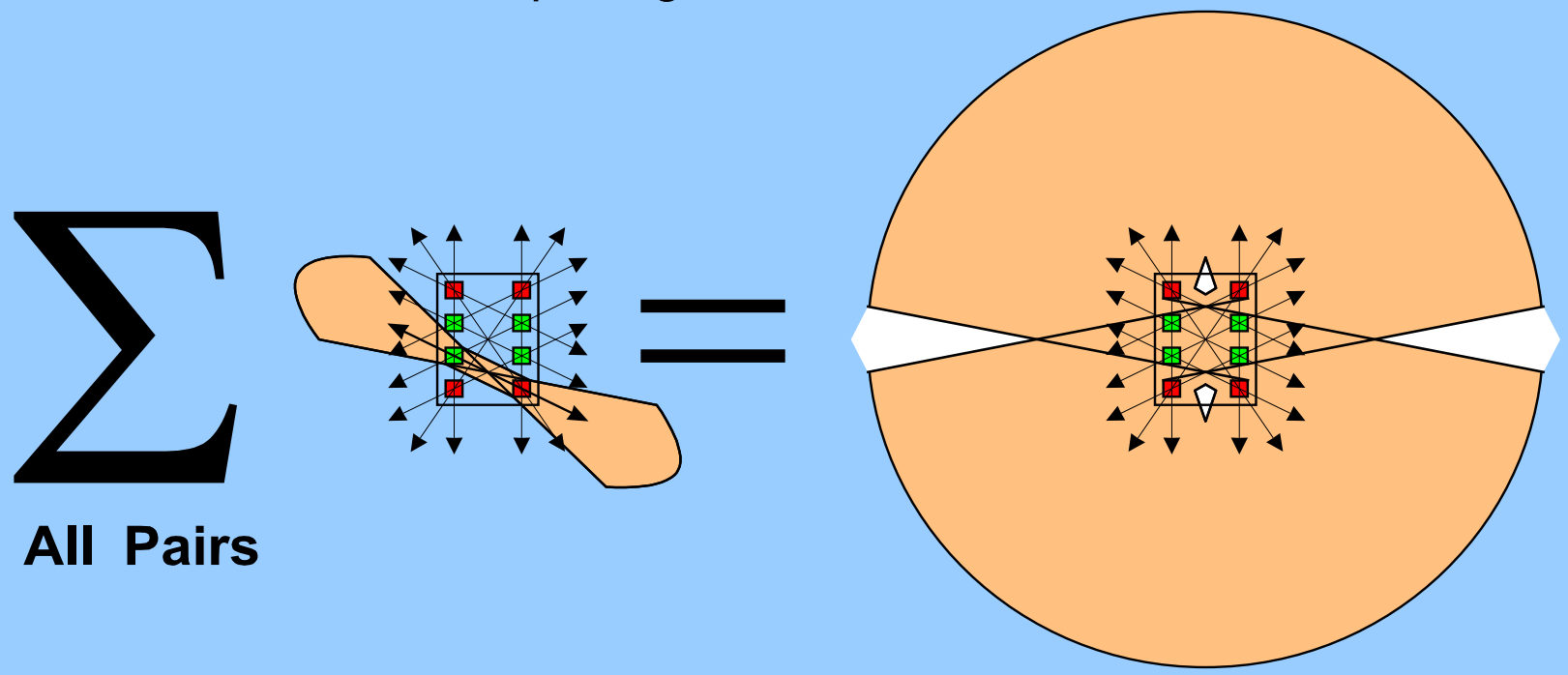
SRAM scaling trends



R. Baumann, RADECS Short Course, 2001

Multiple bit upset

- A single ion may flip two bits or more inside the same memory word: MBU
- Identify safe locations for other bit cells
  - Optimize layout aspect ratio and critical node locations
  - Determine minimum spacing of bits in word line



D.G. Mavis, EWRHE 2004

Estimation of SRAM SER in space ambients

- Estimates for a 0.25 μm SRAM technology, 8 bit word + 4 EDAC bits
  - Area ~ 100 μm^2
  - Single bit error rate ~ 7.5×10^{-9} /day (GEO)
- Error latency
  - Word single bit error rate ~ 9.0×10^{-8} /day (GEO)
  - Word double bit error rate ~ 8.1×10^{-15} /day
  - No special scrubbing necessary
- Proton worst case environments (~1000x error rate)
  - Word double bit error rate ~ 8.1×10^{-9} /day
  - Periodic scrubbing could be advantageous

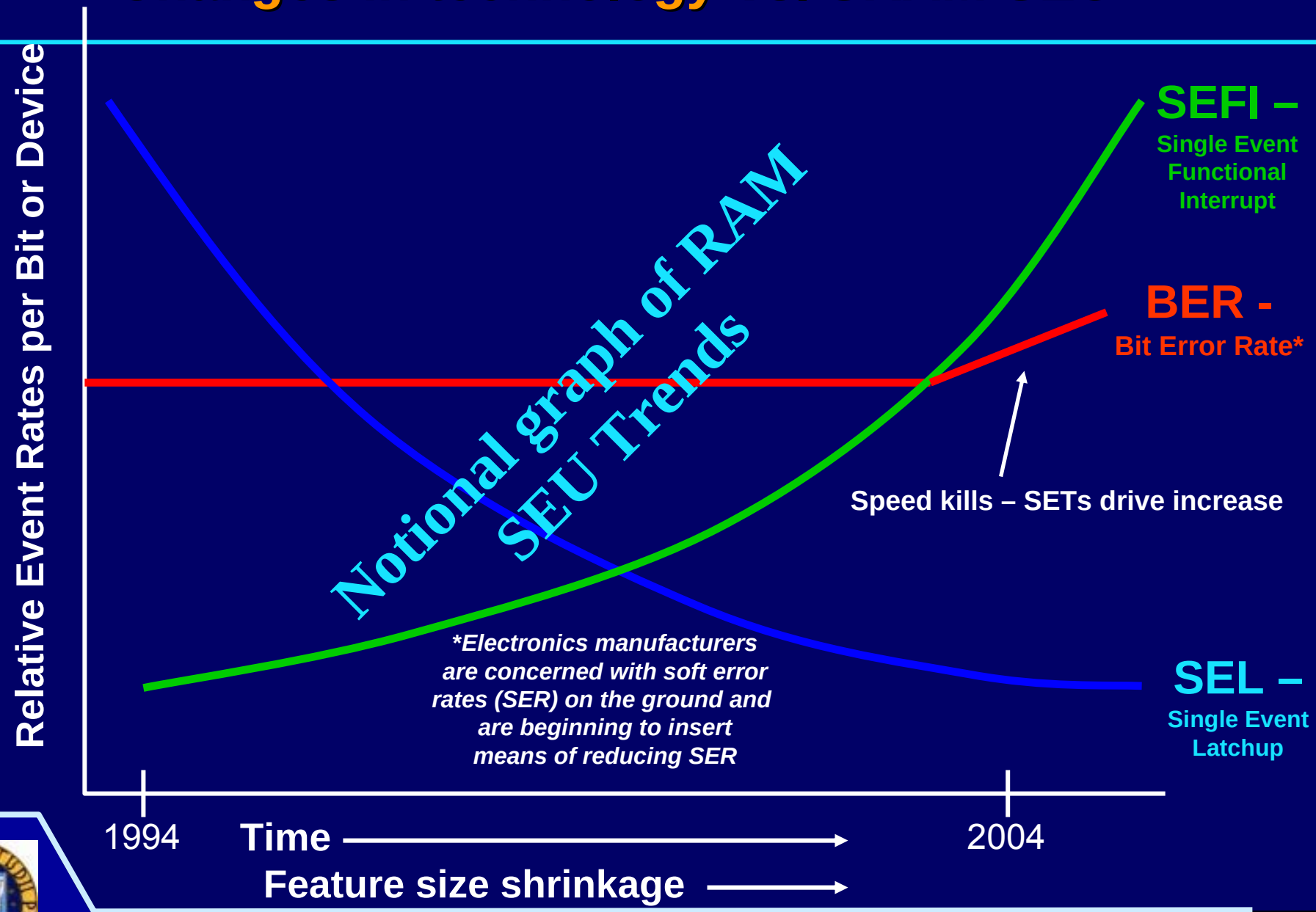
D.G. Mavis, EWRHE 2004

SRAM design alternatives

- Conventional 6T cells with EDAC
  - Small size, high performance
  - Low LET upset threshold
  - High error rate in some space environments (such as in the proton rich belts)
- RC hardened 6T cells with EDAC
  - Large size, slower performance
  - High LET upset threshold
  - Difficult to implement in deep submicron technologies
- Hardened 6T cells with additional capacitors (STM)
  - No performance penalty claimed
  - Requires dedicated process steps

From D.G. Mavis, EWRHE 2004

Changes in technology vs. SRAM SEU



Conclusions

- Reversed biased junctions of off-state MOSFET drains collect charge produced by a single ionizing particle, possibly leading to SRAM cell bit flip
- SEU cross section saturates at high LET
- Critical charge for upset decreases with CMOS minimum feature size, but it may be enhanced by parasitic capacitances coming from interconnections
- SBU's can be compensated by EDAC; MBU's are much less likely but more dangerous
- SEU rate of cell array is not increasing with memory generation, but new problems may come from upsets in the circuit external to the memory array and SE Transients