Metodologie di disegno di ASIC resistenti alle radiazioni

Federico Faccio

CERN

Outline

- ✓ Foreword: CMOS technologies
- ✓ TID: Total Ionizing Dose
  - Effects (reminder)
  - Solutions
  - Trends in state-of-the-art technologies
- ✓ SEEs: Single Event Effects
  - Effects (reminder)
  - SEEs and scaling
  - Solutions
- ✓ Conclusion

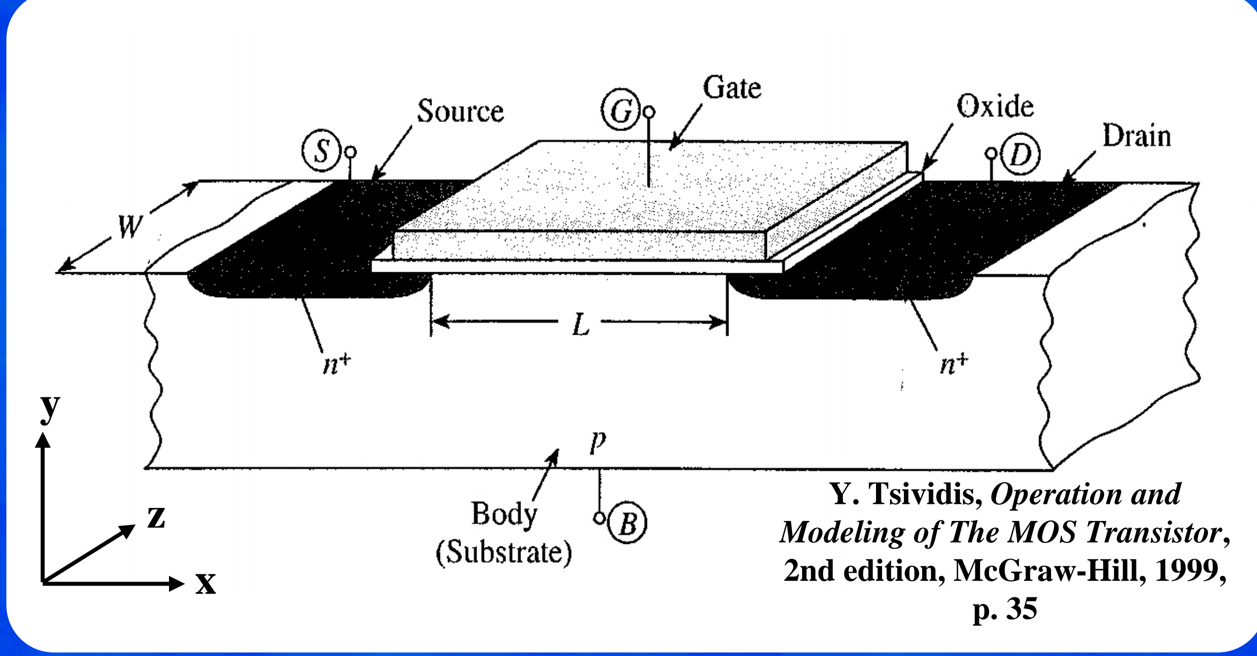
Foreword

✓ What we will be talking about:

- ASICs (application-specific ICs)
- CMOS technologies only
- Effects: TID, SEU, SEL

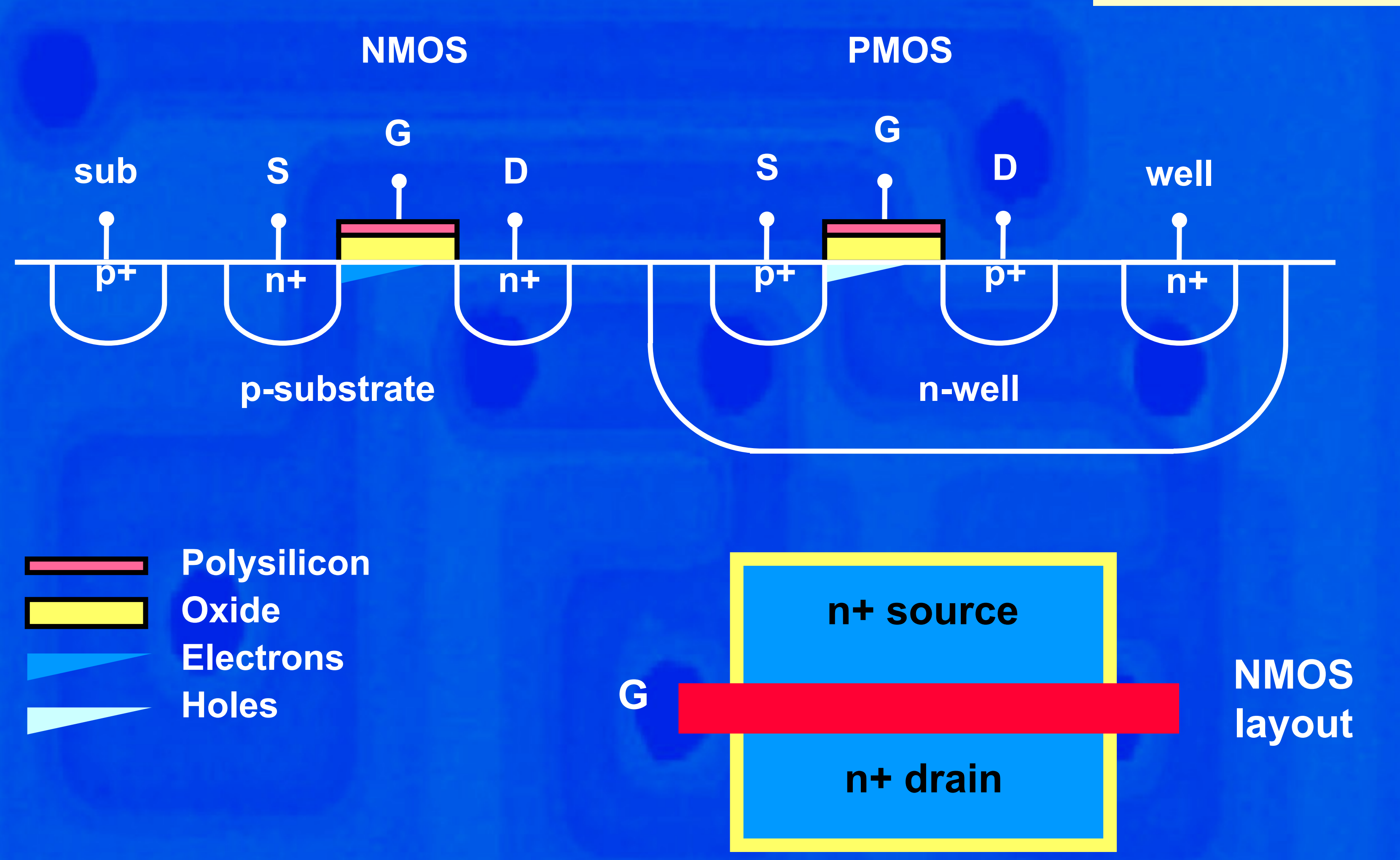
- How to conceive ASICs able of surviving to and functioning in a radiation environment

Foreword: the MOS transistor



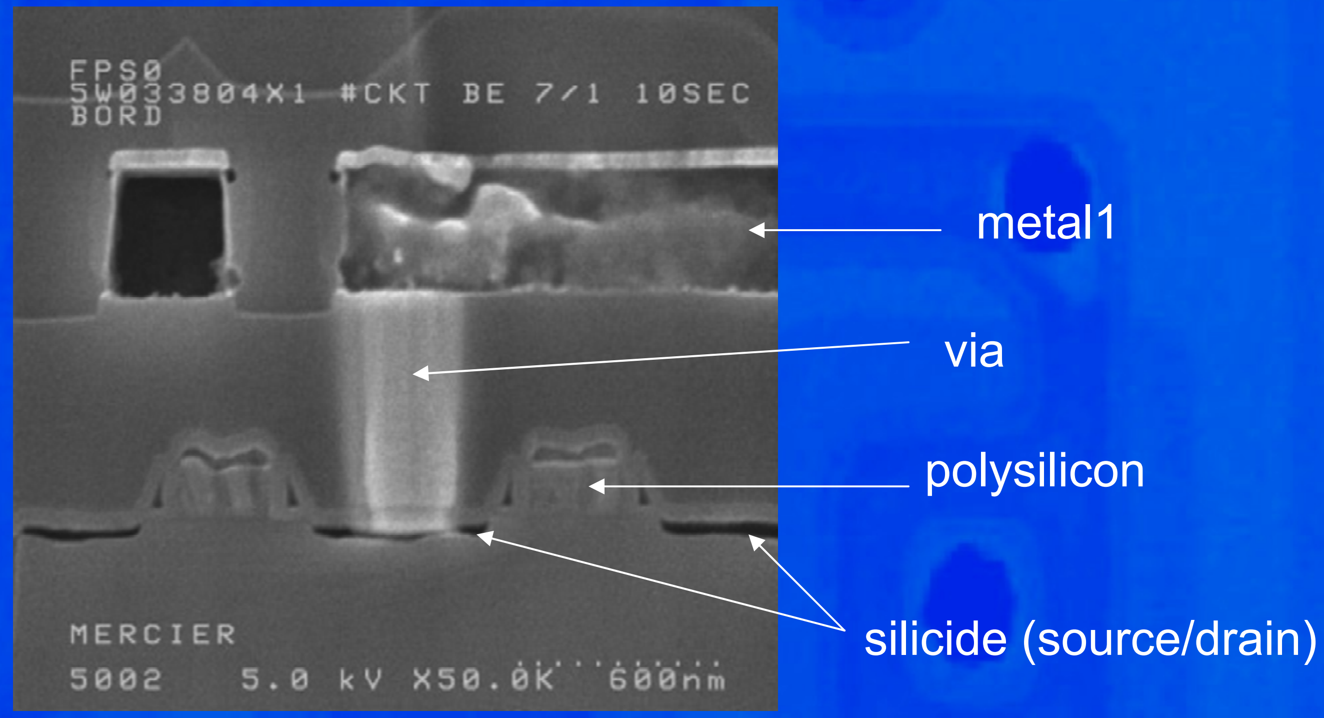
Y. Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd edition, McGraw-Hill, 1999, p. 35

Foreword: CMOS technology

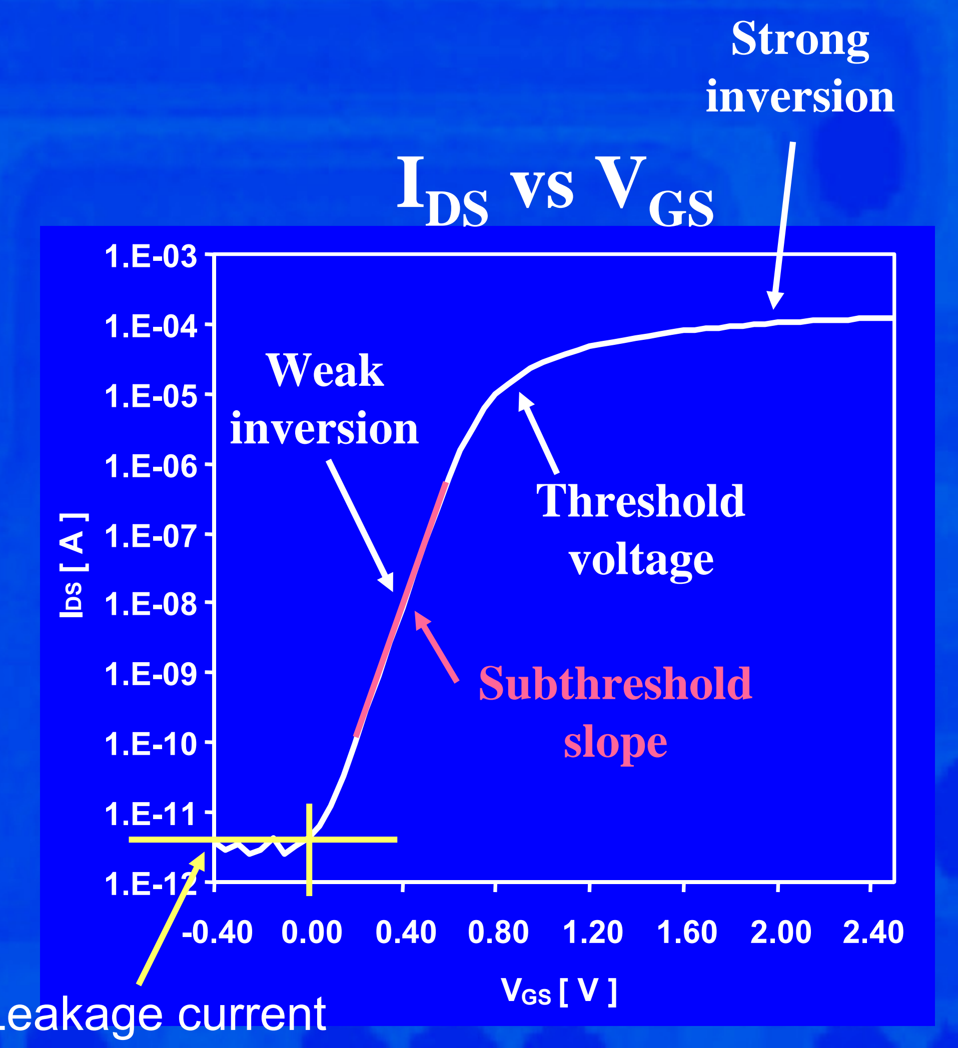


Foreword: CMOS technology

- ✓ SEM of transistors



Foreword: I - V Characteristics



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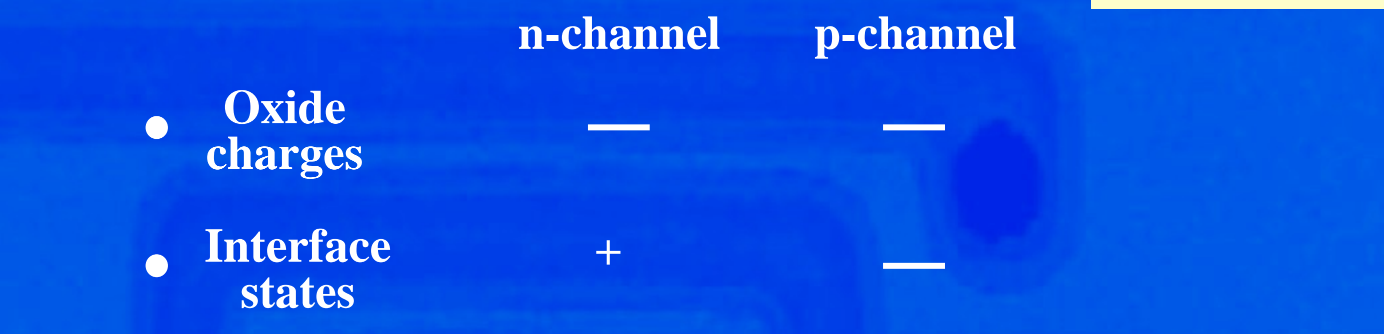
TID effect on "main" transistor



	n-channel	p-channel
• Oxide charges	—	—
• Interface states	+	—

N-channel

I_D

I_2

I_1

0 V_{T2} V_{T1} V_{GS}

Before irradiation

P-channel

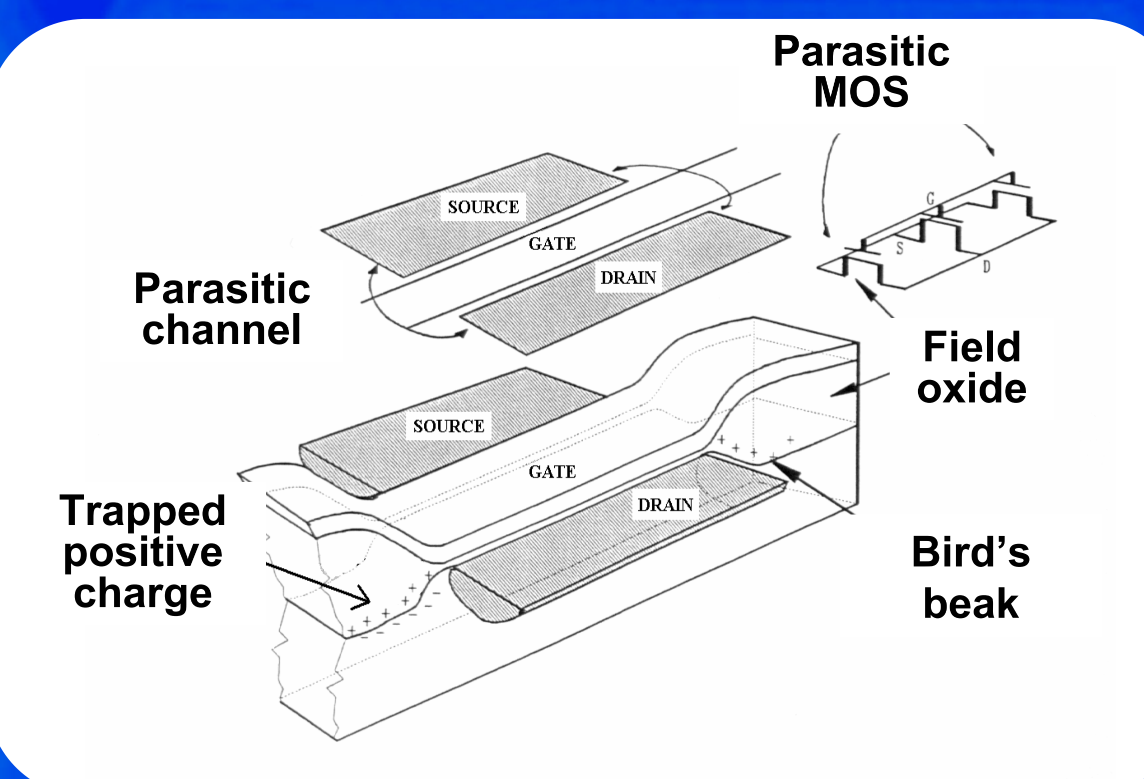
I_D

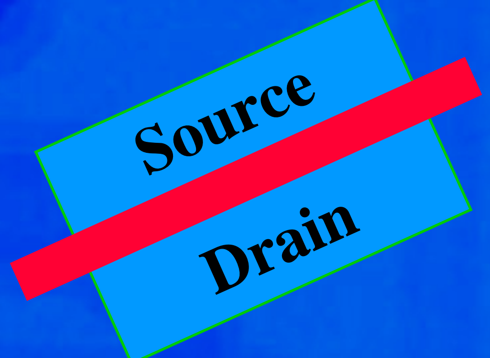
Before irradiation

I_1

0 V_{T1} V_{T2} $-V_{GS}$

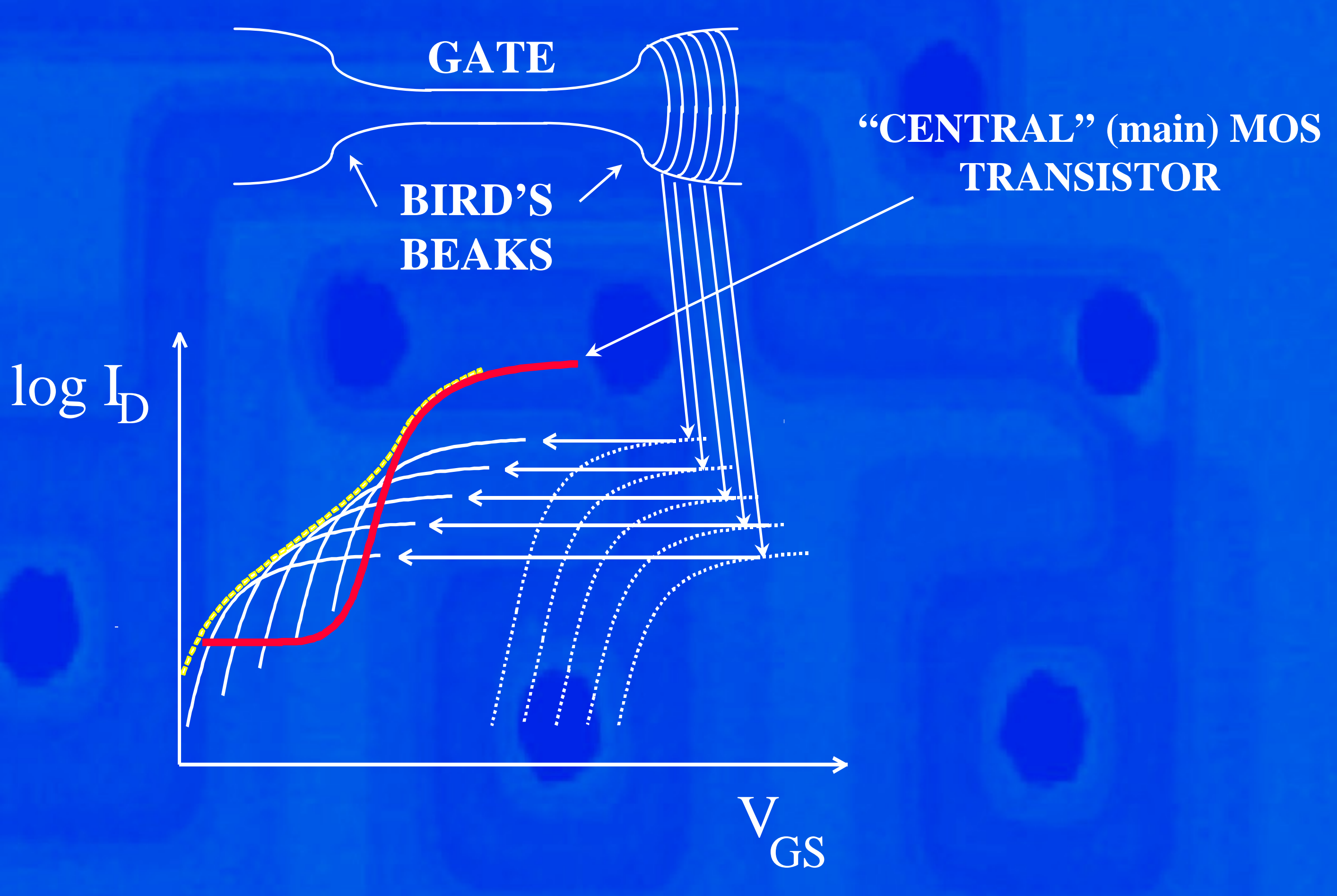
Transistor level leakage





Transistor level leakage

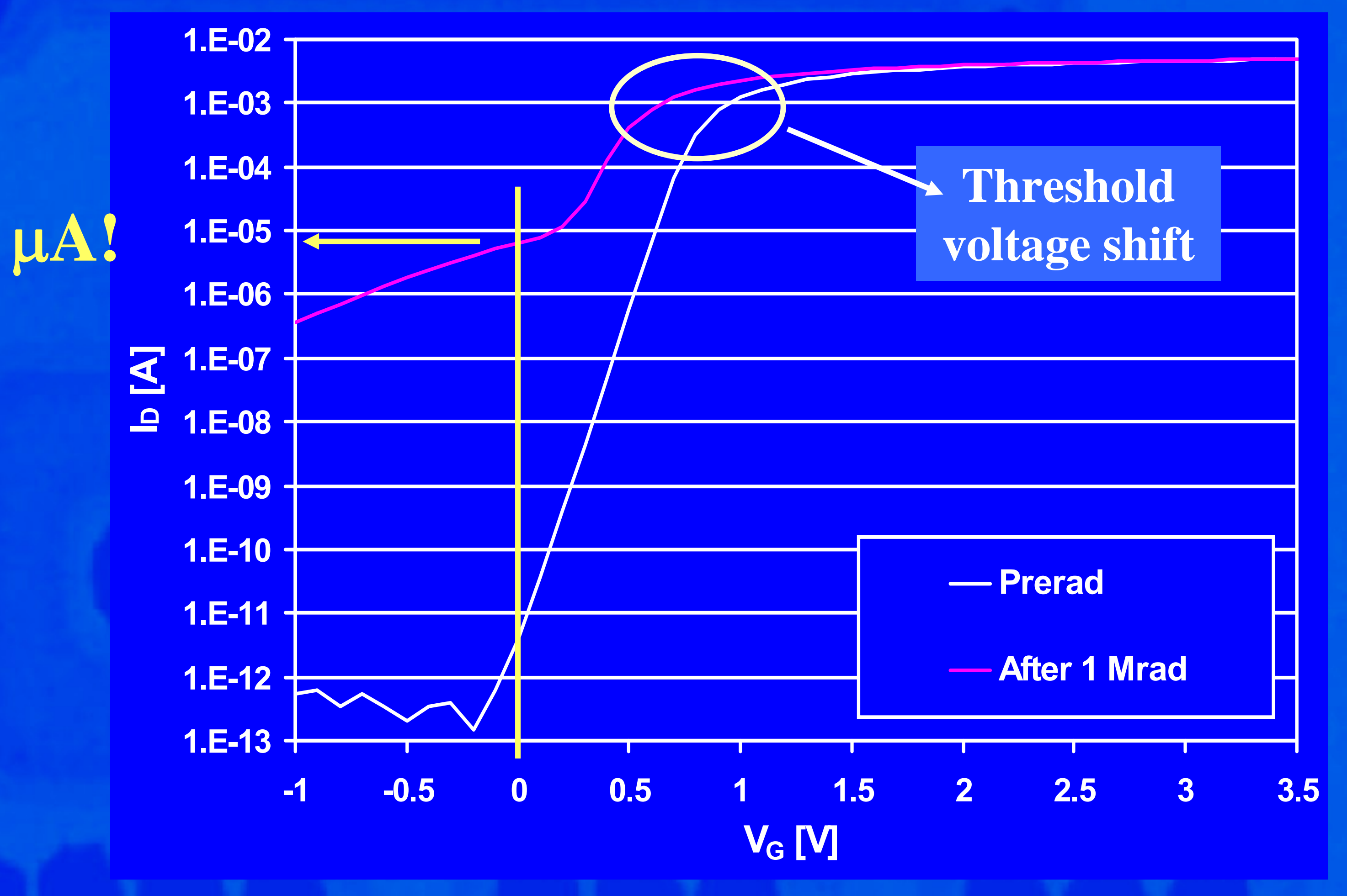
This is for LOCOS, very similar for STI



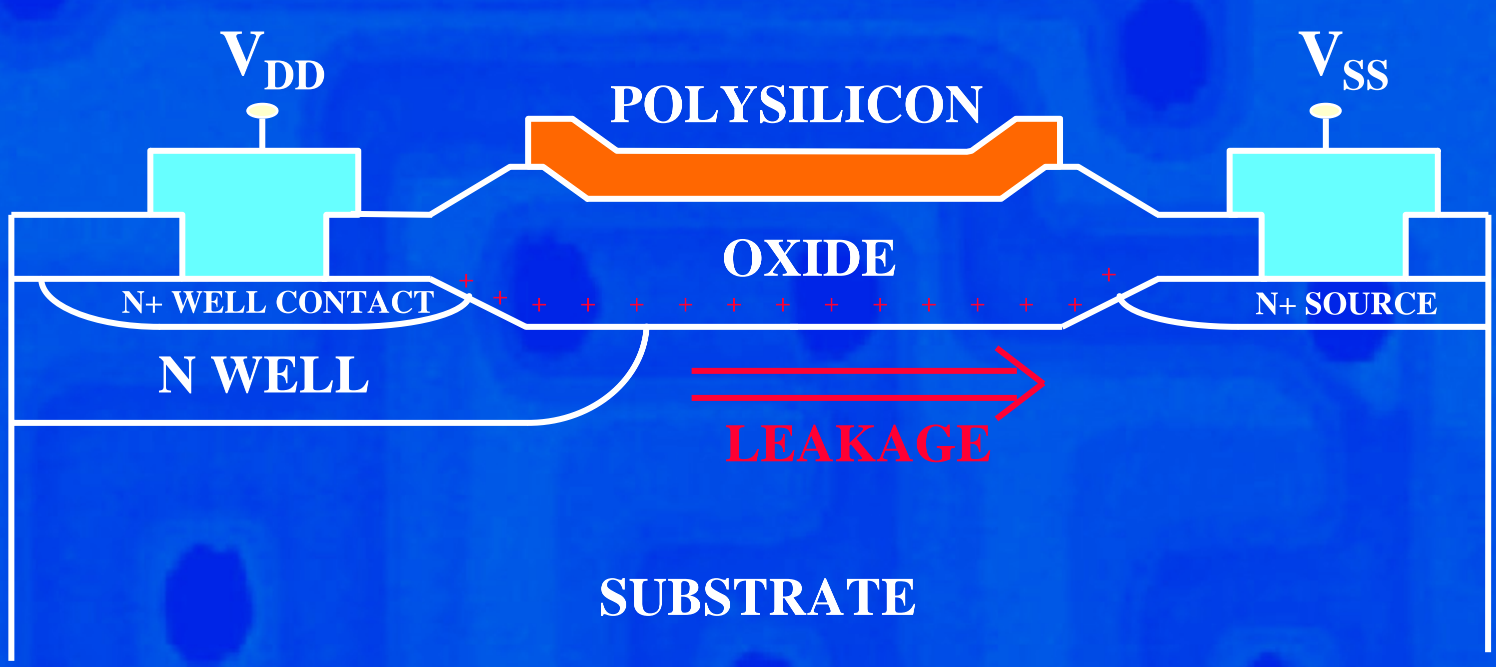
Transistor level leakage: example

NMOS - 0.7 μm technology - t_{ox} = 17 nm

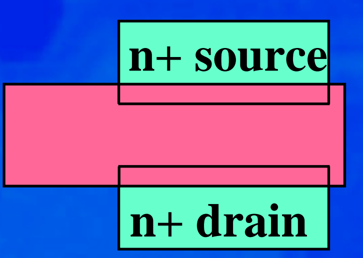
μA!

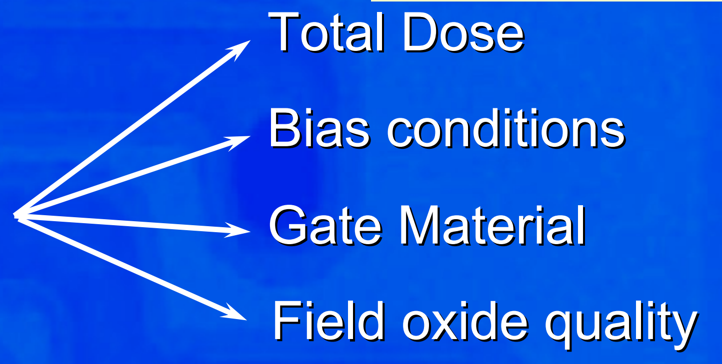


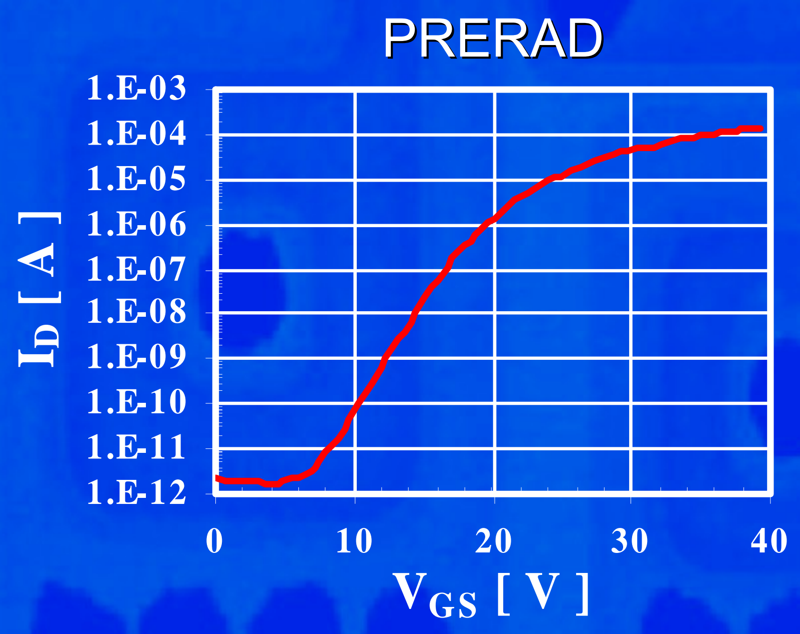
IC level leakage

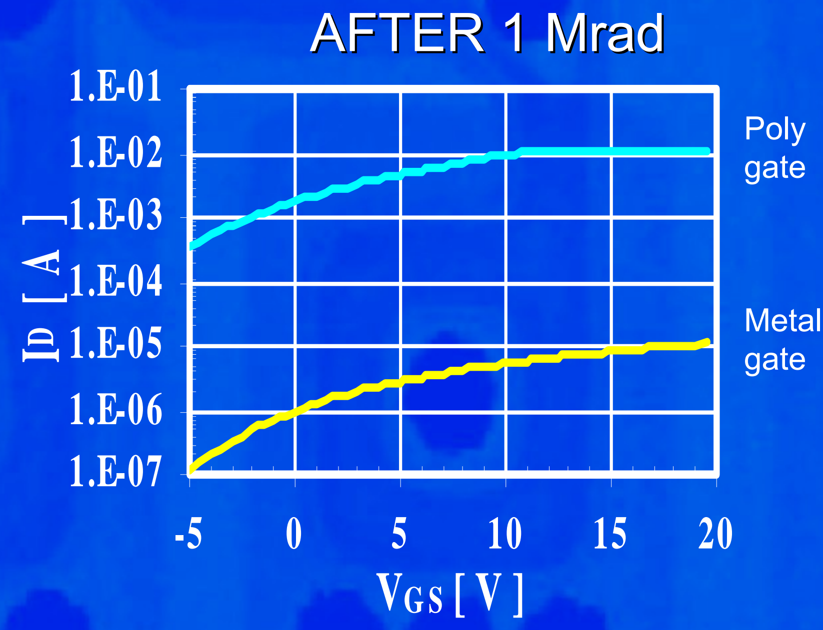


IC level leakage - FoxFETs



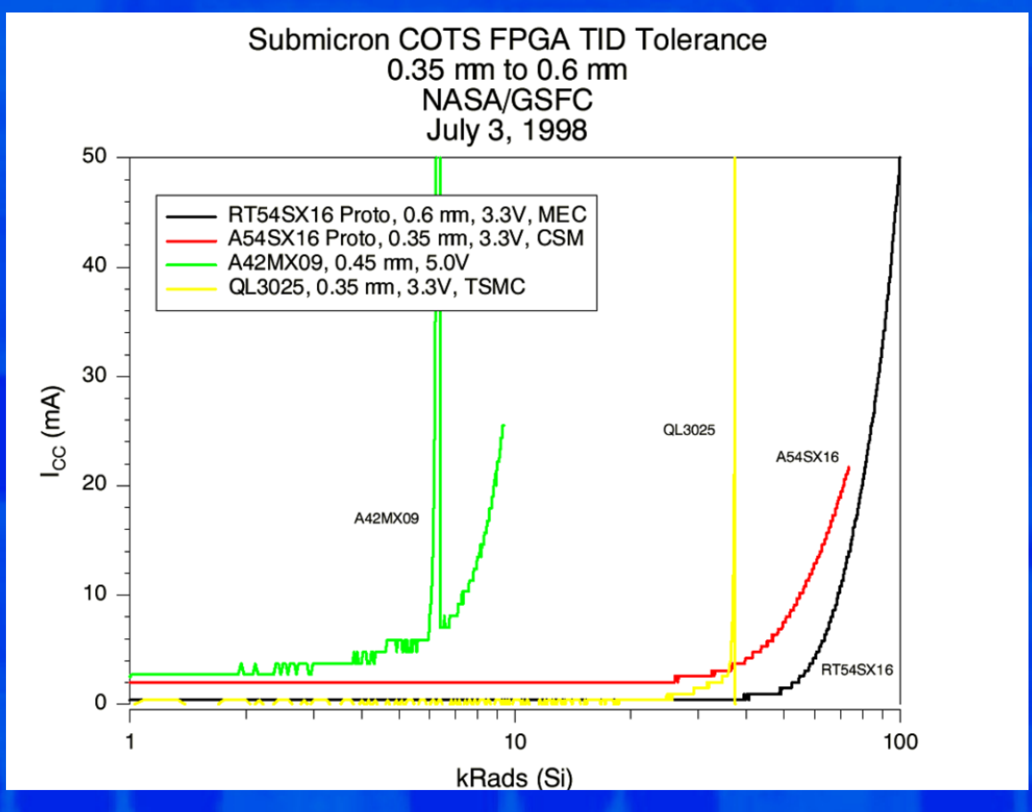






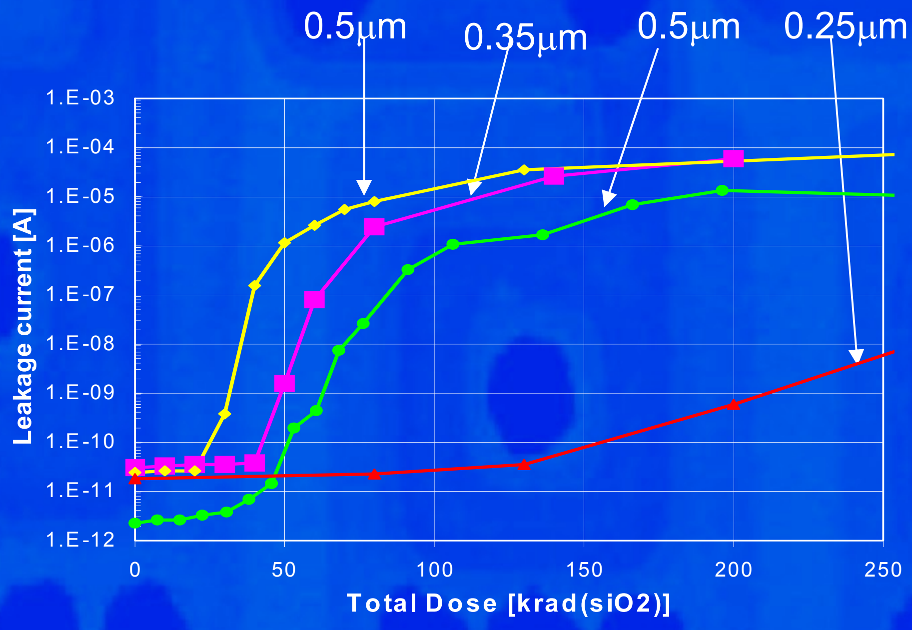
TID-induced failure

- ✓ In modern technologies, leakage current is typically the killer



Is it a problem for me?

- ✓ Which TID can be considered as “safe”?
- ✓ Is there a dependence on design (logic vs analog, …)?
- ✓ Is there variability with time (different results for different production lots)?
- ✓ Is there a technological dependence on the TID tolerance?



Risk management

- ✓ As seen before, there are many variables influencing the final radiation hardness of an IC
- ✓ The "safer" the circuit is designed, the more "expensive" it is (area, performance, complexity, …)
- ✓ Risk reduction comes at some cost

- ✓ In the following, a procedure to RELIABLY designing radiation tolerant ASICs is presented. It reposes on physics, not on specific process recipes, hence it gives very predictable results.

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Radiation hard CMOS processes

- ✓ "Usual solution": technology hardening
- ✓ TID hardness is guaranteed

but

- ✓ Low volume in fabs => yield can be low, and unreliable radiation performance for large quantities
- ✓ Cost is very high
- ✓ Very limited number of processes still available today, and risk of unavailability in the long run
- ✓ Analog performance often not very good

Moore's law

1965: Number of Integrated Circuit components will double every year

G. E. Moore, "Cramming More Components onto Integrated Circuits", *Electronics*, vol. 38, no. 8, 1965.

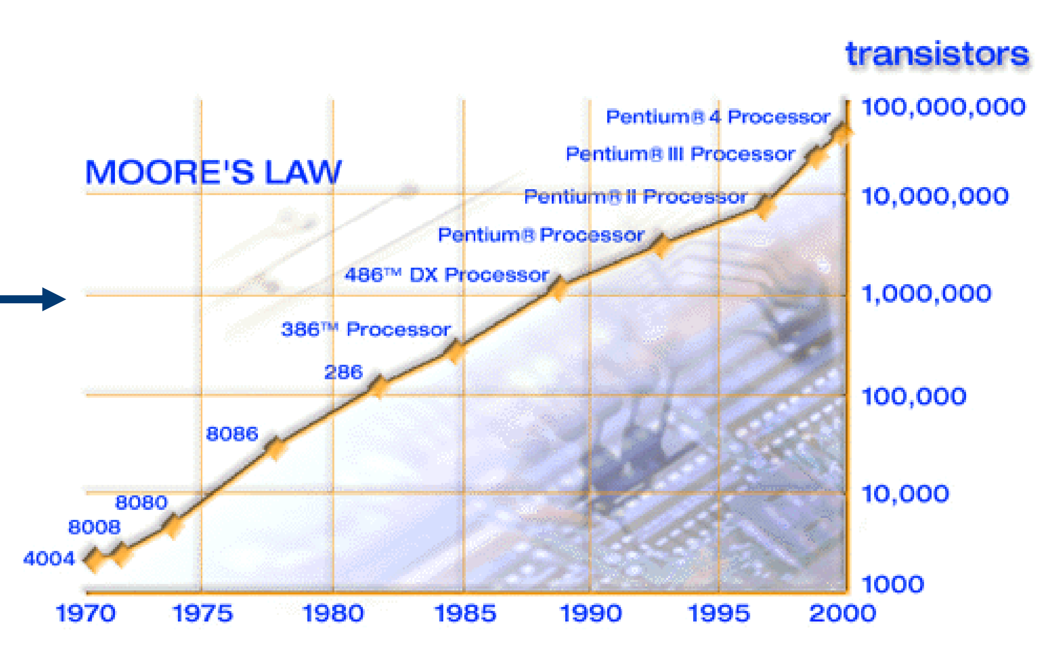
1975: Number of Integrated Circuit components will double every 18 months

G. E. Moore, "Progress in Digital Integrated Electronics", *Technical Digest of the IEEE IEDM 1975*.

1996: The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I don't want to do anything to restrict this definition. - G. E. Moore, 8/7/1996

P. K. Bondyopadhyay, "Moore's Law Governs the Silicon Revolution", *Proc. of the IEEE*, vol. 86, no. 1, Jan. 1998, pp. 78-81.

An example:
Intel's Microprocessors



http://www.intel.com/

Moore's law fundamentals

- ✓ For every generation:
  - CD x 0.7
  - Area x 0.5
  - Chip size x 1.5
  - Structural improvement x 1.3
  - N of components x 4
  - Clock frequency x 1.4

Half pitch definition

DRAM

Metal pitch

MPU/ASIC

Poly pitch

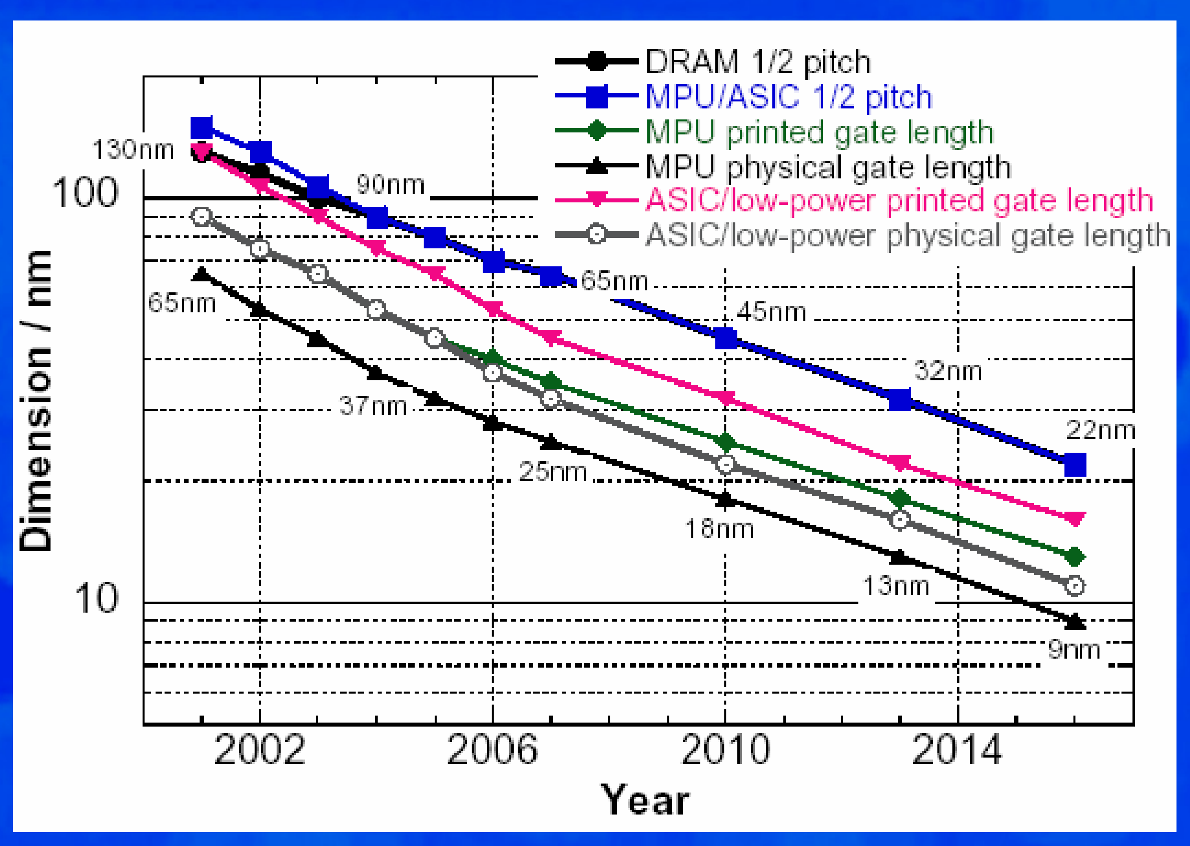
Technology nodes (1/2 pitch):

0.7 0.7

250 -> 180 -> 130 -> 90 -> 65 -> 45 -> 32 -> 22 -> 16

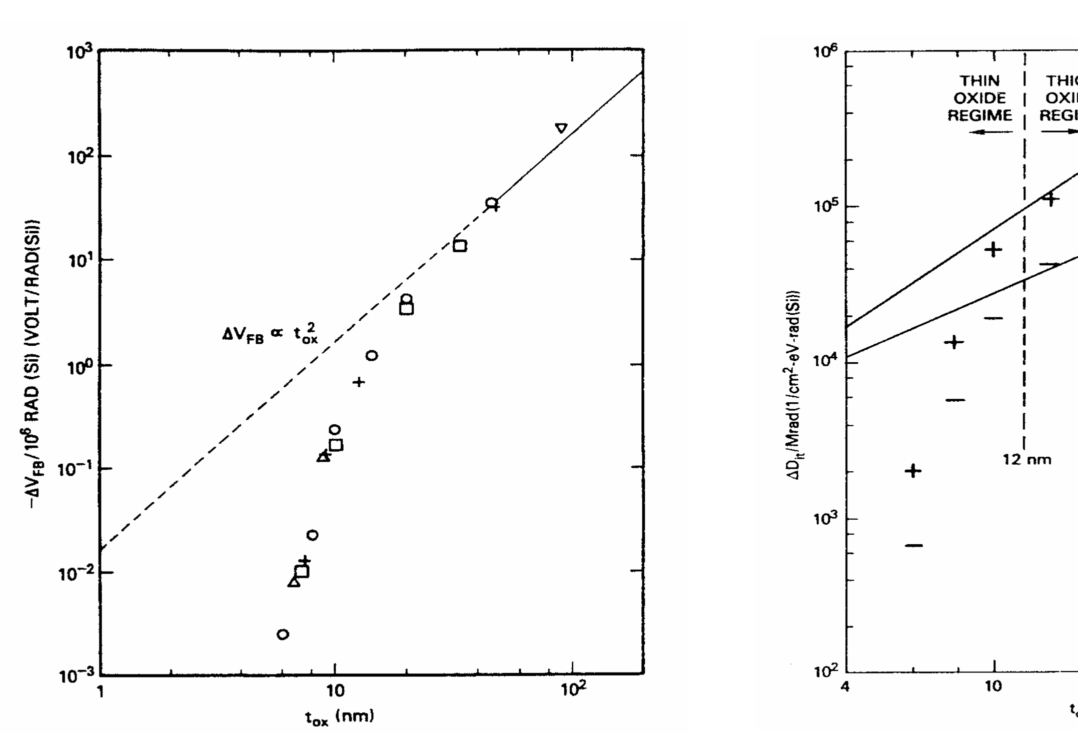
0.5

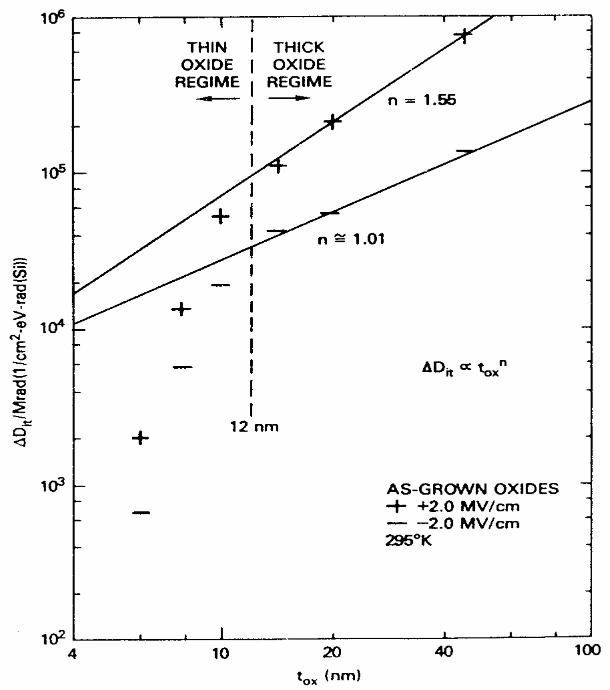
CMOS technology scaling



Radiation effects and t_{ox} scaling

Damage decreases with gate oxide thickness

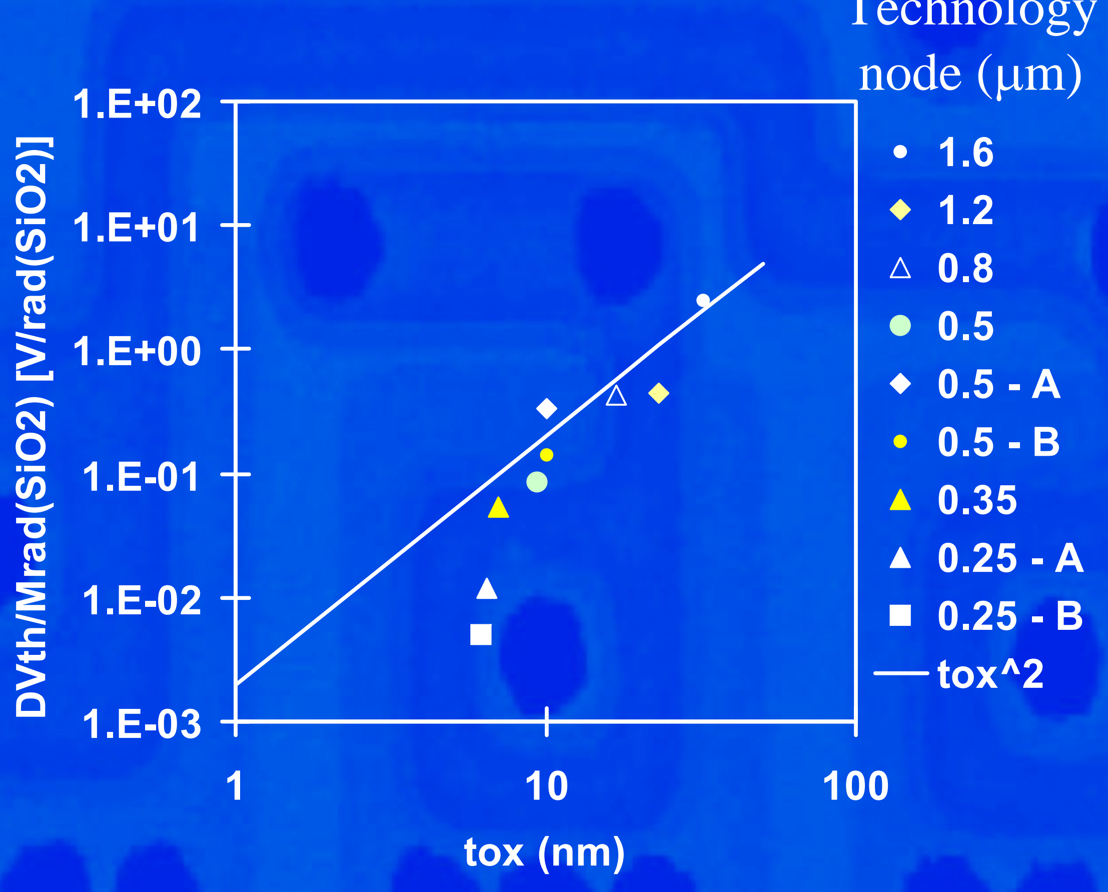




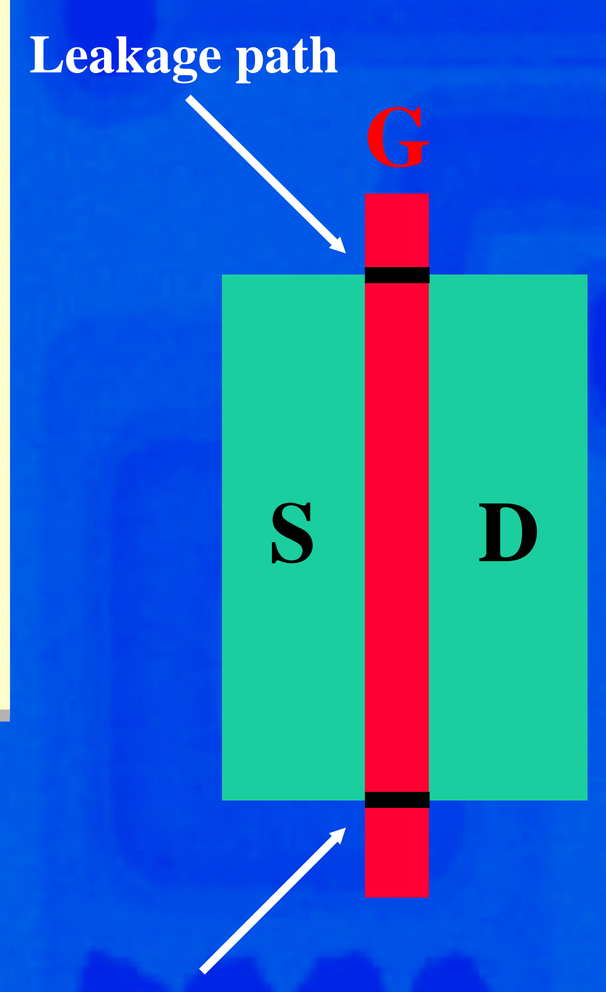
N.S. Saks et al., IEEE TNS, Dec. 1984 and Dec. 1986

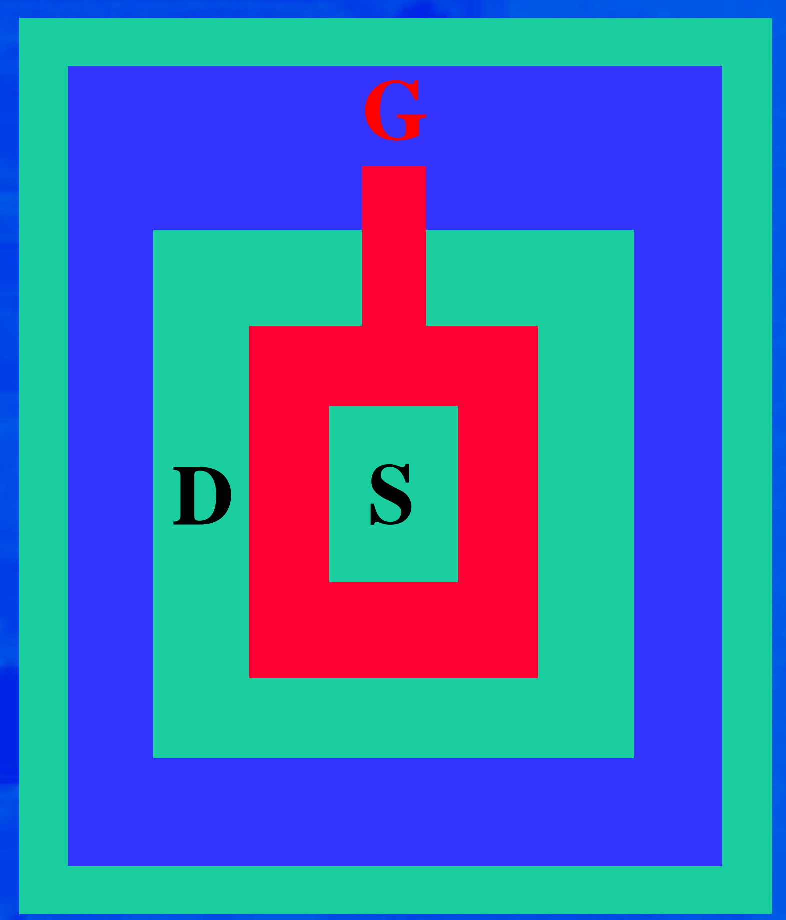
Tendency confirmed

- ✓ Gate oxides in commercial CMOS technologies did follow the curve drawn by Saks and co-workers!

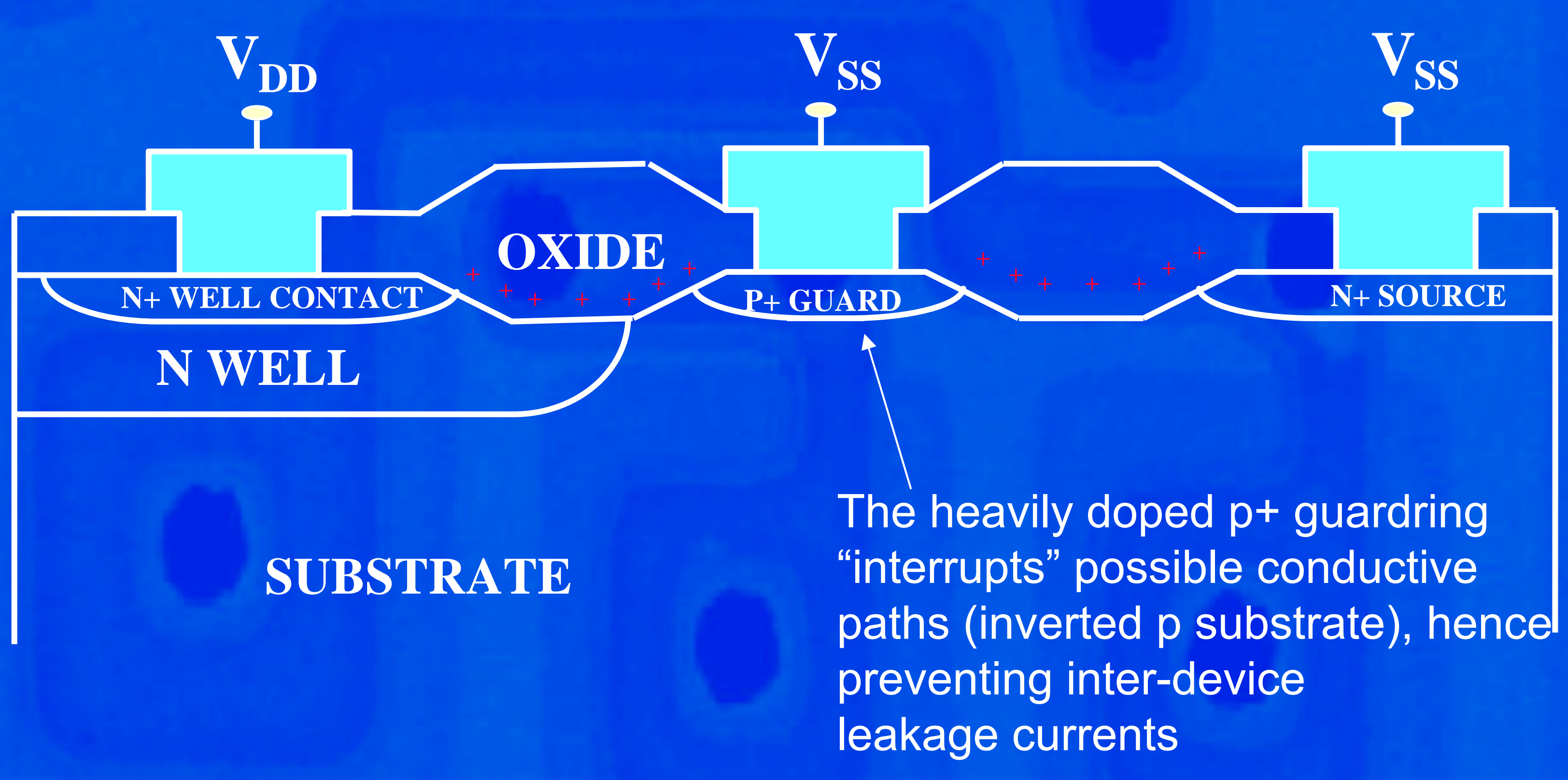


Radiation-tolerant layout (ELT)





Function of the guardring

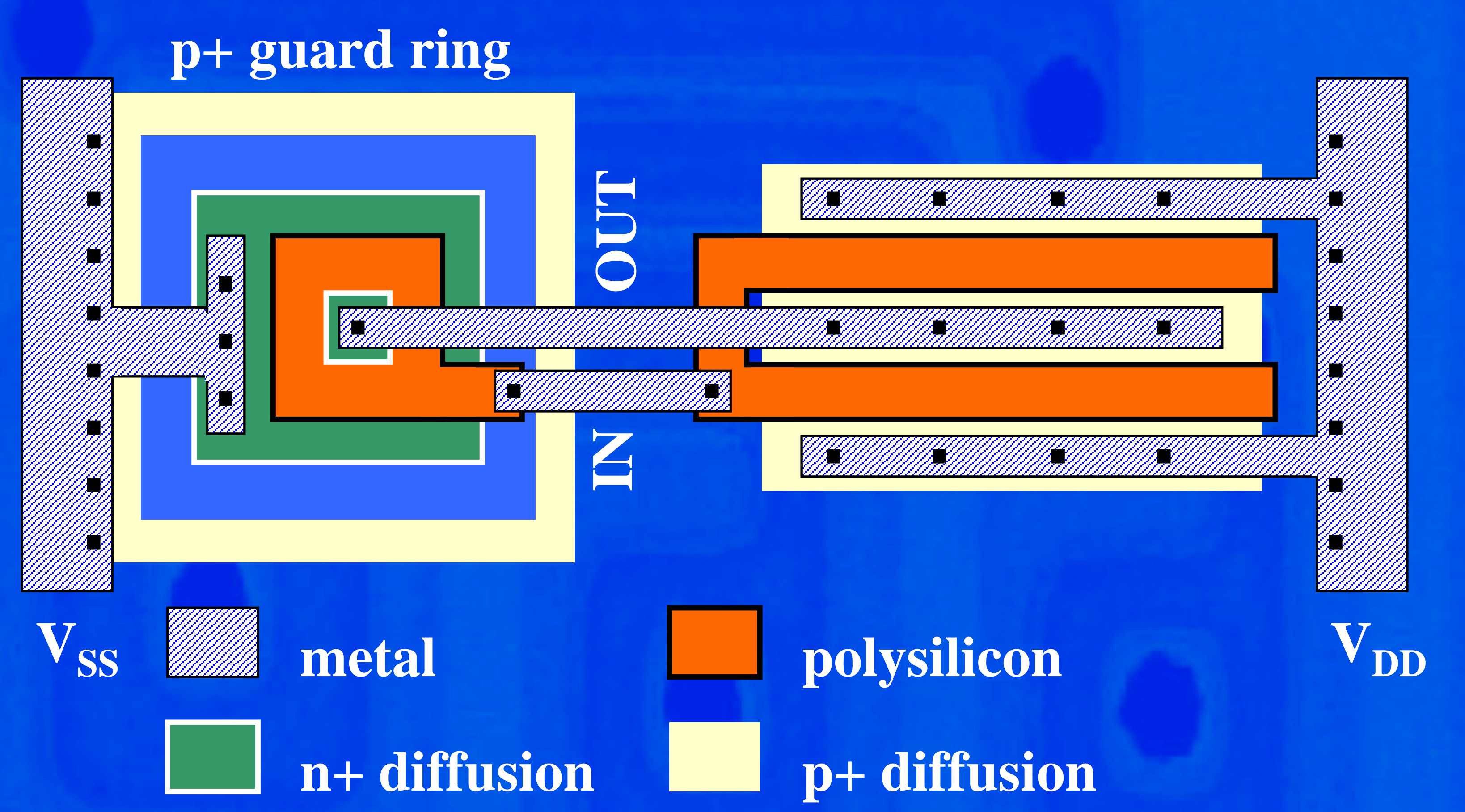


The heavily doped p+ guardring "interrupts" possible conductive paths (inverted p substrate), hence preventing inter-device leakage currents

Radiation tolerant approach

$\Delta V_{th} \propto t_{ox}^{n}$ + **ELT's and guard rings** = **TID Radiation Tolerance**

Layout example (inverter)



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  - Effects (reminder)
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    - Results and difficulties
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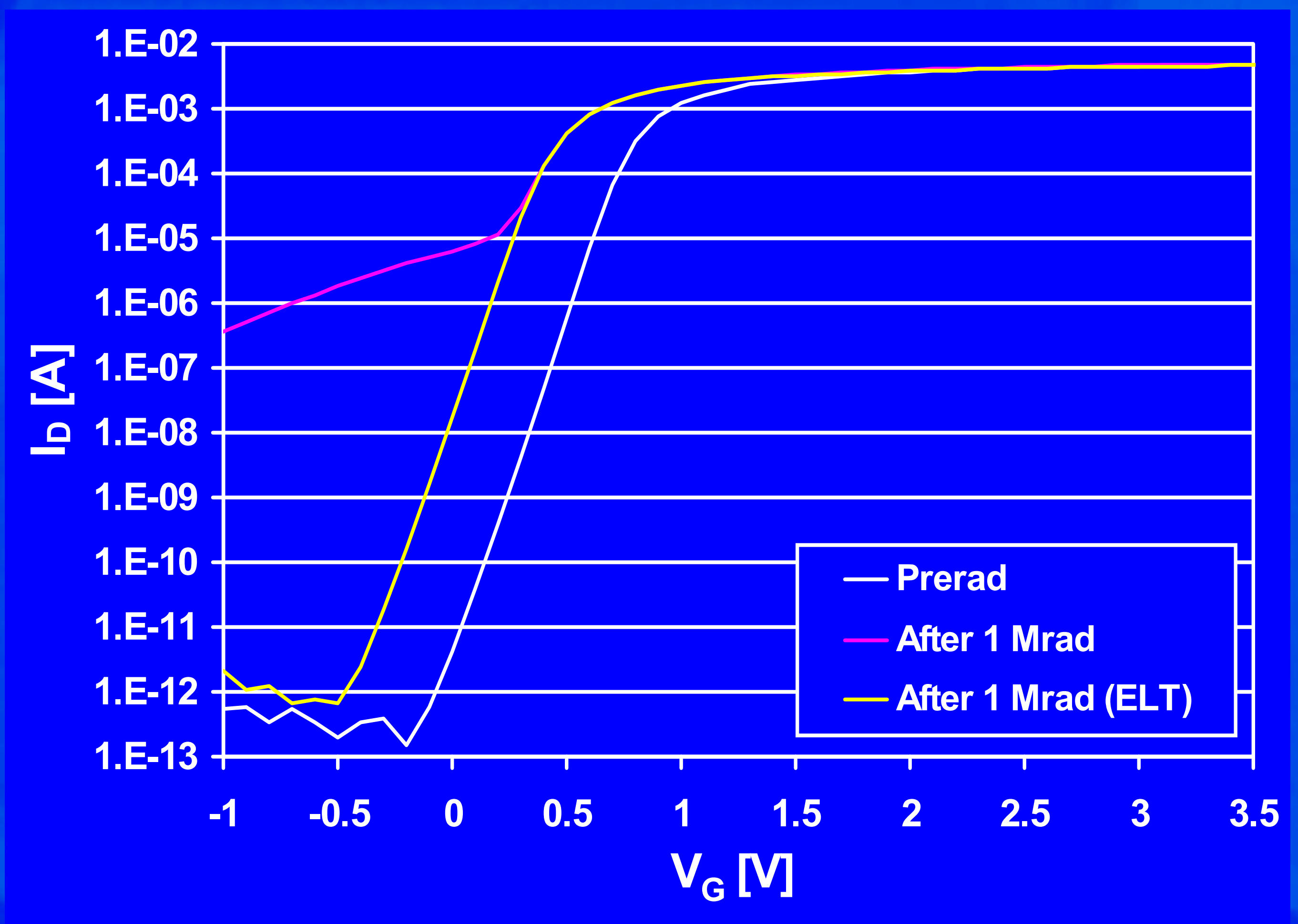
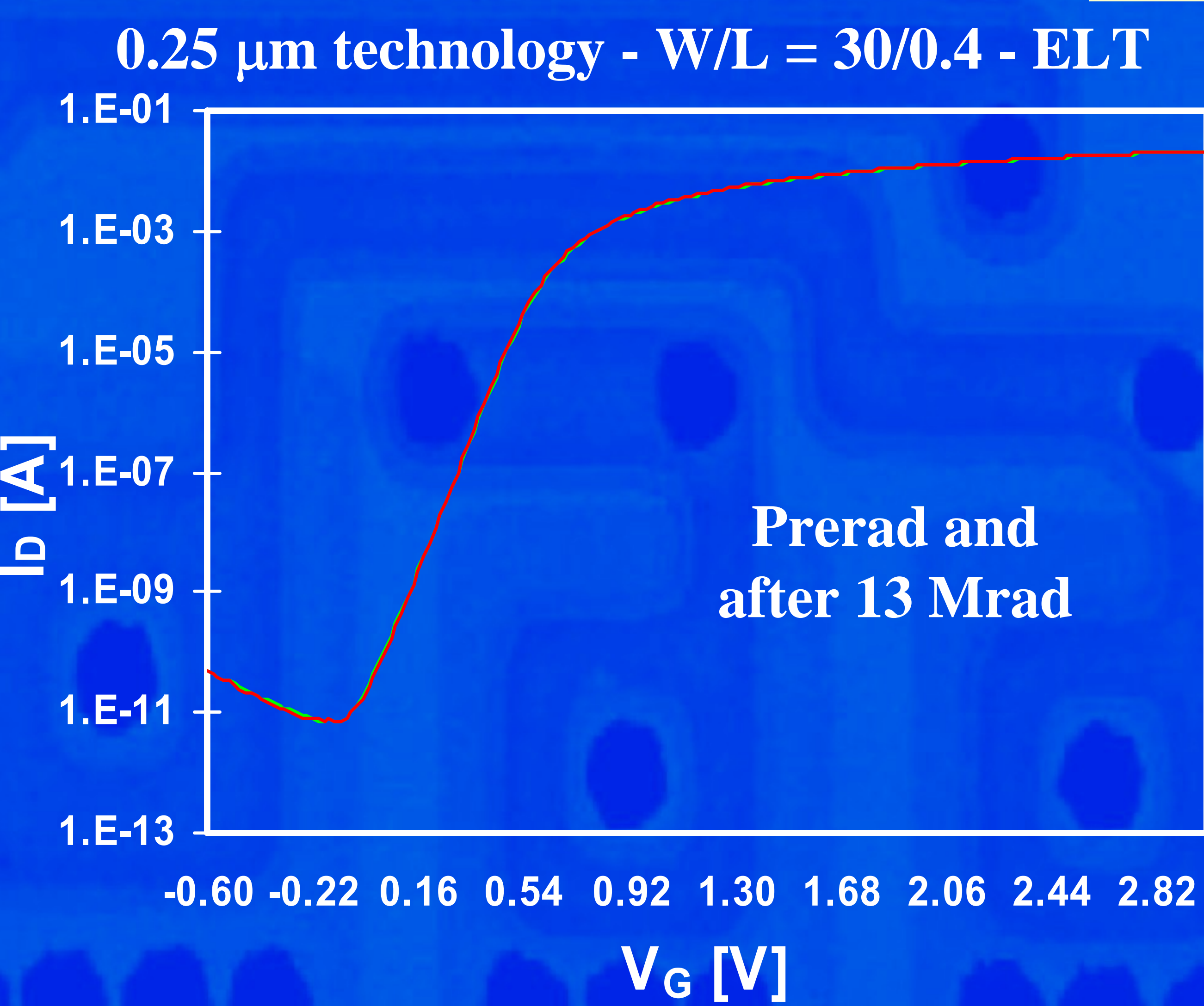
Effectiveness of ELT's

0.7 μm technology - W/L = 2000/1.5

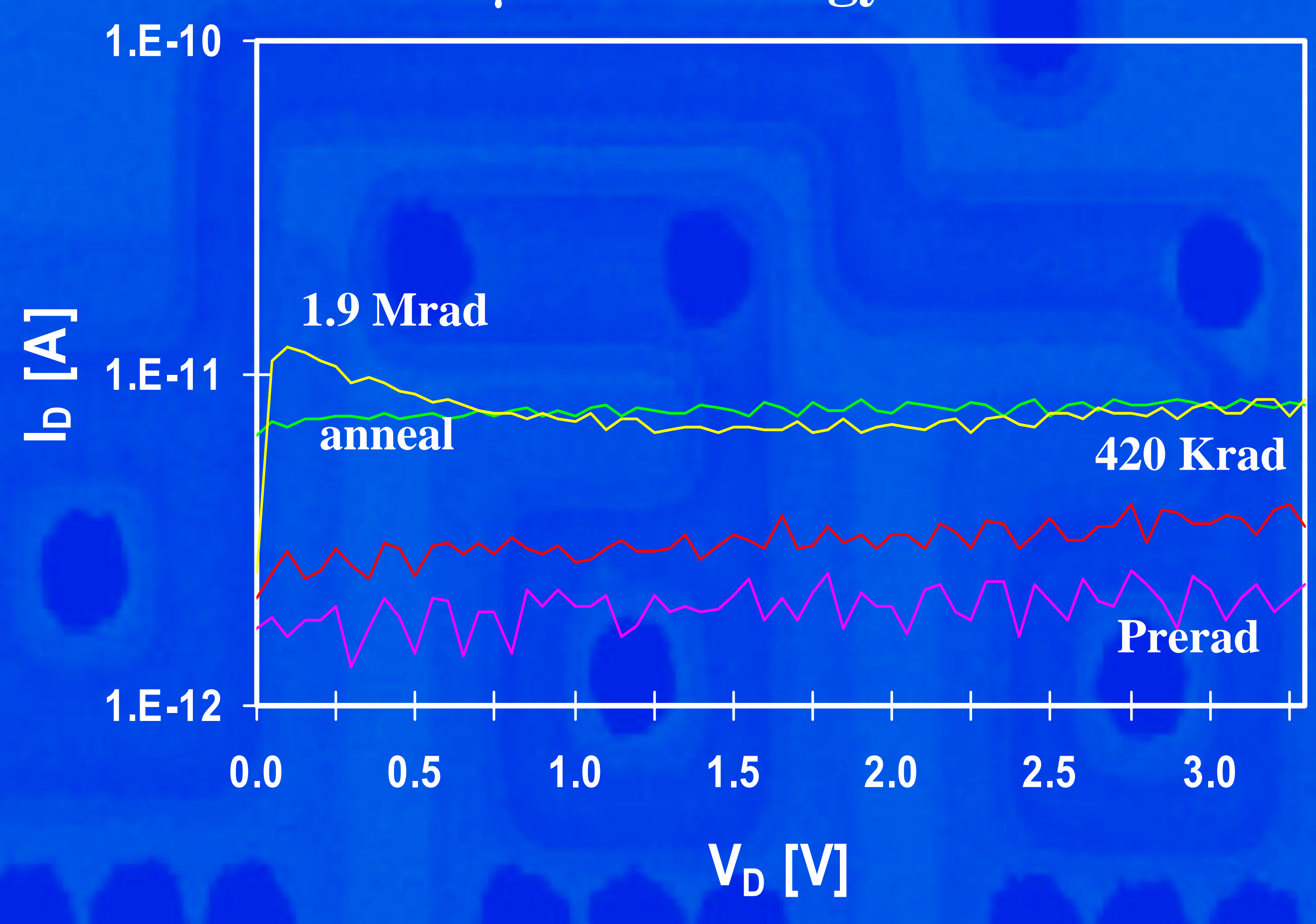


Effectiveness of ELTs

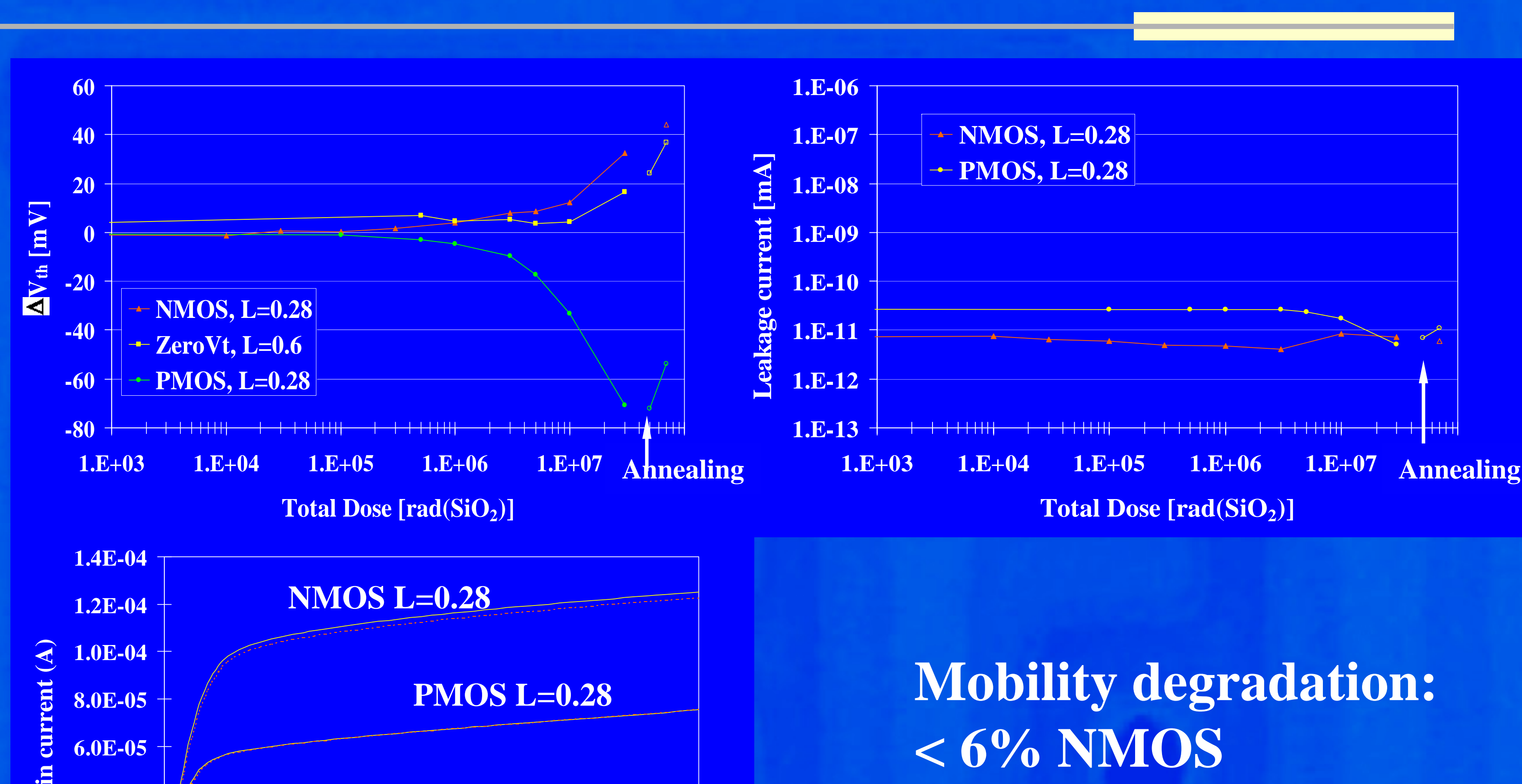


Field oxide leakage

FOXFET 14.4/2.6 without gate, with guardring
0.5 µm technology



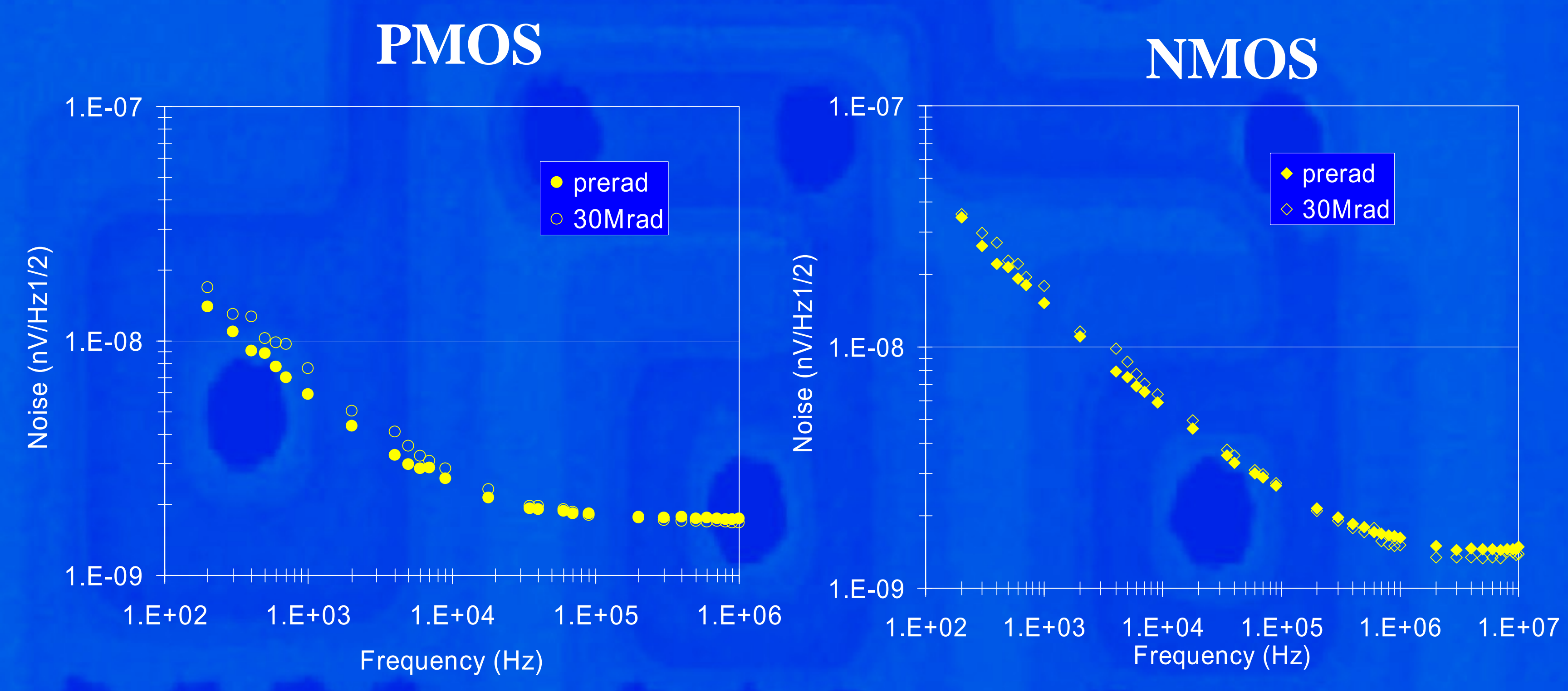
Summary results in 0.25μm



Mobility degradation:
< 6% NMOS
< 2% PMOS

Noise performance

W=2000μm; L=0.5μm



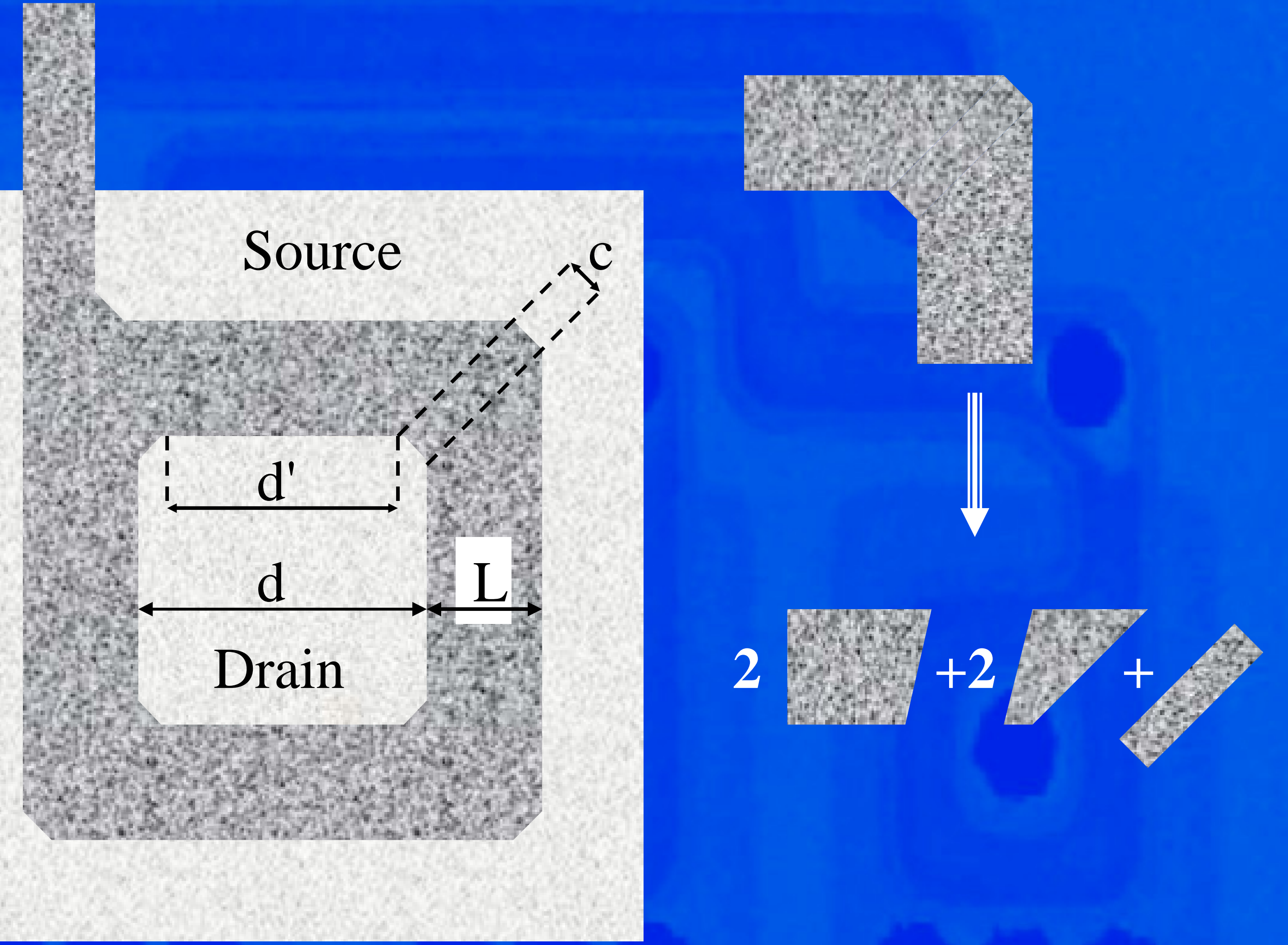
Advantages of this approach

- ✓ Relies on physics (thickness of gate oxide): not process-dependent
- ✓ Allows for using state-of-the-art technologies:
  - Low power
  - High performance
  - High throughput, high yield, short turnaround times
  - Low cost

Difficulties for this approach

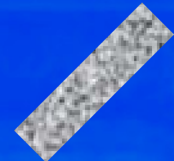
- ✓ Peculiar ELT behaviour
  - Modeling of ELT (size W/L?)
  - Limitation in aspect ratio
  - Asymmetry
- ✓ Lack of commercial library for digital design
- ✓ Loss of density
- ✓ Yield and reliability???

Modeling of ELTs (1)



Modeling of ELTs (2)

$$\left(\frac{W}{L}\right)_{eff} = 4\frac{2\alpha}{\ln\dfrac{d'}{d' - 2\alpha L_{eff}}} + 2K\frac{1-\alpha}{1.13\cdot\ln\dfrac{1}{\alpha}} + 3\frac{\dfrac{d-d'}{2}}{L_{eff}}$$

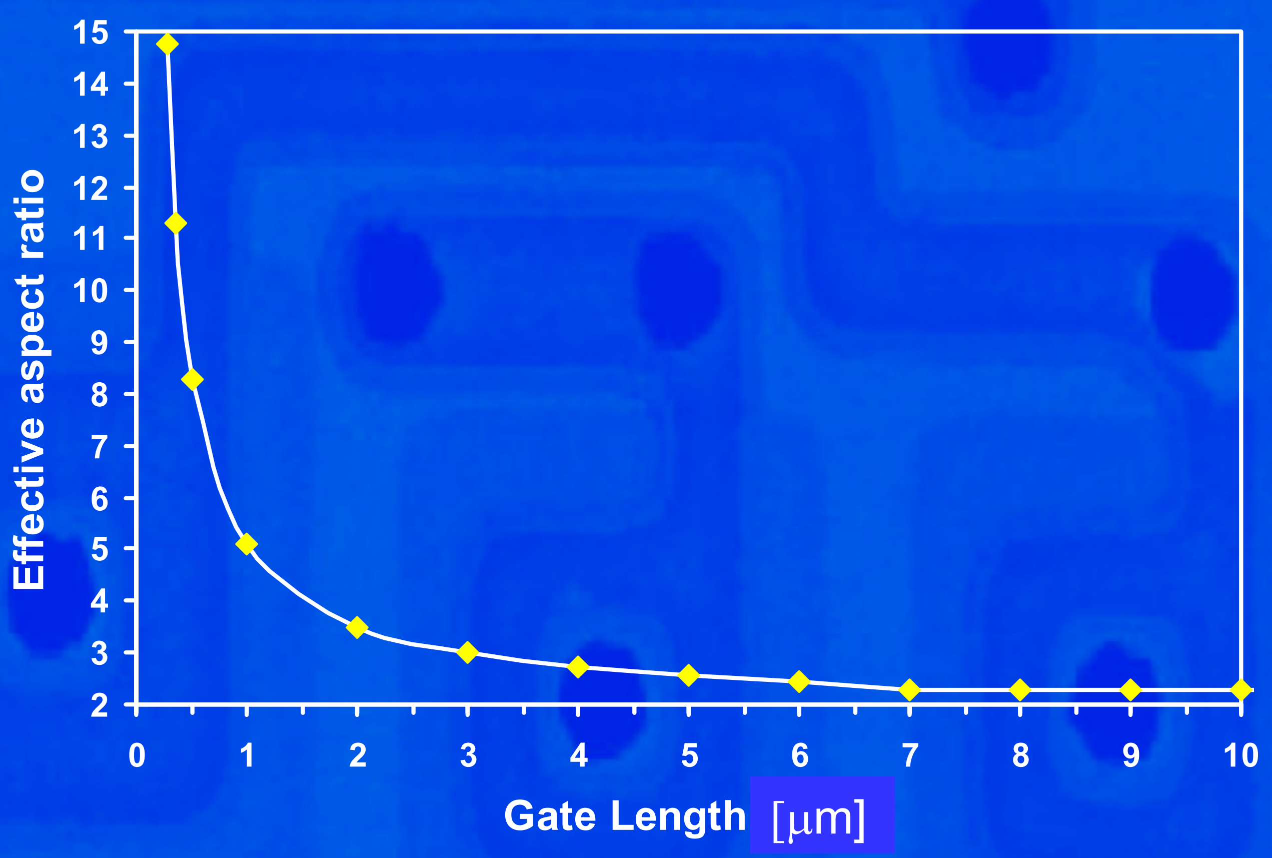


L_{drawn}	Estimated $(W/L)_{eff}$	Extracted $(W/L)_{eff}$
0.28	14.8	15
0.36	11.3	11.2
0.5	8.3	8.3
1	5.1	5.2
3	3	3.2
5	2.6	2.6

- ✓ 1 shape only supported (size of “c” fixed)
- ✓ Custom routines and layers integrated in design kit for extraction/design checking/computation

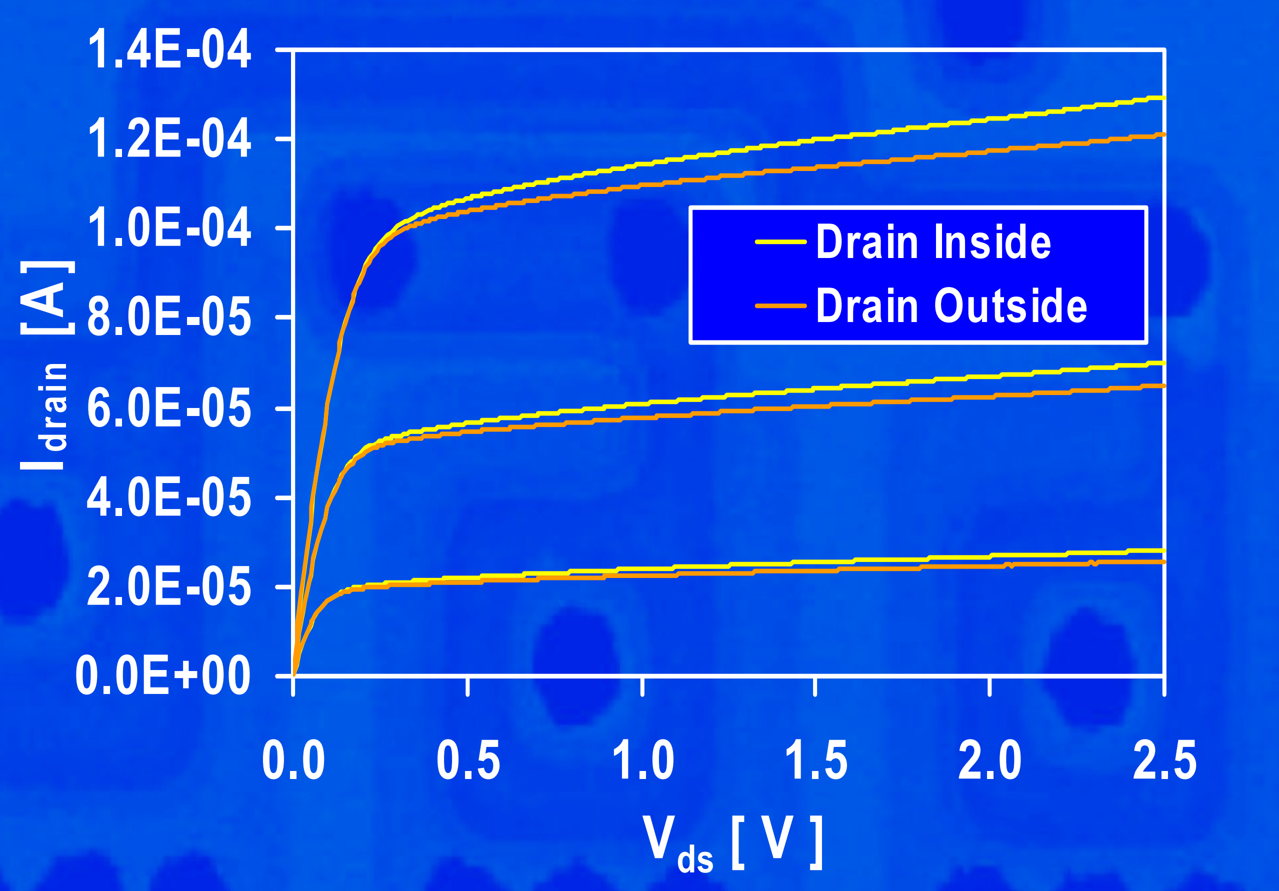
Limitation in the aspect ratio

Aspect ratio = W/L

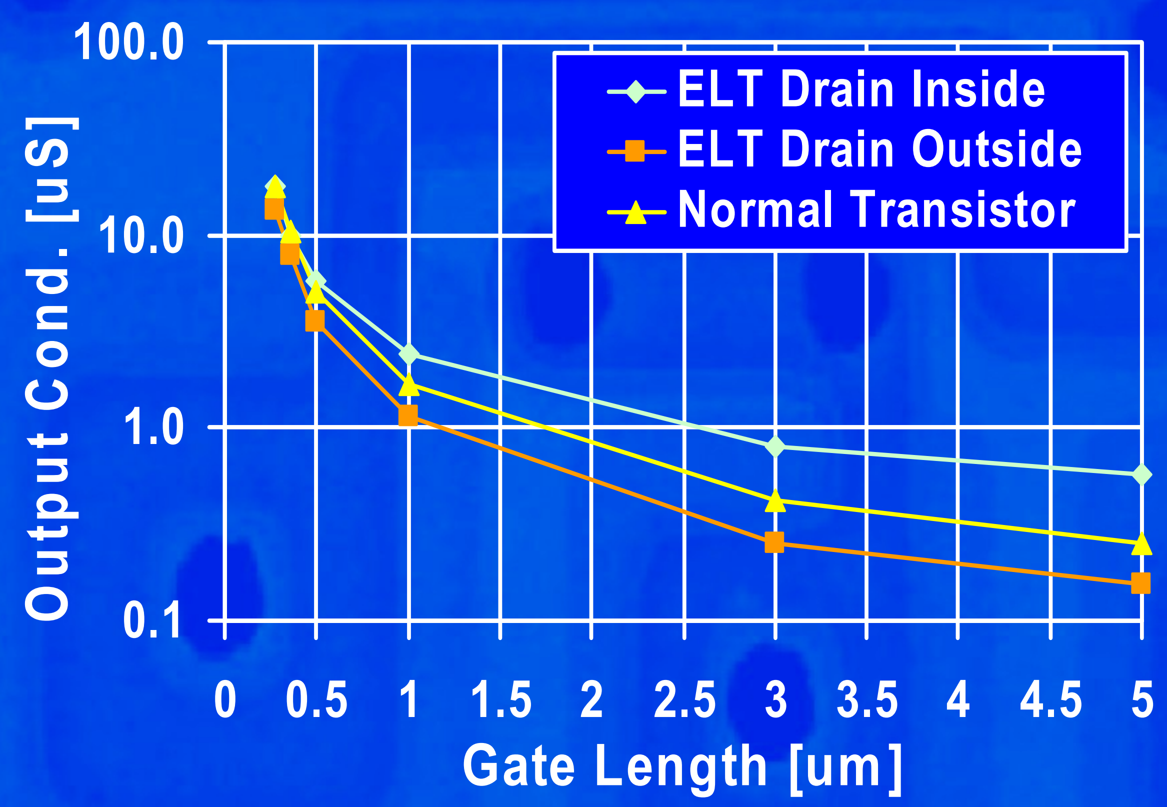


Asymmetry (1)

$L = 0.28\ \mu m \quad G_{DI} = 11.9\ \mu S \quad G_{DO} = 9.6\ \mu S$

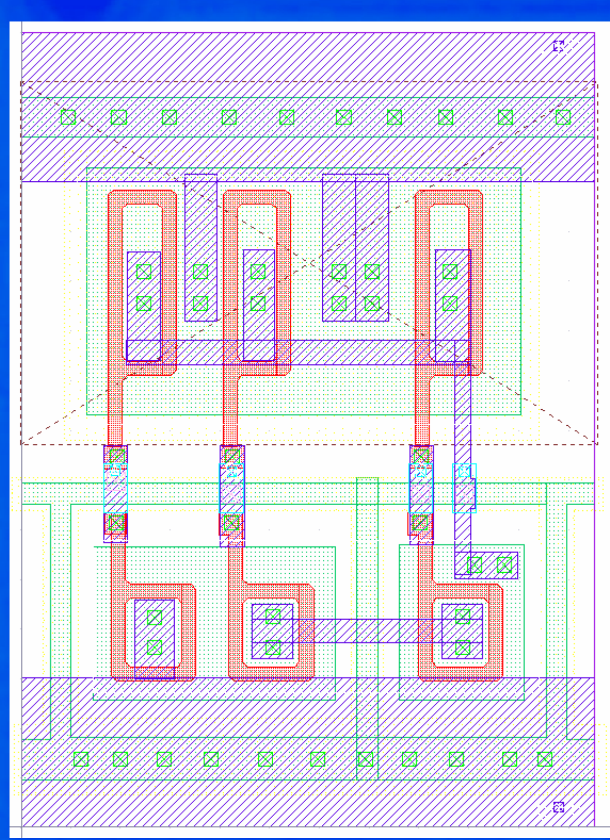


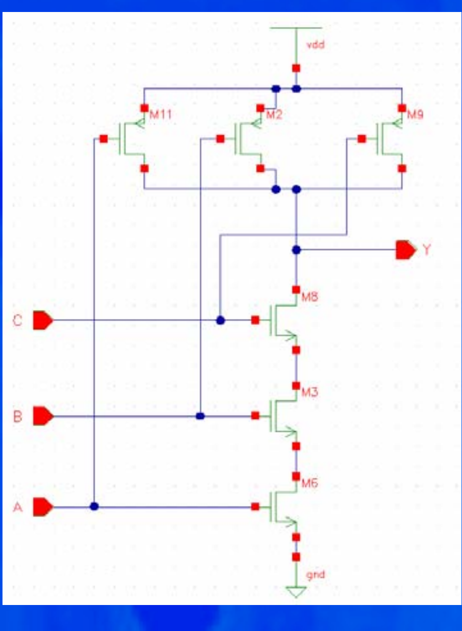
Asymmetry (2)



L (μm)	$\Delta G/G_{DI}$
0.28	19 %
0.36	23 %
0.5	33 %
1	53 %
3	70 %
5	75 %

Lack of commercial library (1)





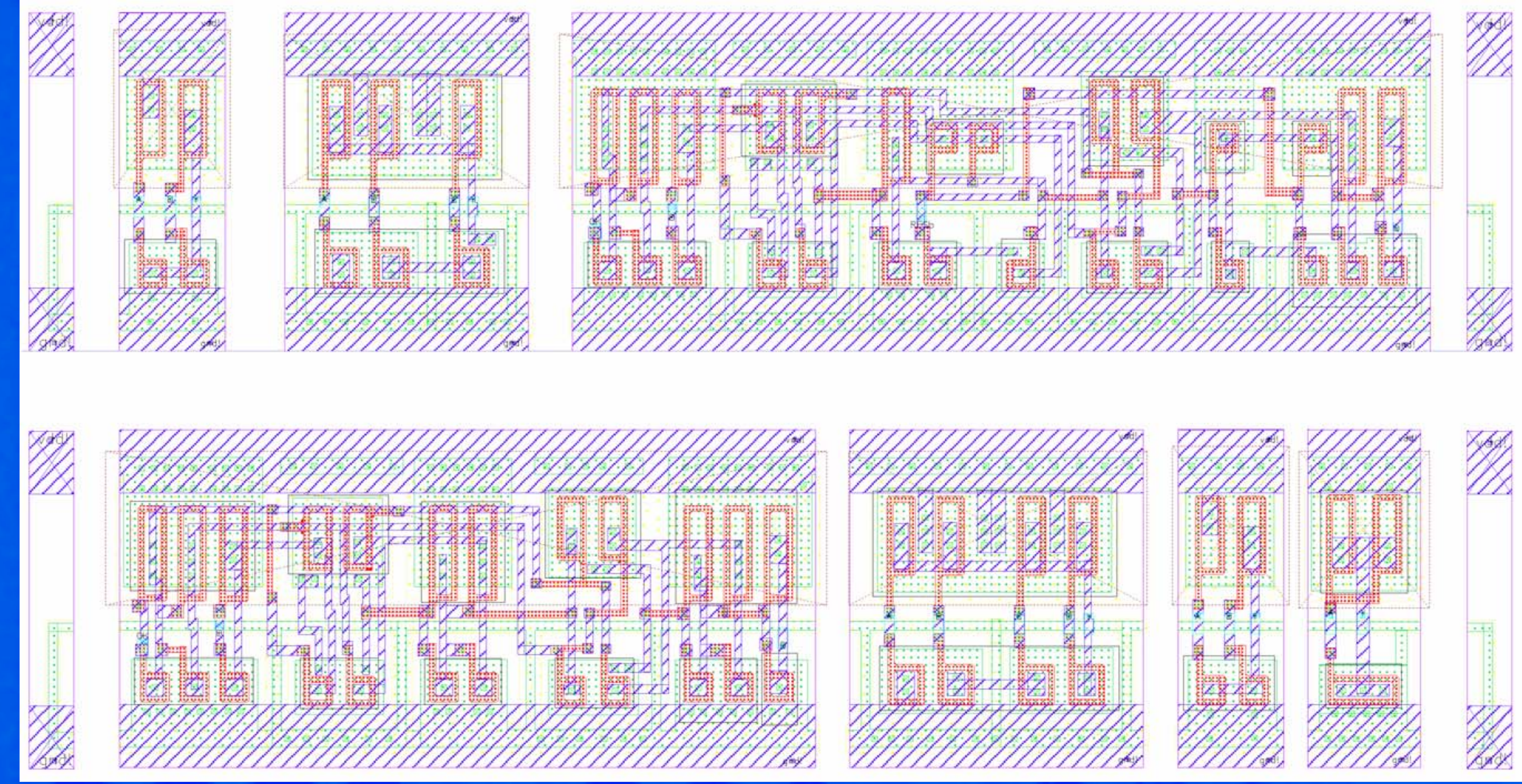
NAND3

Radiation tolerant design :

- Use of enclosed NMOS transistors
- Use of guard rings to isolate all n^+ diffusions at different potentials (including n-wells)

Lack of commercial library (2)

- ✓ Example of core cells



Lack of commercial library (3)

CERNLIB Digital Standard Cells

Core Logic	Cell Name	Trans. count	Size (µm) 16x	Area (μm^2)
Boolean				
Inverter 1X Drive	E_Inv1	2	3	48
Inverter 2X Drive	E_Inv2	3	5	80
Inverter 4X Drive	E_Inv4	6	9	144
Inverter 8X Drive	E_Inv8	10	17	272
2 Input NAND	E_Nand2	4	7	112
3 Input NAND	E_Nand3	6	12	192
4 Input NAND	E_Nand4	8	14	224
2 Input NOR	E_Nor2	4	5	80
3 Input NOR	E_Nor3	6	11	176
4 Input NOR	E_Nor4	8	21	336
2 Input XNOR	E_Xnor2	12	18	288
Complex Gates				
2-Wide 2-Input AND-OR	E_AO22	10	16	256
2-Wide 2-Input AND-OR-INVERT	E_AOI22	8	13	208
2-Wide 2-Input OR-AND-INVERT	E_OAI22	8	12	192
Multiplexers				
2-Input MUX	E_Mux2	12	18	288
4-Input MUX	E_Mux4	28	40	640
Buffers				
Buffer X4 Drive	E_Buf4	8	11	176
Buffer X8 Drive	E_Buf8	16	26	416
Simple Cells				
Logic 0	LOGIC0	2	3	48
Logic 1	LOGIC1	2	3	48
Adders				
1-bit Half Adder	E_HAD1	18	27	432
1-bit Full Adder	E_FAD1	34	45	720
Flip Flops				
Static D FLIP-FLOP	E_dff	24	33	528
Static D FLIP-FLOP with Reset	E_dff_R	28	41	656
Static D FLIP-FLOP with Set	E_dff_S	28	41	656
Static D FLIP-FLOP with Set & Re	E_dff_SR	32	47	752
Static D Flip Flop with Scan	E_dff_SR_SC	40	59	944
Dynamic TSPC D FLIP FLOP	E_TSPC	11	19	304
Latches				
D-Latch	E_LD	18	25	400
D-Latch with Reset	E_LDR	21	29	464

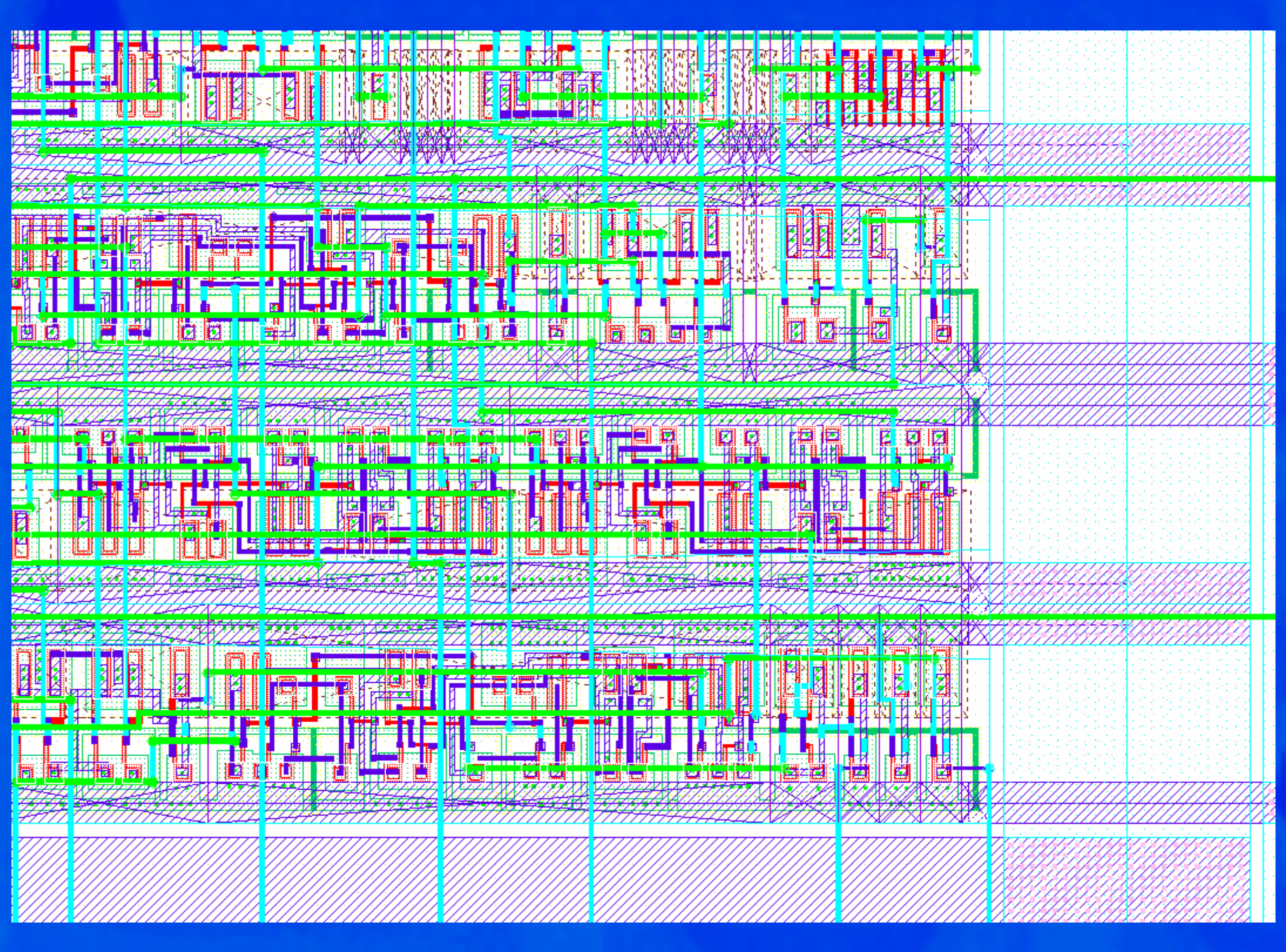
I/O Logic	Cell Name	Trans. count	Size (µm) 458x	Area (μm^2)
Output Pads				
8mA Drive Standard	OB8mA	16	115	51865
16mA Drive Standard	OB16mA	26	115	51865
20mA Drive Standard	OB20mA	34	115	51865
8mA Drive with Slew Rate control	OBSR8mA	14	115	51865
16mA Drive with Slew Rate control	OBSR16mA	30	115	51865
20mA Drive with Slew Rate control	OBSR20mA	38	115	51865
Input Pads				
CMOS Inverter Input	IB1	6	115	51865
Simple PAD	INPAD	0	115	51865
LVDS I/O Pads				
LVDS TX	LVDStx	33	235	105985
LVDS RX	LVDSrx	18	235	105985
I^2C interface I/O Pads				
20mA Open Drain Output	OD20mA	9	115	51865
Bidirectional with 20mA Open Drain	IOD20mA	17	115	51865
Power Pads				
VDD for periphery & core	VDD	0	115	51865
VDD for periphery	VDD_CORE	0	115	51865
VDD for core	VDD_PERI	0	115	51865
VSS for periphery & core	VSS	0	115	51865
VSS for periphery	VSS_CORE	0	115	51865
VSS for core	VSS_PERI	0	115	51865
Corner for I/O periphery	CORNER	0	115	51865
Guard-ring cells				
Endcap Cell Left	CAPL	0	115	51865
Endcap Cell Reft	CAPR	0	115	51865
Filler Cell	FILLERCELL	0	115	51865

- ✓ List of Library Standard Cells

Lack of commercial library (4)

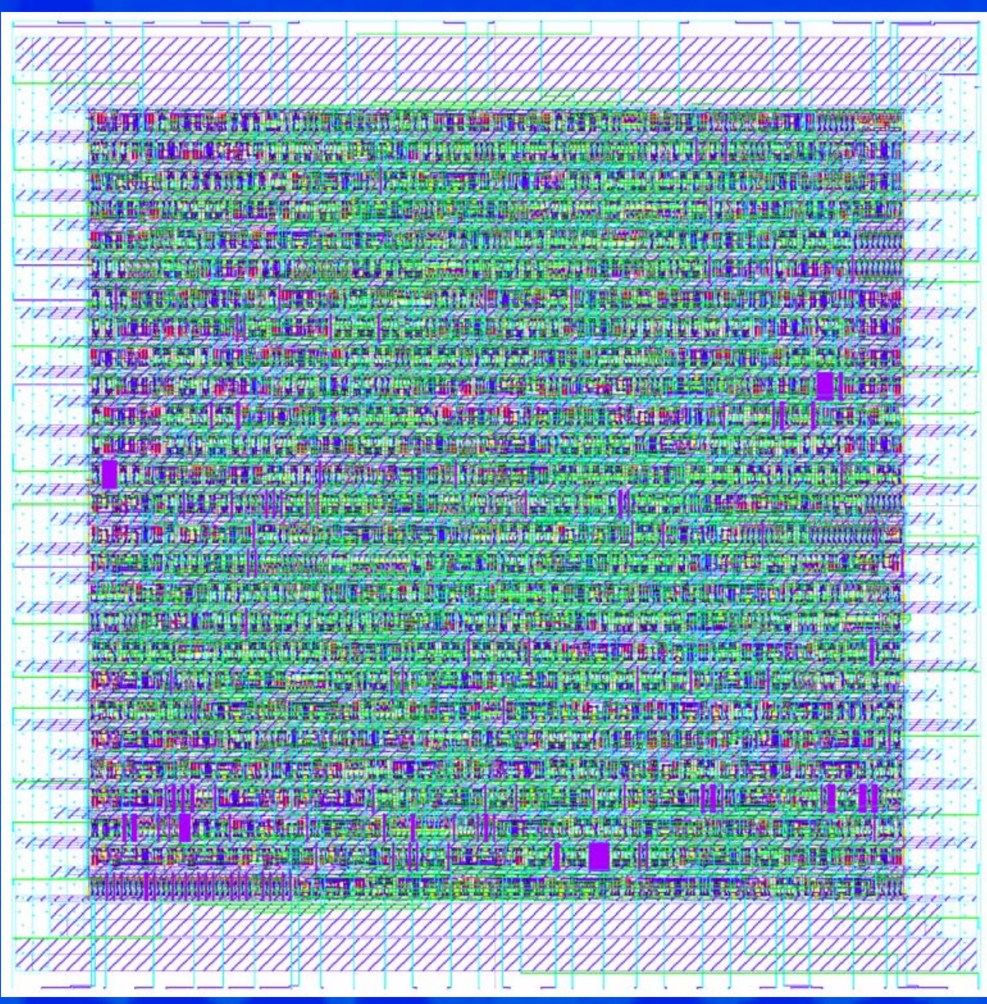
- ✓ Development of a "Design Kit" for CADENCE DFII version 97a
- ✓ Supported Design Flows:
  - Analog
    - Analog simulations (HSPICE).
    - Device extraction.
    - Physical Design Verification (DIVA, DRACULA).
  - Digital
    - Logic Synthesis (SYNOPSYS).
    - Digital Simulations (VERILOG).
    - Place & Route (SILICON ENSEMBLE).
  - Mixed Signal
    - Simulations (HSPICE/VERILOG).

Lack of commercial library (5)



- ✓ P&R tool: Silicon Ensemble
- ✓ Maze Router
  - No channels
  - Flip &Abut the cells
- ✓ Special support for Rad-Tol layout design.
- ✓ Interrconnection : 3 metal layers, upgradable to 6

Lack of commercial library (6)



- ✓ Example: control logic of the APV25 chip
- ✓ No of cells: ~ 900
- ✓ Area: 192,672µm^2
- ✓ Metal Layers: 3
- ✓ Synthesized Logic

Existing libraries

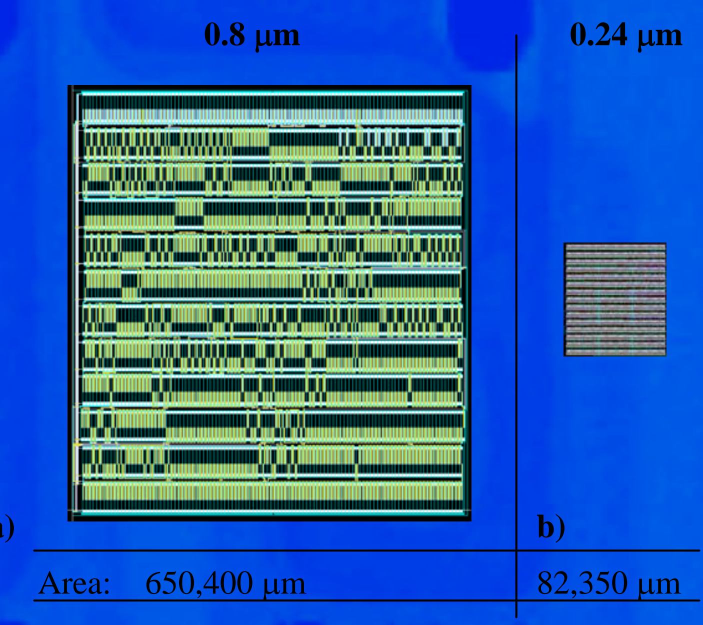
- ✓ List is not exclusive:
  - CERN in 0.25μm
    - "Daughter" libraries in PSI, LBL, Fermilab
  - IMEC (for ESA) in 0.18μm
  - Mission Research Corporation (for Aerospace Corporation) in 0.18μm

Loss of density

- ✓ Radiation Tolerant techniques introduce a ~70% layout area overhead

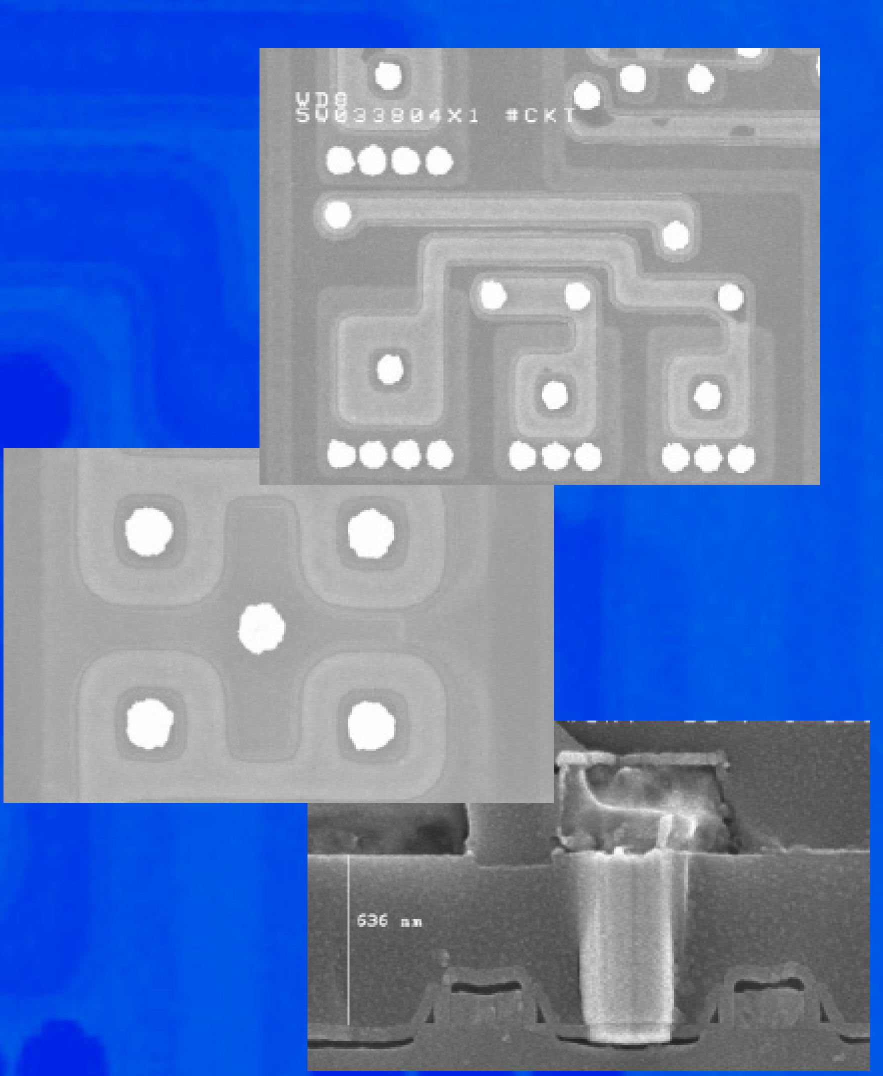
	Standard	Rad-Tol	Penalty
Inverter	33.6 μm^2	50.9 μm^2	34 %
2-in NAND	46.0 μm^2	119.0 μm^2	61 %
2-in NOR	47.8 μm^2	80.0 μm^2	41 %
Static D-F/F	153.0 μm^2	533.1 μm^2	71 %
Static D-F/F SR	188.1 μm^2	572.0 μm^2	75 %

- ✓ Gate density is 8 times larger when compared to a 0.8µm technology
  - Example: ring oscillator with 1280 inverters in 0.8 and 0.25mm technologies (0.25 uses the CERN radtol library)



Yield and reliability?

- ✓ Construction analysis performed on several chips
- ✓ Circuits produced, qualified and tested in thousands (100 different designs!)
- ✓ No concern on yield or reliability found yet…



Outline

- ✓ Foreword: CMOS technologies
- ✓ TID: Total Ionizing Dose
  - Effects (reminder)
  - Solutions
    - ASIC examples
  - Trends in state-of-the-art technologies
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  - Effects (reminder)
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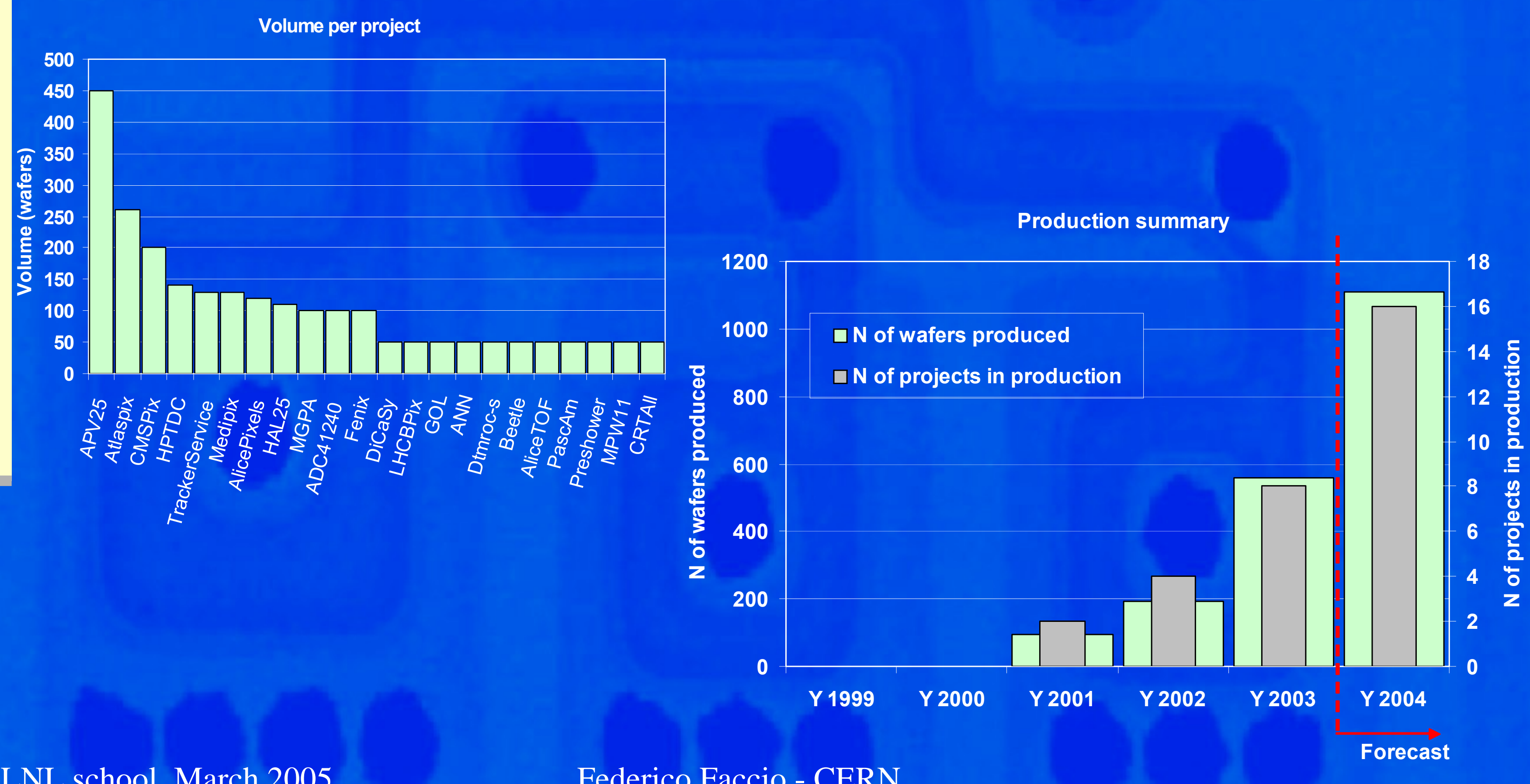
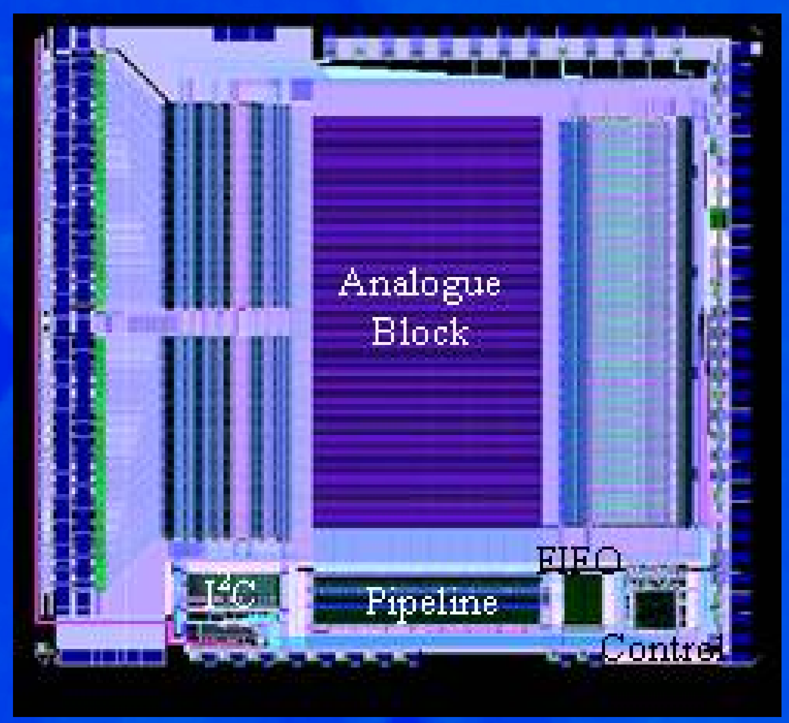
“Large” scale production

✓ Relatively large number of project in production, for quantities between 50 and 450 wafers (200mm size)



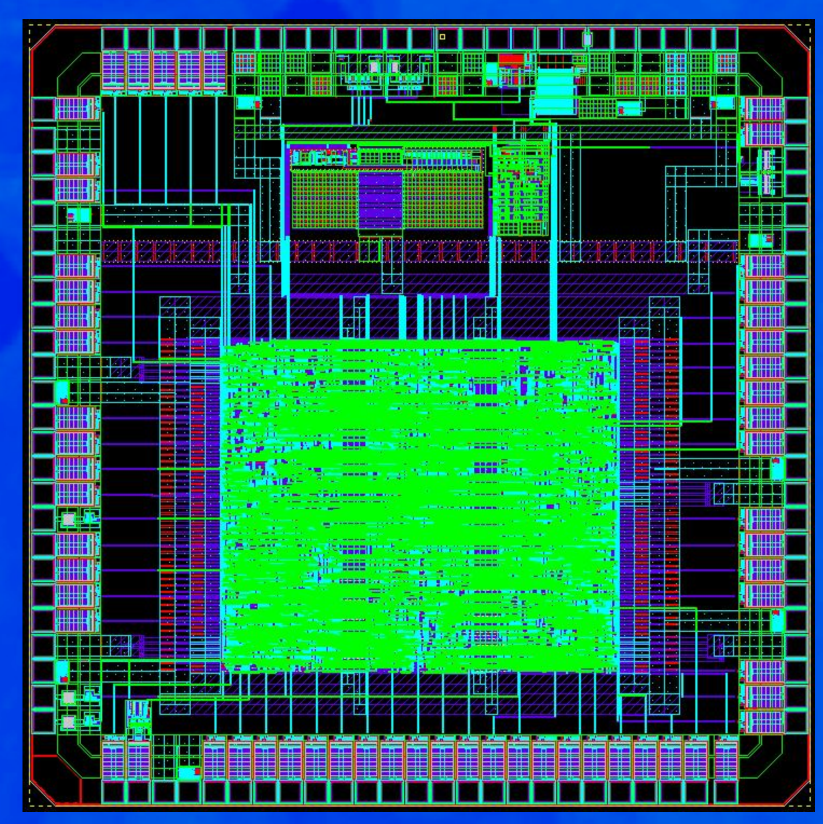
ASICs examples (1)

- ✓ APV25: readout of Silicon tracker detector of the CMS experiment
- ✓ 128 channels, analog output
- ✓ Irradiation performed:
  - X-rays up to 10 Mrad (qualification during production, 90 samples), and 100 Mrad (1 sample)
  - 300 MeV/c pions up to $2x10^{14}$ p/cm^2
  - Heavy Ions up to 62 MeVcm^{2}mg^{-1}



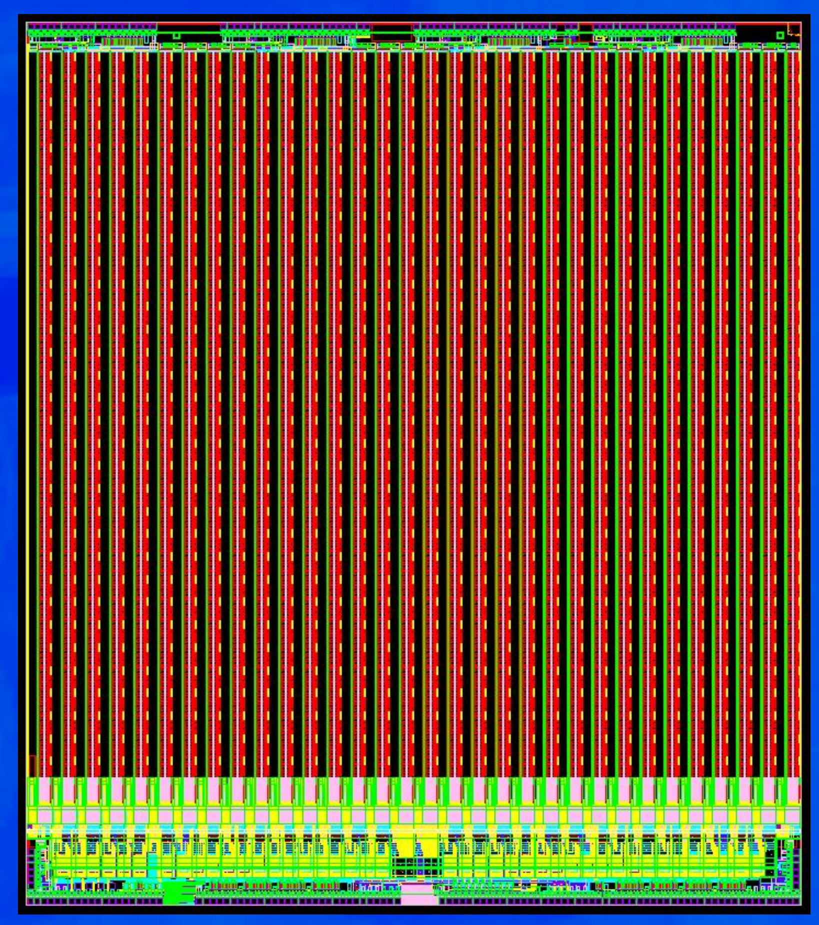
ASICs examples (2)

- ✓ GOL, optical link driver (serializer + laser driver) @ 1.6 Gbit/s
- ✓ Irradiation performed:
  - X-rays up to 10Mrad
  - 60 and 300 MeV protons up to 10^{13} p/cm^2
  - Heavy Ions up to 110 MeV cm^2 mg^{-1}



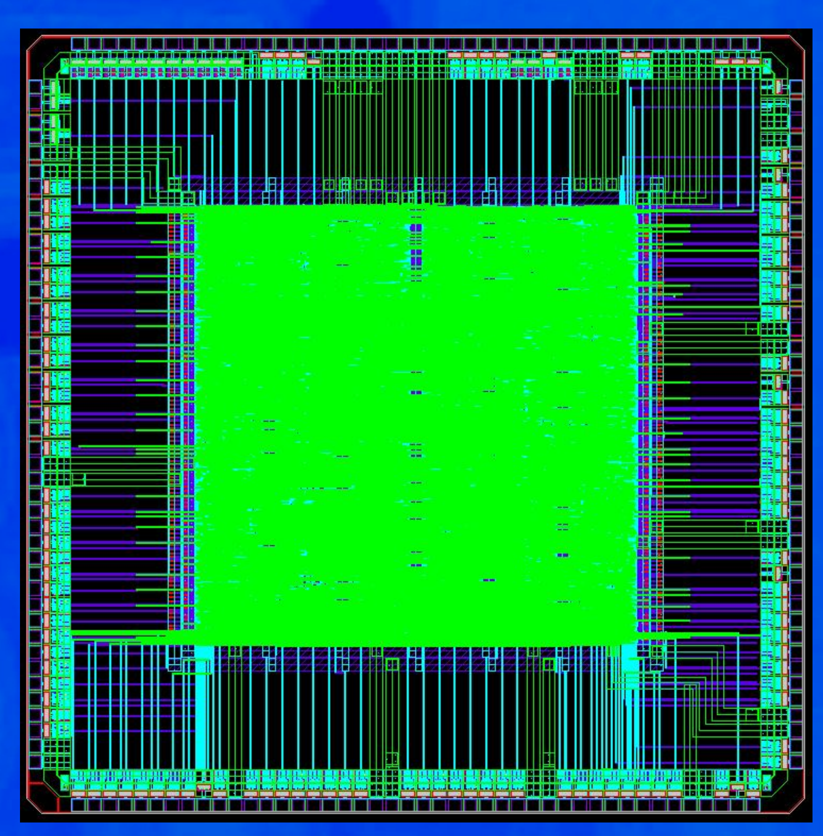
ASICs examples (3)

- ✓ Alice Pixel1, readout of silicon pixel detector of the ALICE experiment
- ✓ 2.1cm^2, 8000 analog channels, 13M transistors
- ✓ Irradiation performed:
  - X-rays up to 30 Mrad
  - 60 MeV protons up to 6.4x10^{12} p/cm^2
  - 450 GeV/c protons up to 9x10^{14} p/cm^2 in target area (prototype of the ASIC)
  - Heavy Ions up to 110 MeVcm^{2}mg^{-1}
  - 150 GeV pions (100 hours)



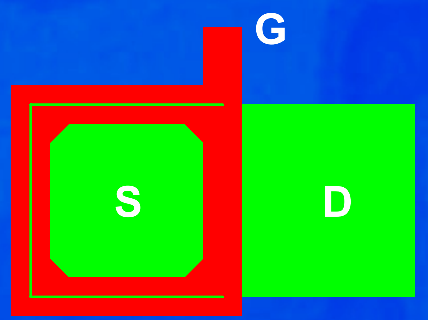
ASICs examples (4)

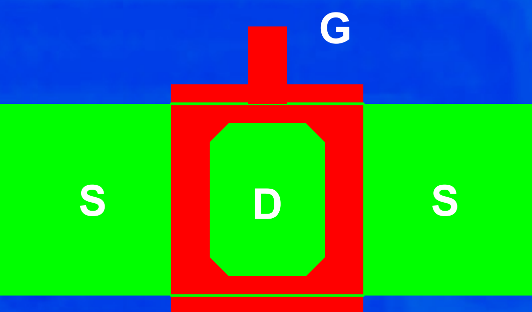
- ✓ CCU, control chip for the CMS tracker detector (fully digital chip, 120kgates)
- ✓ Irradiation performed:
  - X-rays up to 10 Mrad
  - 300 MeV protons up to $3x10^{13}$ p/cm^2



Other edgeless designs

✓ Other "edgeless" transistor designs are possible !

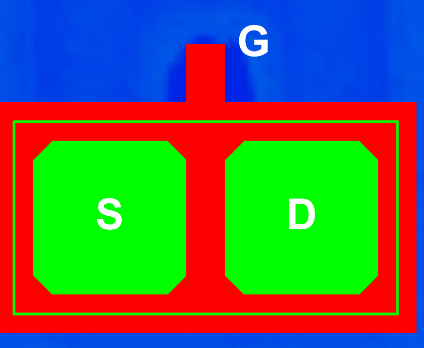


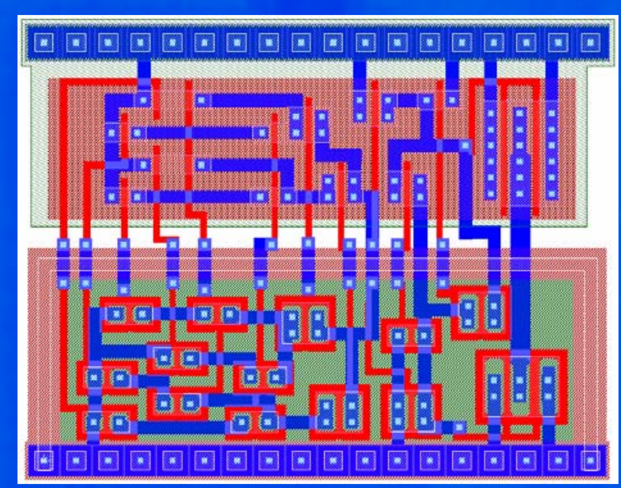


from D.Mavis, MRC

Ringed Source

Ringed Interdigitated





Butterfly

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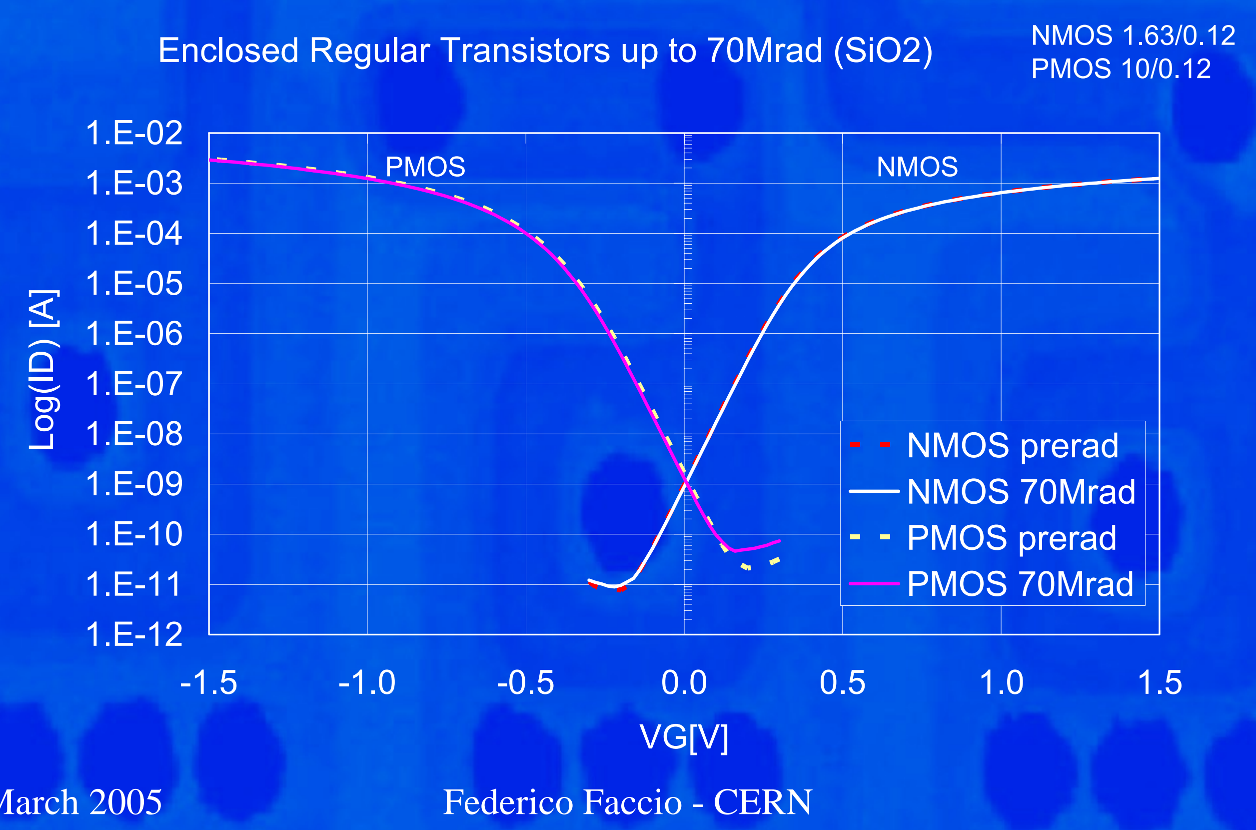
Trends in 130nm node

- ✓ Exploring more advanced CMOS technologies: 130nm node
- ✓ Similar technologies from 2 vendors have been selected and measured (at the transistor level)
- ✓ Results are very comparable between the two vendors

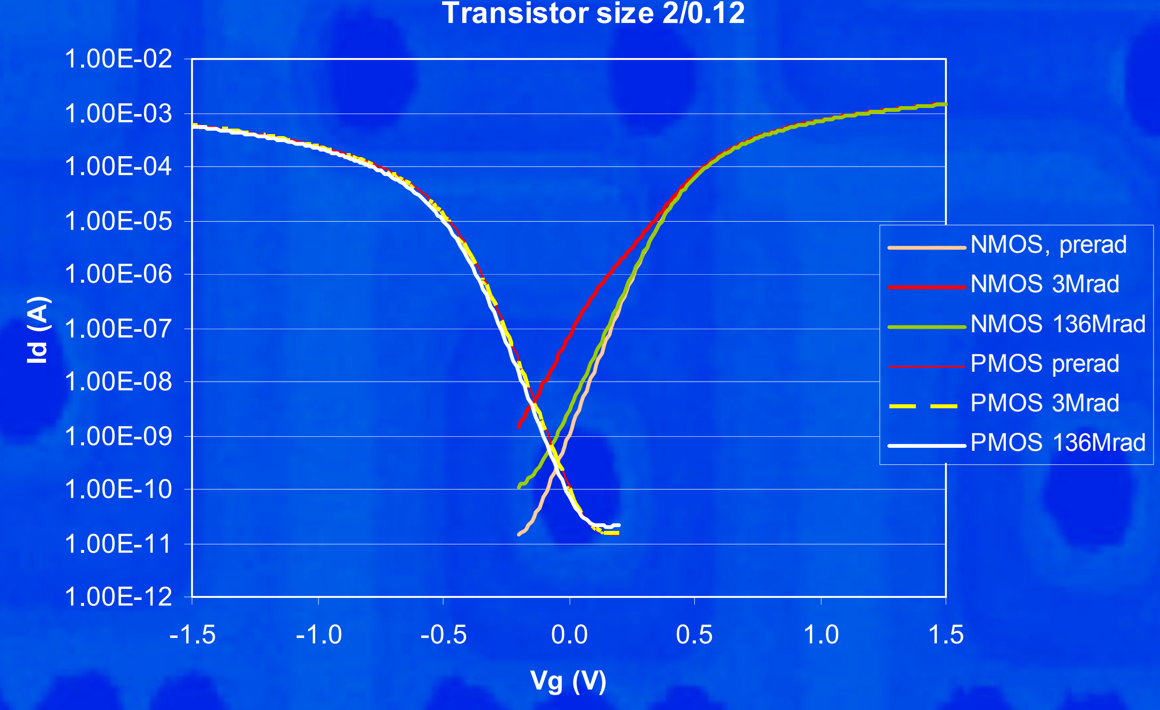
130nm: enclosed transistors

- ✓ All TID irradiations with X-rays
- ✓ Negligible degradation for all thin-oxide enclosed transistors (NMOS and PMOS), for all parameters



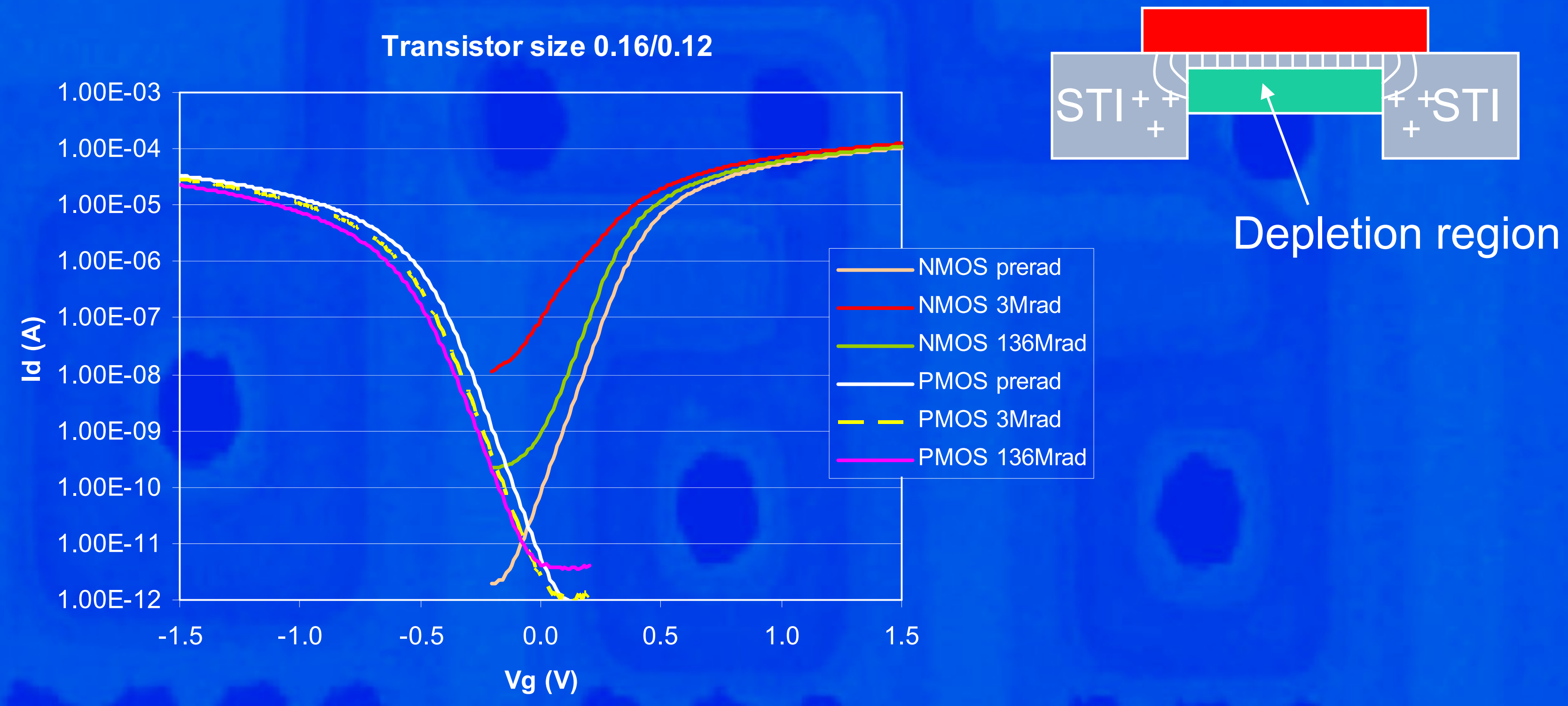
130nm: wide linear FETs

- ✓ Width larger than about 1μm
- ✓ Comparable to enclosed above threshold
- ✓ NMOS: edge effect well visible in subthreshold!
- ✓ Magnitude of effect can change with hardware “vintage”!



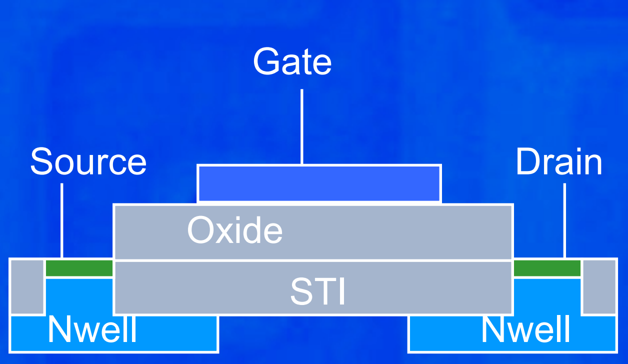
130nm: narrow linear FETs

- ✓ Effects increase for smaller W
- ✓ Strong edge effect: Narrow Channel Effect
- ✓ All transistor types affected



130nm: FOXFETs

- ✓ Transistors on Field Oxide
- ✓ PC or M1 "gate"
- ✓ N+ diffusion or Nwell Source & Drain
- ✓ Nwell-Nwell has the largest current



FoxFET NWell 200/0.92

I (A): 1.00E-03, 1.00E-04, 1.00E-05, 1.00E-06, 1.00E-07, 1.00E-08, 1.00E-09, 1.00E-10, 1.00E-11, 1.00E-12, 1.00E-13

Vg (V): 0.00E+00, 2.00E+00, 4.00E+00, 6.00E+00, 8.00E+00, 1.00E+01

Legend: prerad, 1Mrad, 136Mrad

130nm: summary

- ✓ Enclosed transistors are very good, as expected (very thin gate oxide)
- ✓ Standard linear transistors are not too bad, and can possibly be used as such for some applications (careful to narrow channel effect!)
- ✓ From FOXFETs, lateral isolation could be a problem, at least it can increase the power consumption
- ✓ Globally, TID tolerance is better than in older technologies, even for standard layout designs

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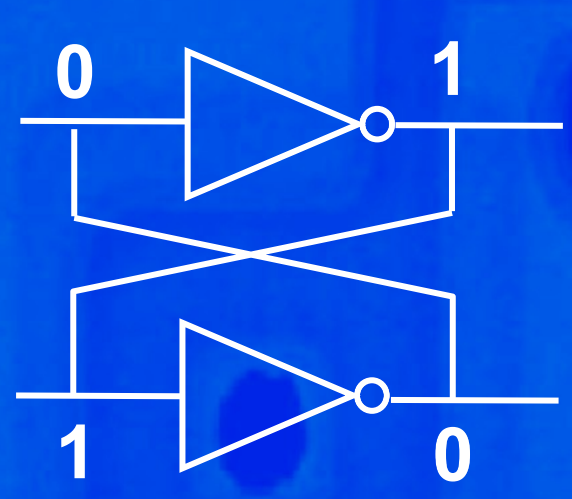
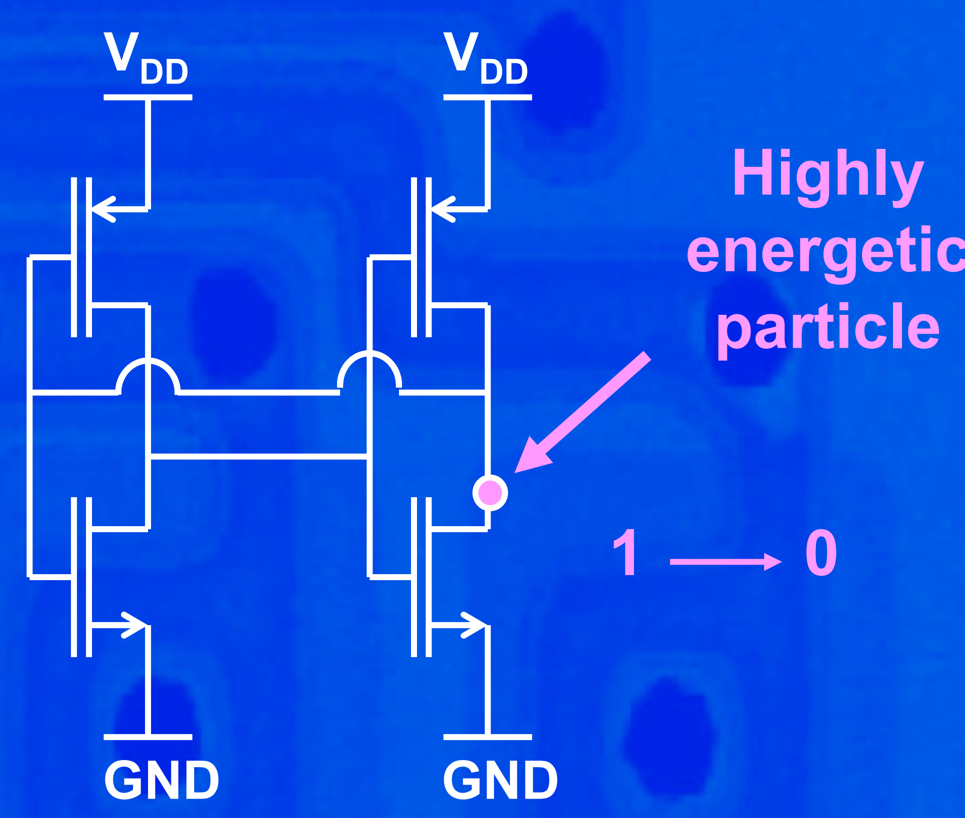
SEU (Single Event Upset)

Static RAM cell





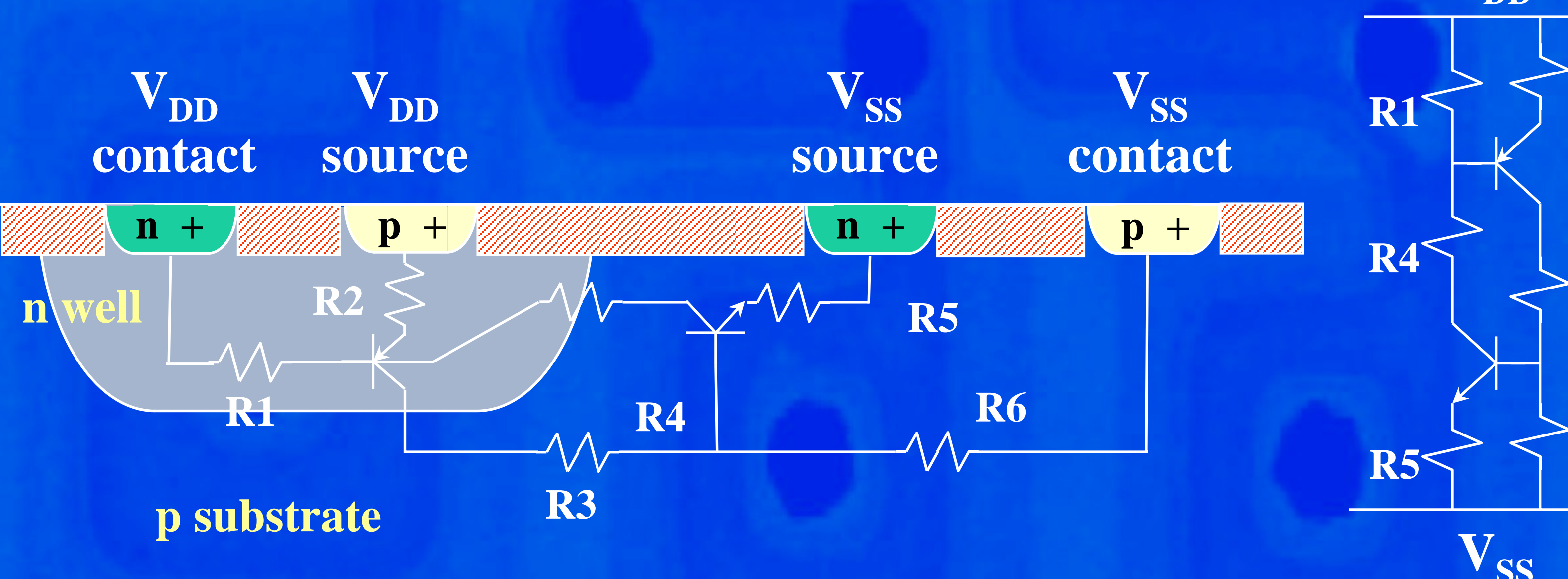
Sensitive Volume SV

Critical Energy E_{crit}

Single Event Latchup (SEL)

Electrical latchup might be initiated by electrical transients on input/output lines, elevated T or improper sequencing of power supply biases. These modes are normally addressed by the manufacturer.

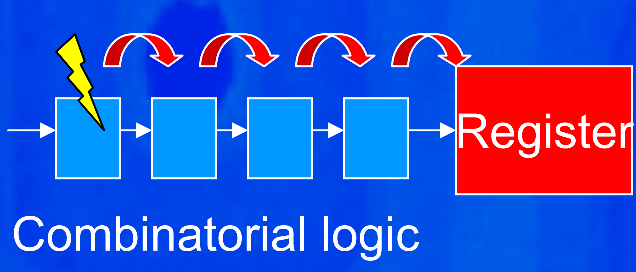
Latchup can be initiated by ionizing particles (SEL)

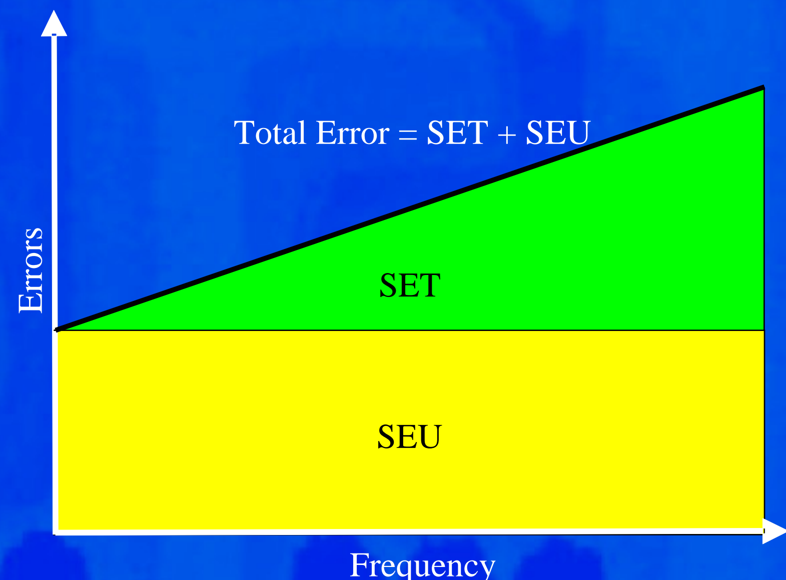


A.H. Johnston et al., IEEE TNS, Apr. 1996

“Digital” Single Event Transient

- ✓ Particle hit in combinatorial logic: with modern fast technologies, the induced pulse can propagate through the logic until it is possibly latched in a register
- ✓ Latching probability proportional to clock frequency
- ✓ Linear behaviour with clock frequency is observed





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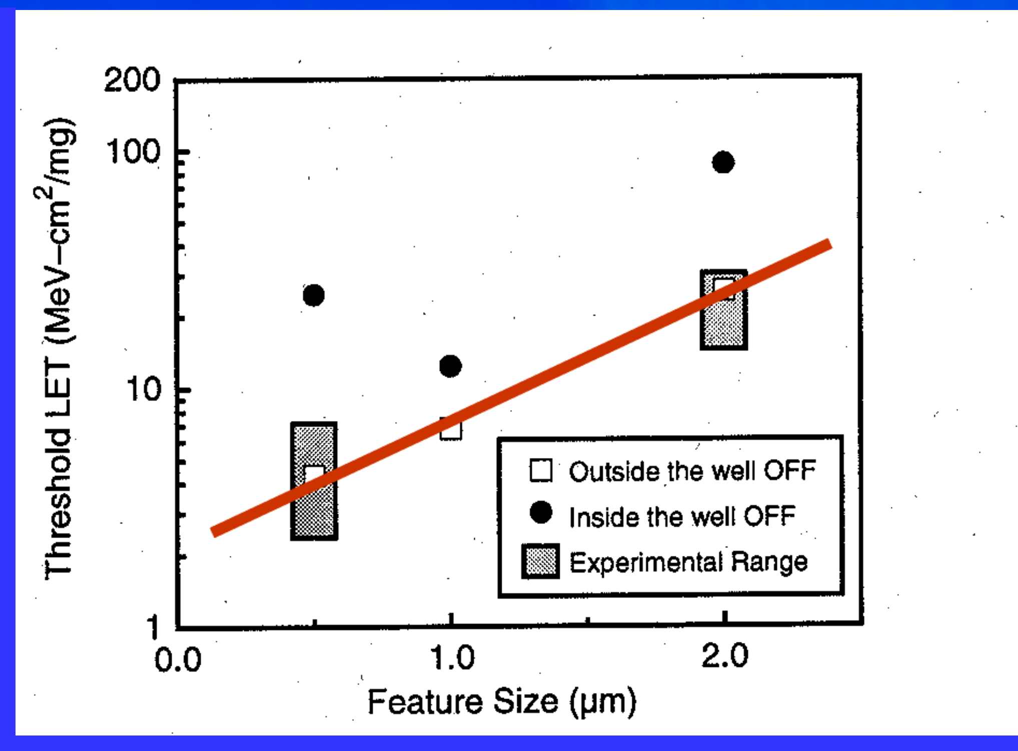
SEU and scaling: forecast

- V_{DD} reduced
- Node C reduced
- New mechanisms for SEU



P.E. Dodd et al., IEEE TNS, Dec. 1996

From the above, it looks like the SEU problem worsens with scaling

SEU and scaling: reality

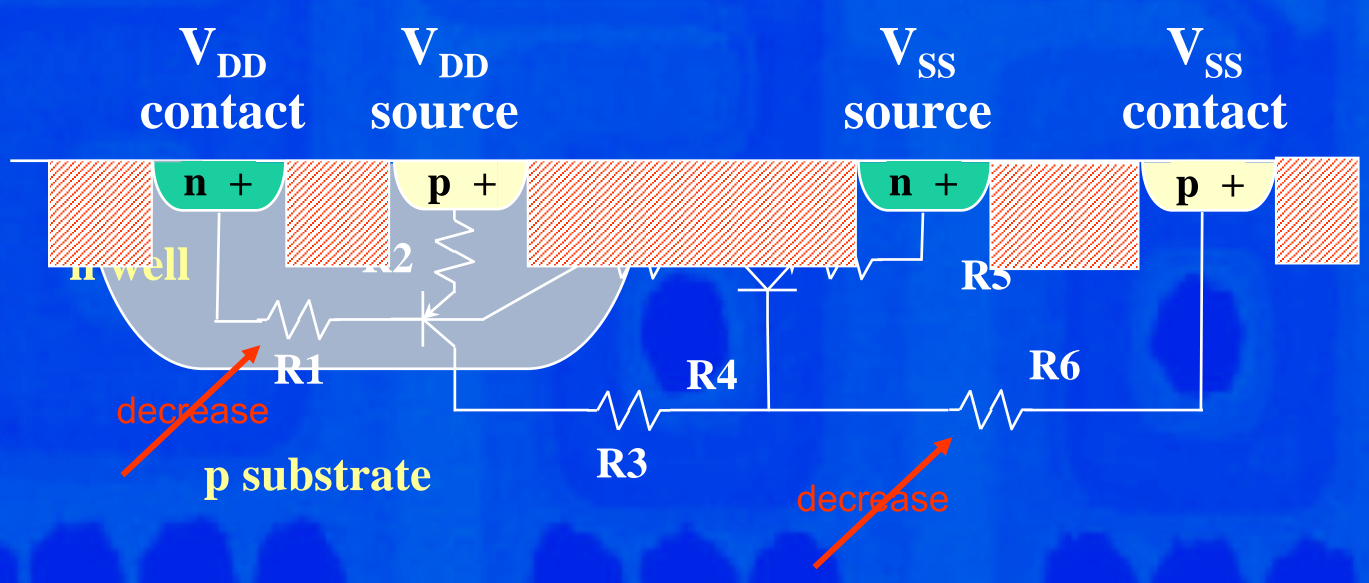
- ✓ All sources agree: DRAM sensitivity has been scaling down (cell area scaling has outpaced the decrease in stored charge).
- ✓ Picture somewhat less clear for SRAMs
- ✓ P.Hazuka et al (work funded by Intel) developed a model to predict SER scaling with Lg. The results suggest that the per-bit sensitivity decreases –at least- linearly with Lg
- ✓ Overall: FIT/MB decreases, but FIT/chip increases

- ✓ Not only Vdd and node capacitance have to be taken into account: sensitive area and charge collection efficiency are also important and change with technology generation!

SEL and scaling

- ✓ Retrograde wells
- ✓ Trench isolation
- ✓ V_{DD} reduced

All these issues help in preventing SEL, but they might not be always effective



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    - SEL
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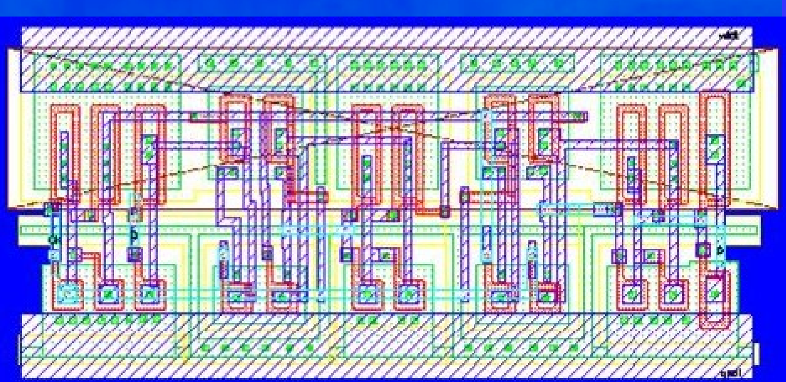
Solutions: SEU

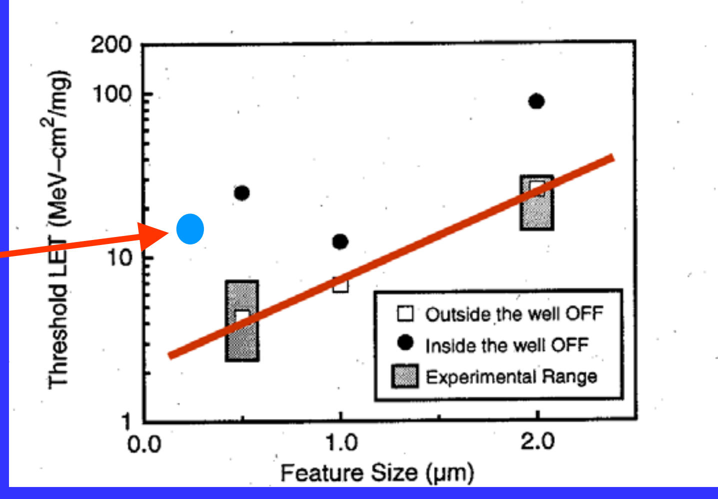
- ✓ Technology level: epitaxial substrates, SOI,…
- ✓ Cell design: SEU-tolerant FFs or memories
- ✓ Redundancy
  - Triple Modular Redundancy (TMR): triplication and voting
  - Encoding (EDAC)
- ✓ Always to be considered at system level

Cell design (1)

✓ Increase the critical charge by increasing the node capacitance:

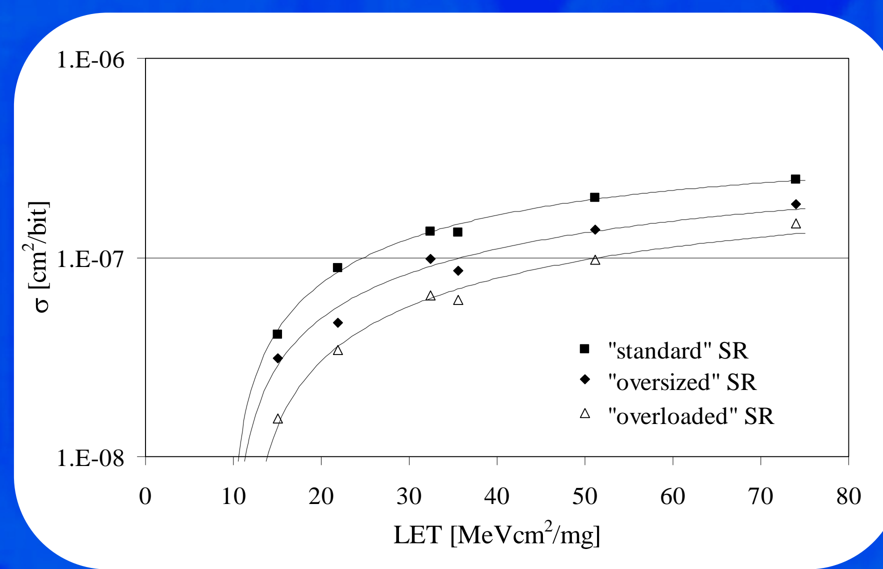
- Design larger transistors – also more driving strength





Cell design (2)

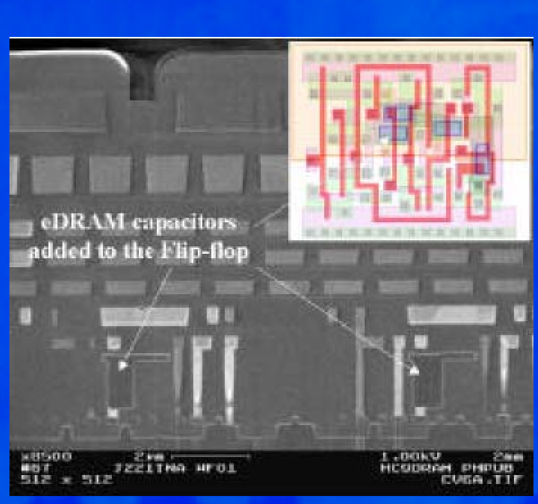
- ✓ Increase the critical charge by increasing the node capacitance:
  - Add “extra” capacitors
    - Metal/metal to avoid loosing space

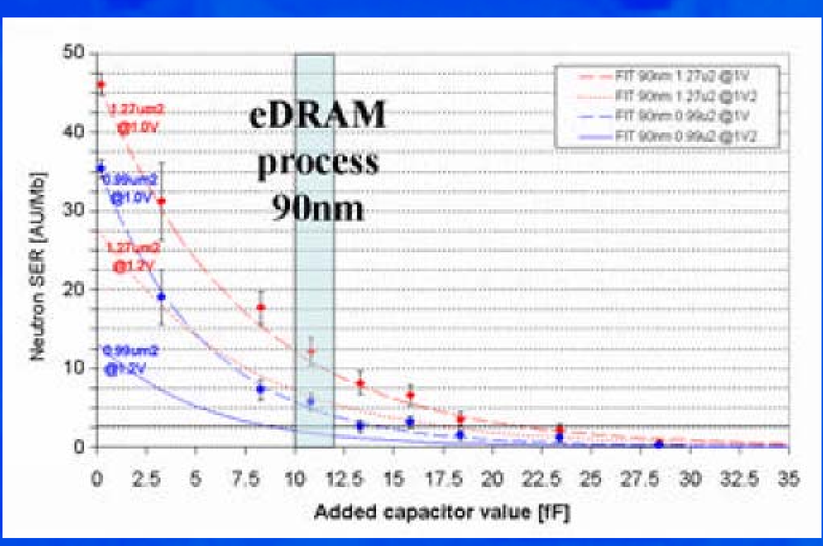


Upset rates in proton environment:
- twofold decrease for the “oversized”
- tenfold decrease for the “overloaded”

Cell design (3)

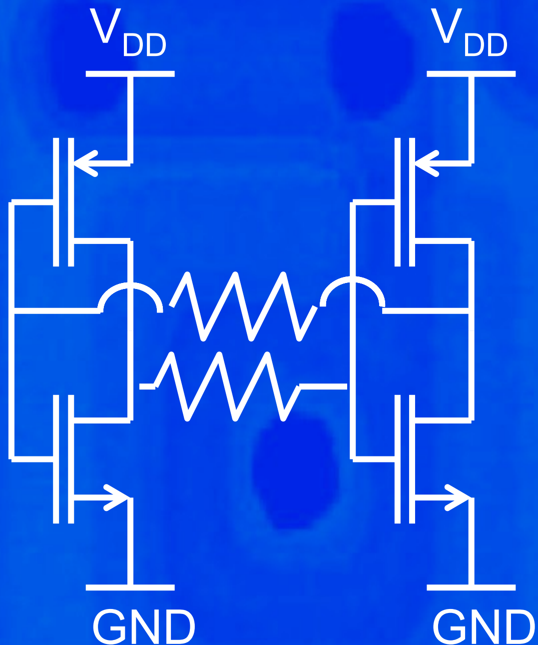
- ✓ Increase the critical charge by increasing the node capacitance:
  - Add “extra” capacitors
    - Special technology options





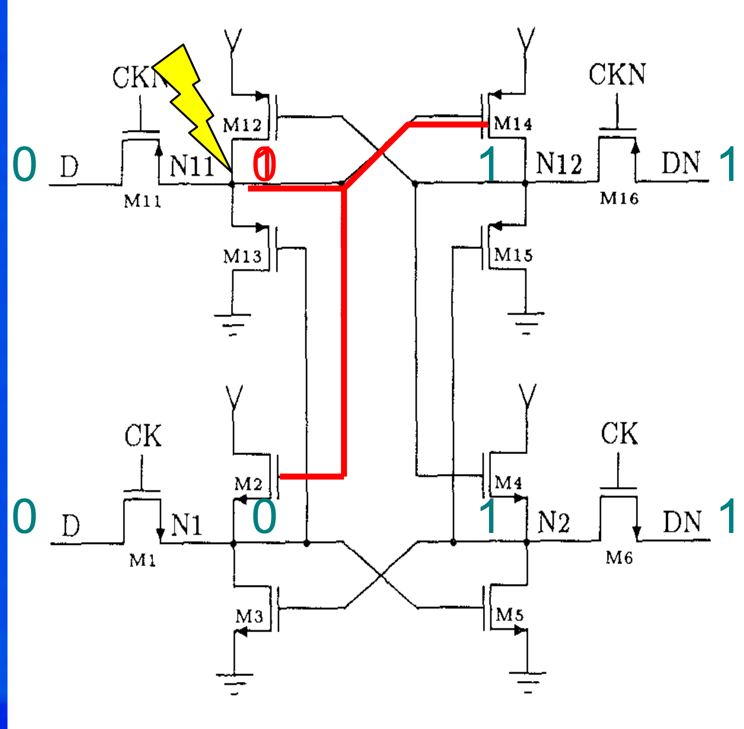
Cell design (4)

- ✓ Use special cell architectures
  - SRAM cell with added resistors, delaying the propagation of the perturbation, so allowing the cell to recover its correct state



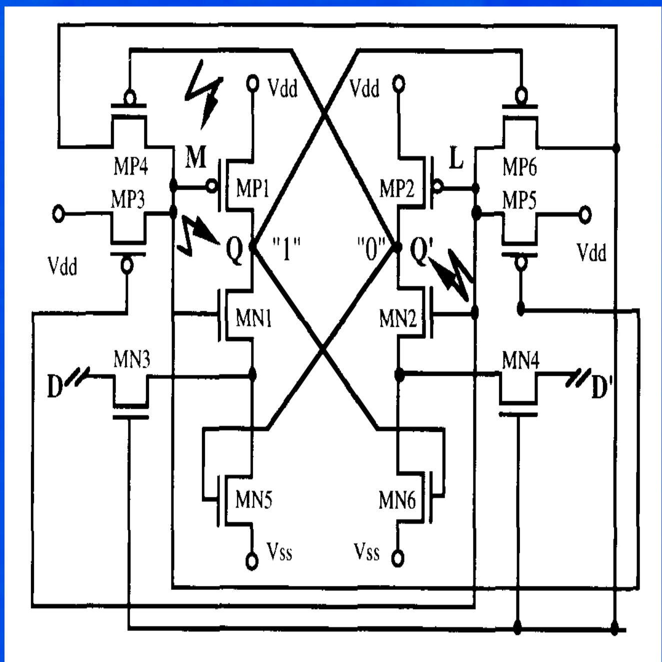
Cell design (5)

- ✓ Use special cell architectures
  - Whitaker SRAM cell
  - It uses the fact that n+ diffusions (NMOS) can only be induced to change state from 1 to 0, and p+ from 0 to 1



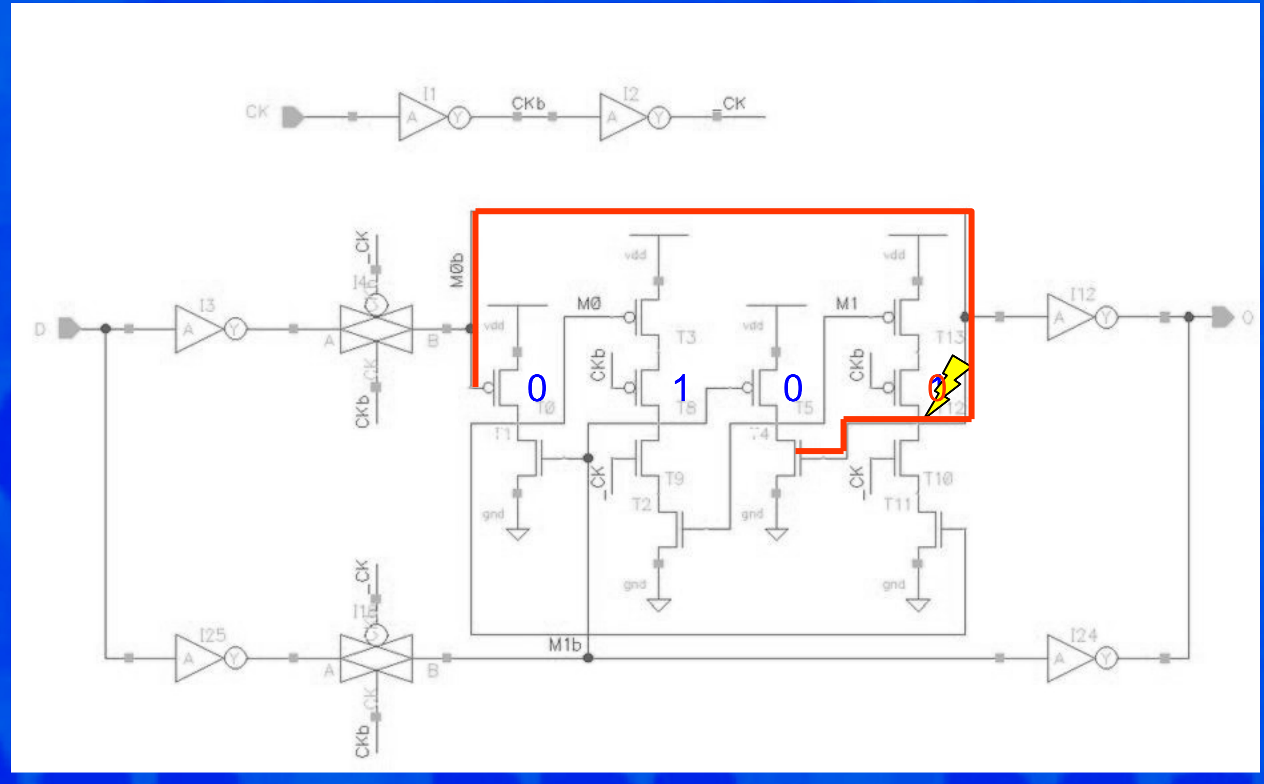
Cell design (6)

- ✓ Use special cell architectures
  - HIT (Heavy Ion Tolerant) cell



Cell design (7)

- ✓ DICE (Dual Interlock Cell)
- ✓ Dual Interlock ensures SEU protection against hit on one node
- ✓ Writing in the cell requires access to 2 nodes



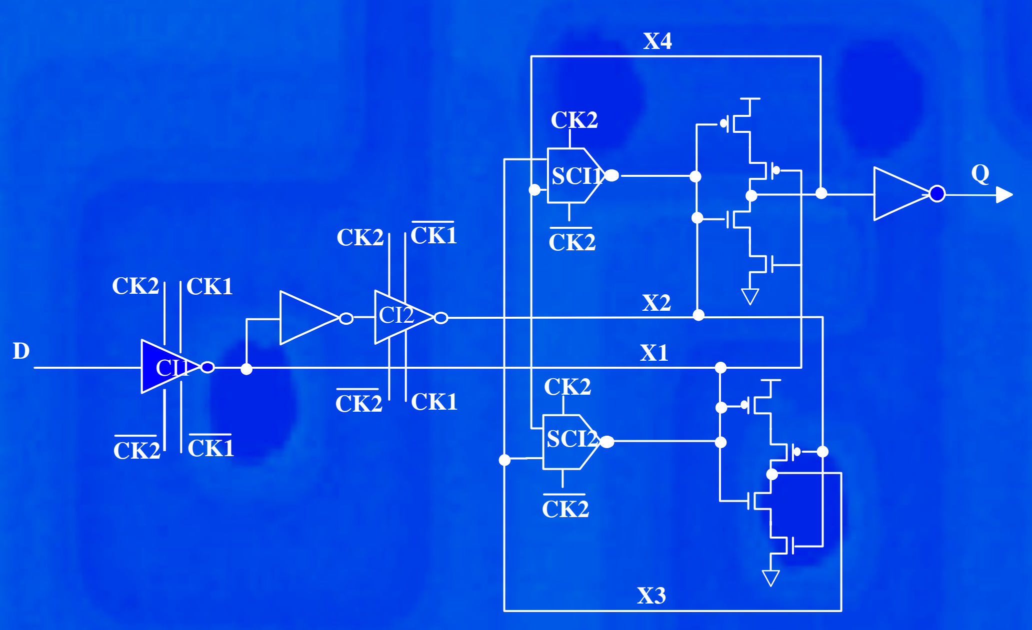
Cell design (8)

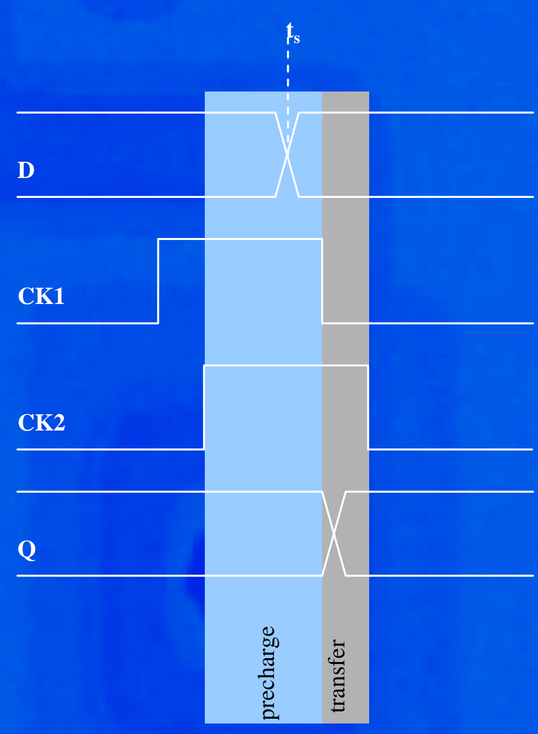
- ✓ DICE cell weakness:
  - Recovery time needed after SEU
    - Output glitch
    - A rising edge of the clock during recovery time can store wrong data in the following pipeline stage
  - Local clock buffers
  - Charge collection by multiple nodes is not negligible! (in 90nm technology, just 10x SEU rate improvement)

Cell design (9)

✓ Use special cell architectures

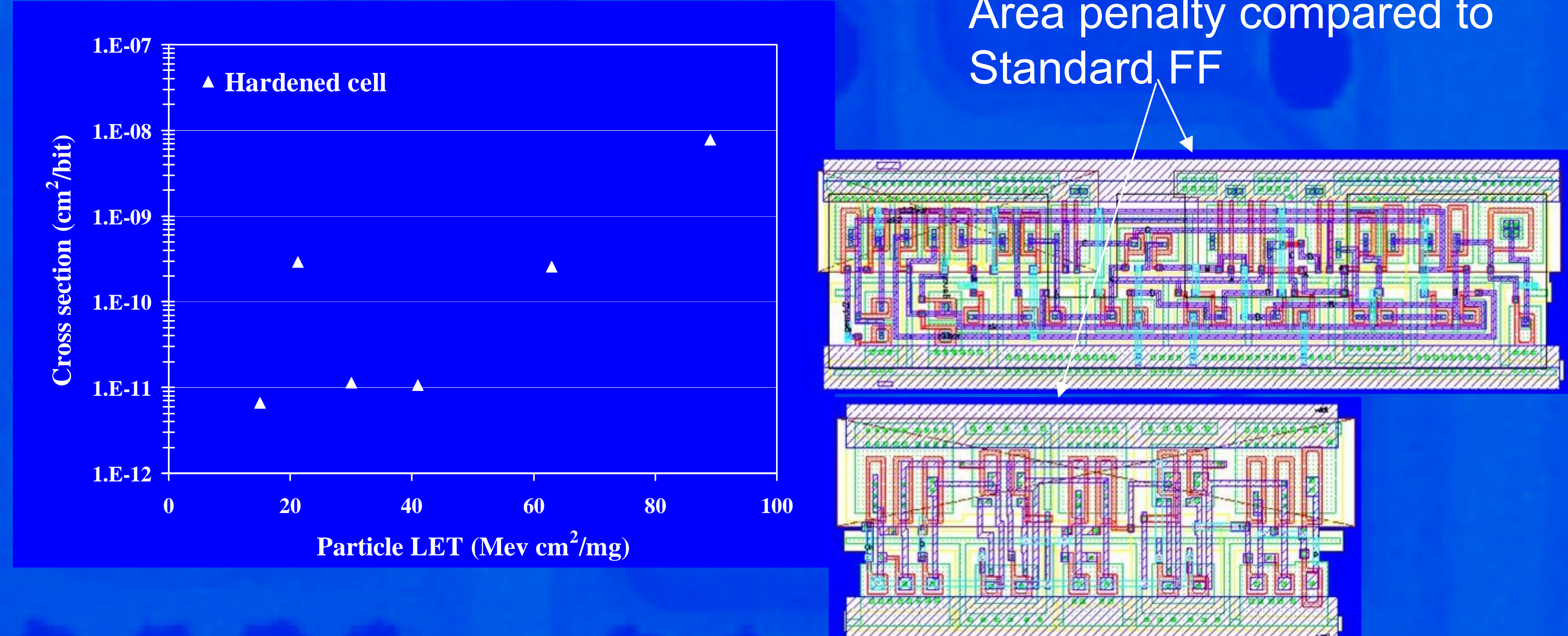
- Modified DICE cell





Cell design (10)

- ✓ Use special cell architectures
  - Modified DICE cell (as storage element, unclocked)

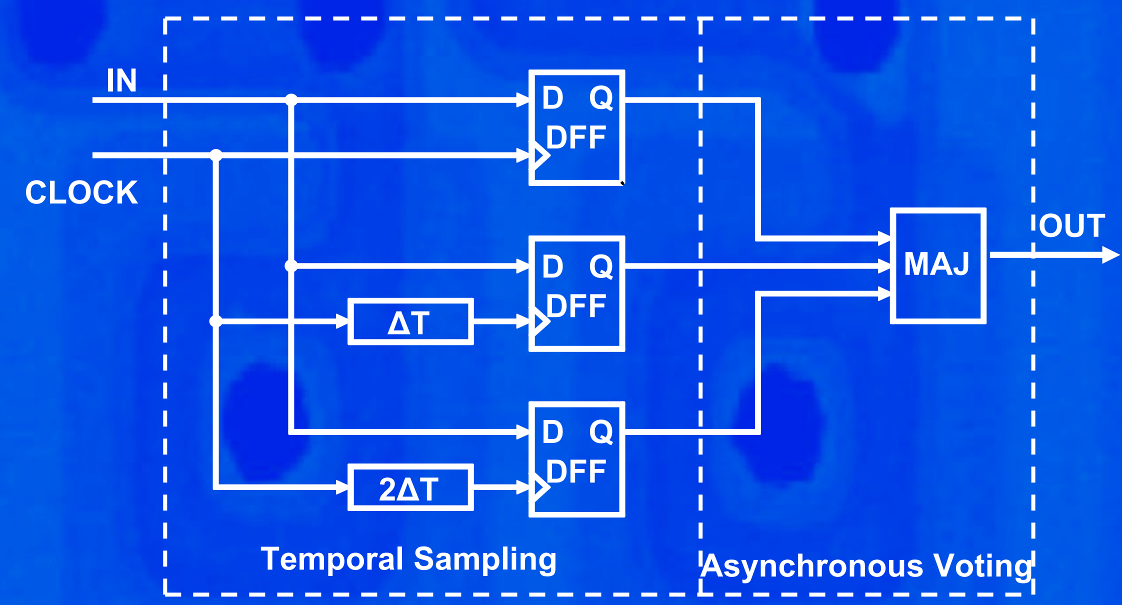


Cell design (11)

✓ Use special cell architectures

- Temporal sampling with internal clock delays (after Mavis) effective against digital SET

• Transient can only be captured by 1 latch
• Sensitive to transients on clock line
• Many variations to this concept exist (one can delay data instead of clock, for instance)

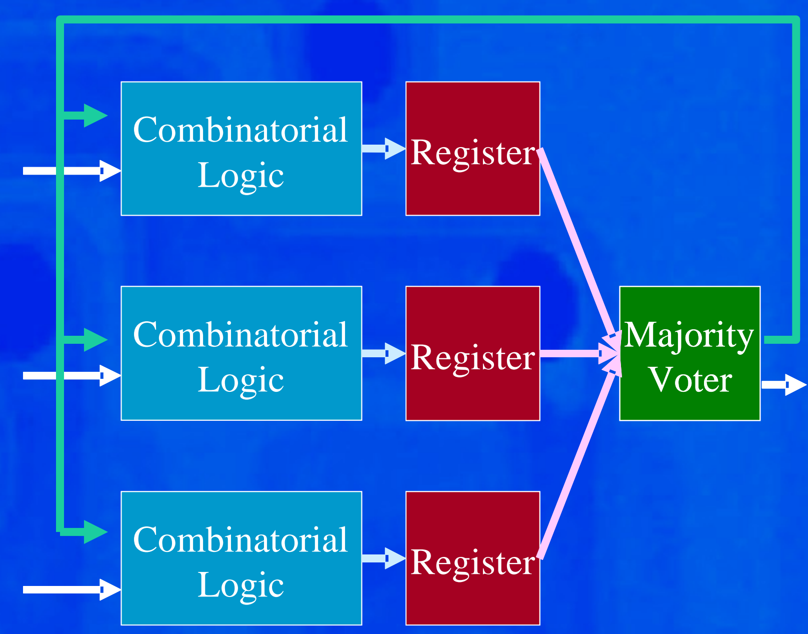


Solutions: SEU

- ✓ Technology level: epitaxial substrates, SOI,…
- ✓ Cell design: SEU-tolerant FFs or memories
- ✓ Redundancy
  - Triple Modular Redundancy (TMR): triplication and voting
  - Encoding (EDAC)
- ✓ Always to be considered at system level

Redundancy: TMR (1)

- ✓ Triplication with 1 voter

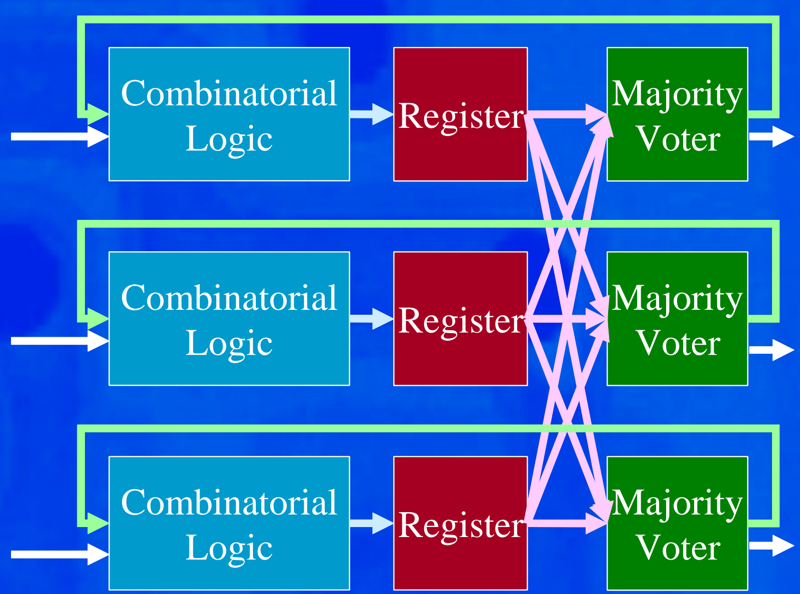


- The state machine is instantiated 3 times, with 1 voter
- An SEU can corrupt the output of one of the blocks, but majority voting restores the correct state
- An error in the voter instead corrupts the state!

Redundancy: TMR (2)

- ✓ Triplication with 3 voters

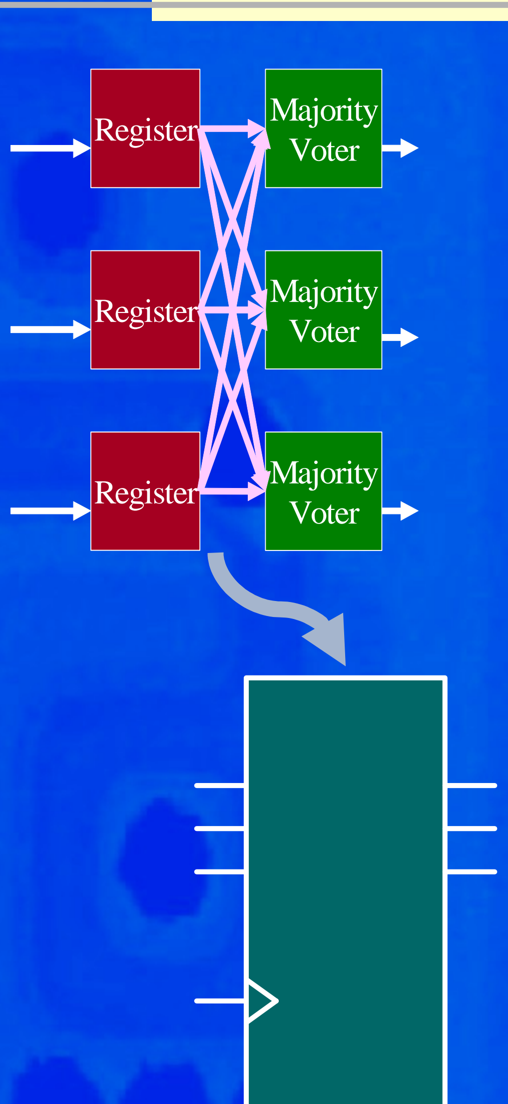
- ✓ The state machine is instantiated 3 times, with 3 voters
- ✓ An SEU can corrupt the output of one of the blocks, but majority voting restores the correct state
- ✓ An error in one of the voters is also restored



Redundancy: TMR (3)

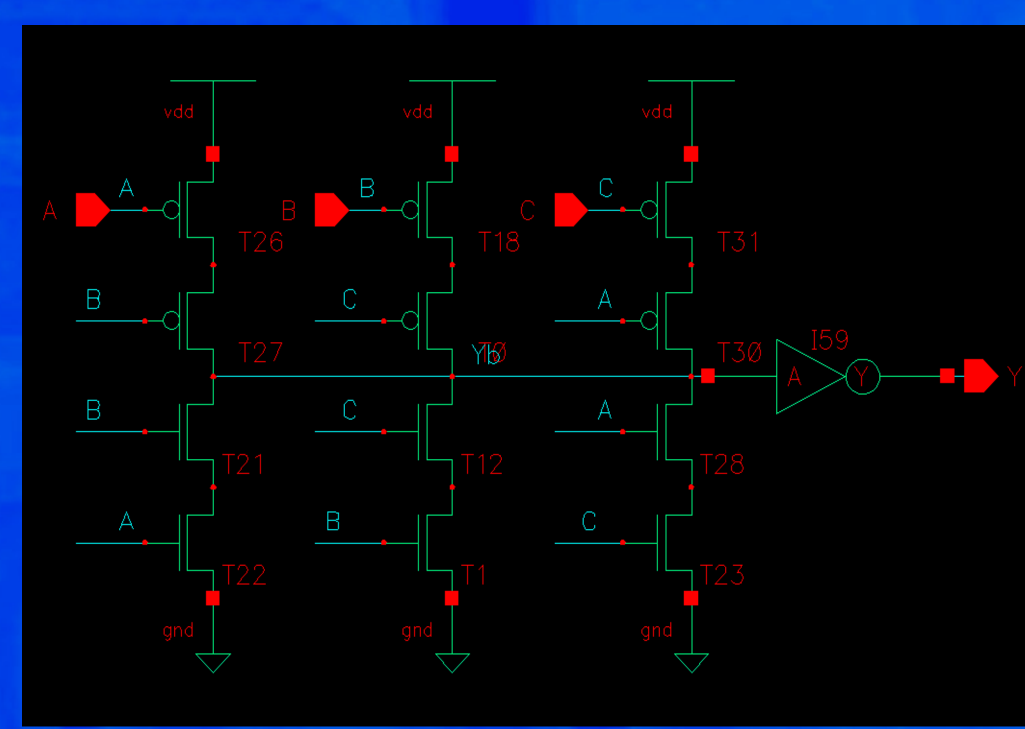
- ✓ Integrating the registering/voting part of TMR state machines in one single cell (G.Cervelli-CERN/MIC)

- ✓ 3 data inputs
- ✓ 3 data outputs



Redundancy: TMR (4)

- ✓ Integrating the register/voting in one single cell: the schematic



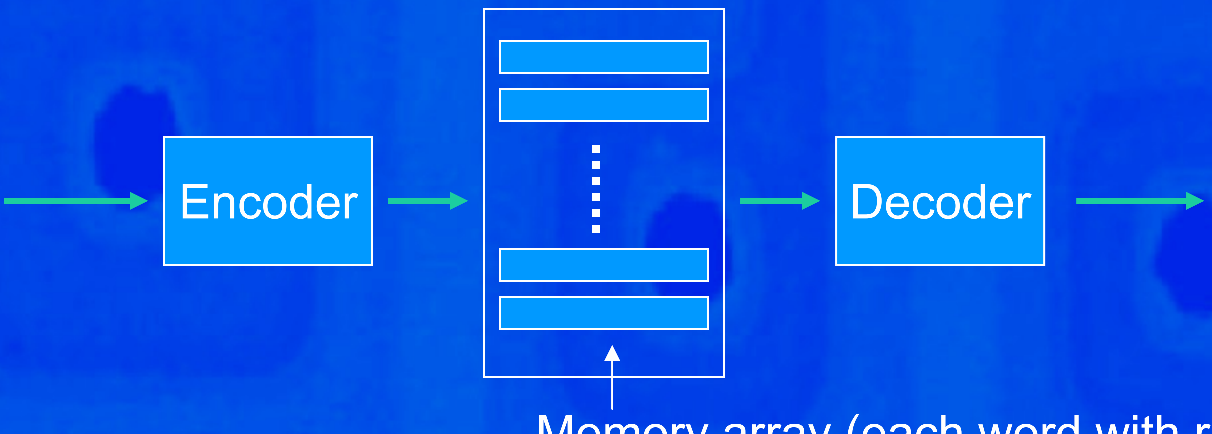
- ✓ Very compact layout
- ✓ 14 transistors
  - Better than XOR+MUX style
- ✓ Fast
  - 2 logic levels only
  - Possible to save the inverter

Solutions: SEU

- ✓ Technology level: epitaxial substrates, SOI,…
- ✓ Cell design: SEU-tolerant FFs or memories
- ✓ Redundancy
  - Triple Modular Redundancy (TMR): triplication and voting
  - Encoding (EDAC)
- ✓ Always to be considered at system level

Redundancy: encoding (1)

- ✓ Adding redundant information (bits) and encoding-decoding
  - Used for data transmission and for memories
  - Requires complex encoding-decoding logic
  - Several different codes can be used (Hamming, Reed-Solomon, BCH, etc.)



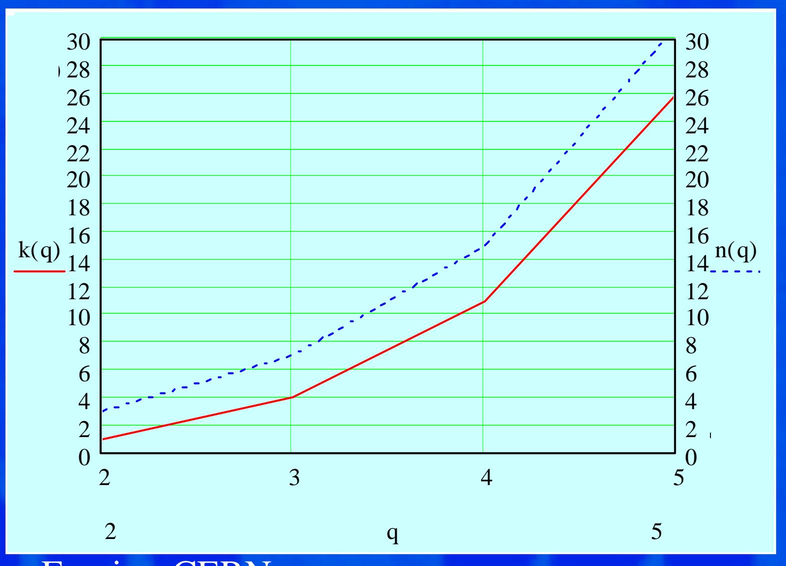
Redundancy: encoding (2)

✓ Example: Hamming encoding (1950)

k = number of message bits
q = number of check (parity) bits
n = number of word bits

Minimum distance between words = 3
⇒All valid words in the code differ AT LEAST by 3 bits
⇒It can be used for single error correction, double error detection

$n = k+q \qquad n \leq 2^q-1$



Redundancy: encoding (3)

✓ Example: Hamming encoding (1950)

Example of encoding for k = 8 q = 4 n = 12

Encode in a way requiring “as easy as possible” encoding/decoding logic

1. Check bits in powers of 2 positions in the word (position 1,2,4,8)
2. Other word bits are the message bits
3. Each check bit computes the parity for some of the word bits:
   - Position 1: check 1 bit, skip 1 bit, etc. (bits 1,3,5,7,9,11)
   - Position 2: check 2 bits, skip 2 bits, etc. (bits 2,3,6,7,10,11)
   - Position 4: check 4 bits, skip 4 bits, etc. (bits 4,5,6,7,12)
   - Position 8: check 8 bits, skip 8 bits, etc. (bits 8,9,10,11,12)

Word to encode: 10101010

word	1	1	1	1	0	1	0	0	1	0	1	0
position	1	2	3	4	5	6	7	8	9	10	11	12

Redundancy: encoding (4)

✓ Example: Hamming encoding (1950)

Word to encode: 10101010

Encoded word	1	1	1	1	0	1	0	0	1	0	1	0
position	1	2	3	4	5	6	7	8	9	10	11	12
SEU changes to	1	1	1	1	0	0	0	0	1	0	1	0

Check the parity bits in the received word:

- Position 1: OK
- Position 2: wrong
- Position 4: wrong
- Position 8: OK

The position of wrong bit is the sum of the wrong positions, that is Position 6!

Outline

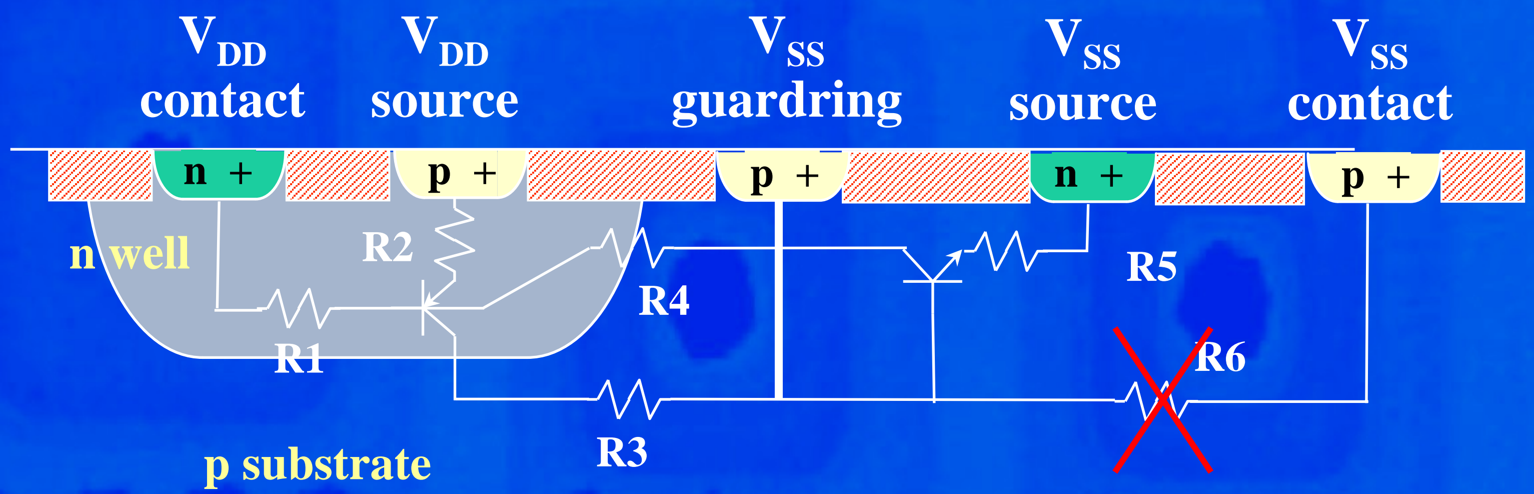
- ✓ Foreword: CMOS technologies
- ✓ TID: Total Ionizing Dose
  - Effects (reminder)
  - Solutions
  - Trends in state-of-the-art technologies
- ✓ SEEs: Single Event Effects
  - Effects (reminder)
  - SEEs and scaling
  - Solutions
    - SEU
    - SEL
- ✓ Conclusion

Reducing SEL sensitivity

The best solution is to decrease the gain of the parasitic pnpn structure. Technological and layout solution can help in that respect:

Technological => use of epitaxial substrates and retrograde wells
=> use of trench instead of junction isolation

Layout => increase the distance between complementary devices
=> use guardrings
=> use lots of substrate and well contacts



Conclusion

- ✓ Design of radiation-tolerant ASICs is possible, using commercial-grade CMOS technologies, and achieving tolerance to high TID levels
- ✓ SEU rates can be decreased with proper engineering (study of environment, introduction of tolerant cells, redundancy, encoding, etc.) and should always be considered at the system level

Further reading

- ✓ General material on radiation effects:
  - The best source is the “archive of Radiation Effects Short Course Notebooks, 1980-2002” collecting the courses given at the IEEE NSREC conference (CD sold by IEEE)
- ✓ On Enclosed Transistor Layout:
  - Ph.D. thesis describing results in 0.25μm technology:
  - G.Anelli, “Conception et caractérisation de circuits intégrés résistants aux radiations pour les détecteurs de particules du LHC en technologies CMOS submicroniques profondes“, Ph.D. Thesis at the Politechnic School of Grenoble (INPG), France, December 2000, availeble on the web at the URL: http://rd49.web.cern.ch/RD49/RD49Docs/anelli/these.html
  - Paper containing all references on the work done at CERN on this subject: F.Faccio, “Radiation Issues in the new generation of high energy physics experiments”, Int. Journal of High Speed Electronics and Systems, Vol.14, No.2 (2004) 379-399
- ✓ On SEU-tolerant Cells:
  - Increased capacitance:
    - F.Faccio et al., “Single Event Effects in Static and Dynamic Registers in a 0.25mm CMOS Technology”, IEEE Trans. Nucl. Science, Vol.46, No.6, pp.1434-1439, December 1999
    - F.Faccio et al., “SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25mm CMOS technology for applications in the LHC”, in the proceedings of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, September 20-24, 1999, pp.571-575 (CERN 99-09, CERN/LHCC/99-33, 29 October 1999)
    - P.Roche, F.Jacquet, C.Caillat, J.P.Schoellkopf, "An Alpha Immune and Ultra Low Neutron SER High Density SRAM", proceedings of *IRPS 2004*, pp671-672, April 2004
  - Special SEU-tolerant cells:
    - R.Velazco et al., “2 CMOS Memory Cells Suitable for the Design of SEU-Tolerant VLSI Circuits”, IEEE Trans. Nucl. Science, Vol.41, No.6, p.2229, December 1994
    - T.Calin et al., “Upset Hardened Memory Design for Submicron CMOS Technology”, IEEE Trans. Nucl. Science, Vol.43, No.6, p.2874, December 1996
    - M.N.Liu et al., “Low power SEU immune CMOS memory circuits”, IEEE Trans. Nucl. Science, Vol.39, No.6, p.1679, December 1992
    - J.Canaris, S.Whitaker, “Circuit techniques for the radiation environment of Space”, IEEE 1995 Custom Integrated Circuits Conference, p.77
    - P.Eaton, D.Mavis et al., “Single Event Transient Pulsewidth Measurements Using a Variable Temporal Latch Technique”, IEEE Trans. Nucl. Science, Vol.51, no.6, p.3365, December 2004
- ✓ On TMR and encoding:
  - Paper comparing techniques and containing references, to be used as a starting research point: S.Niranjan, J.F.Frenzel, “A comparison of Fault-Tolerant State Machine Architectures for Space-Borne Electronics”, IEEE Trans. On Reliability, Vol.45, No1, p.109, March 1996