Ionizing Radiation Effects on Advanced CMOS Technologies

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Reliability and Radiation Effects on Advanced CMOS Technologies
What is the impact of CMOS technology evolution on the radiation sensitivity of modern digital integrated circuits?

As we explore this issue, we will investigate in more details the basic mechanisms underlying the radiation response of CMOS circuits.
CMOS Scaling
- Feature Size
- New Materials and Architectures
- Frequency

Total Ionizing Dose
- Basic Mechanisms
- Impact of Scaling
- New Phenomena

Single Event Effects
- Single Event Upsets
- Single Event Transients
The MOSFET

How to make it faster?

Until early 2000’s

- Scaling!

Afterwards

- Scaling and…
- New materials
- New device architectures

Intel 4004 featuring 10-μm MOSFETs

www.intel.com/museum

The MOSFET

How to make it faster?

- Until early 2000’s
  - Scaling!
- Afterwards
  - Scaling and…
  - New materials
  - New device architectures

Core 2 Duo transistor
Intel 45-nm node, featuring strained silicon, high-k gate oxide, and metal gate

*M. Bohr, ISSCC 2009*
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Scaling Factor</th>
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<td>Feature Size $t_{ox}, L, W$</td>
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Scaling of operating voltage has actually been slower than feature size reduction.
Moore's Law

- Exponential decrease of the feature size with time
- Exponential increase in transistor count

M. Bohr, ISSCC 2009

Transistors

- High-k gate oxide $\Rightarrow$
  - $\uparrow$ channel control
  - $\downarrow$ leakage
- Strained Silicon $\Rightarrow$
  - $\uparrow$ drive current
- Silicides
  - $\downarrow$ series resistance

Back-end

- Low-k inter-metal layers
  - $\downarrow$ stray capacitance
- Copper vs Aluminum
  - $\downarrow$ series resistance

www.intel.com/research
### Periodic Table of Elements

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*Materials < 1990s*

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Device Architecture

- Silicon On Insulator (SOI)
  - Partially Depleted
  - Fully Depleted
  - Double Gate
  - FinFETs

- Several Advantages
  - Reduced Capacitance
  - Improved Electrostatics
  \[ \Rightarrow \text{Better Short Channel Effects} \]

Bulk MOSFET
Device Architecture

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    ⇒ Better Short Channel Effects

Partially Depleted SOI MOSFET
Device Architecture

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Fully Depleted SOI MOSFET
Device Architecture

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Double Gate SOI MOSFET

Device Architecture

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  - Fully Depleted
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  - FinFETs

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  - Reduced Capacitance
  - Improved Electrostatics
    \( \Rightarrow \) Better Short Channel Effects

FinFET
Until a few years ago, increasing frequency was the focus. Now, due to power dissipation constraints, parallelism (multi-core CPU) has become the major front.
Parametric shifts in transistors parameters due to the build-up of trapped positive charge and interface states caused by several low-LET particles striking a chip

Total Ionizing Dose affects dielectric layers (e.g., gate oxide, isolation oxides)
- Radiation strikes generating **e-h pairs**
- A large part of the e-h pairs **recombine**
- Surviving electrons are quickly swept out of the oxide
- Surviving holes slowly transport in the opposite direction
Holes hop through shallow defects and release Hydrogen
Holes get trapped close to the interface
Hydrogen generates interface traps
A large part of the initial e-h pairs recombine immediately after generation.

- Electric field $\uparrow \Rightarrow$ Charge Yield $\uparrow$
- LET $\uparrow \Rightarrow$ Charge Yield $\downarrow$

Cross section of oxide traps depends on the electric field

Worst-case bias conditions depend on charge yield and oxide-trap dependence on electric field

Interface trap generation occurs over time, after radiation exposure, due to holes and Hydrogen transport to the interface.

Bias conditions play a fundamental role.

Interface-States vs Dose Rate

- No true dose-rate dependence
- Given equal time from the irradiation, the same amount of interface state and trapped charge will occur, regardless of dose rate

\[ \Delta V_{it} (V) \]

\[ 100 \text{ krad(SiO}_2\text{)} \]

- Cs-137, 0.05 rad(SiO\text{)}\text{/s}
- Cs-137, 0.165 rad(SiO\text{)}\text{/s}
- x-ray, 52 rad(SiO\text{)}\text{/s}
- x-ray, 5550 rad(SiO\text{)}\text{/s}
- LINAC, 2 pulses, 6x10^9 rad(SiO\text{)}\text{/s}

Hole Trapping vs Time

- Trapped charge changes over time
- No dose-rate effects

Neutralization of trapped holes due
- Tunneling
- Thermal Emission

Annealing of interface traps does not occur at room temperature

Simple model for charge trapping dependence on oxide thickness:

$$\Delta V_t = \frac{Q_{ot}}{C_{ox}} = k \cdot t_{ox}^2$$

The thinner the oxide, the smaller the degradation.

Actually, things go even better for ultra-thin oxides (< 10 nm)…
Rapidly decreasing charge trapping and interface state formation in ultra-thin oxides

Saks and Ancona, 1986
Gate Leakage Current

- Fowler-Nordheim tunneling
- Direct tunneling
- Leakage is a limit to scaling

\[ J_g [\text{A/cm}^2] \]

\[ V_g [\text{V}] \]

D.J. Frank et al., Proc. IEEE, 2001
Fowler-Nordheim Tunneling

Electron tunneling through a triangular barrier

\[ J_{FN} = A \cdot E_{ox}^2 \cdot \exp \left( -\frac{B}{E_{ox}} \right) \]

where

\[ A = \frac{q^3 \cdot m_o}{16\pi^2 \cdot \hbar \cdot m_{ox} \cdot \phi_S} \]

\[ B = \frac{4 \cdot \sqrt{2} \cdot m_{ox} \cdot \phi_S^{3/2}}{3 \cdot \hbar \cdot q} \]

**Direct Tunneling**

Electron tunneling through a trapezoidal barrier

\[ B = \frac{4 \cdot \sqrt{2 \cdot m_{ox} \cdot \phi_S^{3/2}}}{3 \cdot h \cdot q} \]

\[ A = \frac{q^3 \cdot m_o}{16\pi^2 \cdot h \cdot m_{ox} \cdot \phi_S} \]

\[ J_D = \frac{A \cdot E_{ox}^2}{(1 - \sqrt{\phi_S - q \cdot E_{ox} \cdot t_{ox}})^2} \cdot \exp \left[ -\frac{B}{E_{ox}} \cdot \frac{\phi_S^{3/2} - (\phi_S - q \cdot E_{ox} \cdot t_{ox})^{3/2}}{\phi_S^{3/2}} \right] \]

Wentzel-Kramers-Brillouin (WKB) approximation
Radiation Induced Leakage Current

- When $t_{ox}<7$ nm, irradiation induces leakage current at low fields.
- Radiation Induced Leakage Current (RILC)
- True DC conduction
- Not depending on radiation LET
Radiation induced defects: electron neutral traps

Conduction mechanism: inelastic electron Trap Assisted Tunneling (TAT)

Modeled by WKB or other methods

Oxide field dependent

Most effective RILC defects at $\approx t_{ox}/2$

Generation mechanism correlated to the trapped positive charge
Defect characteristics:
- 1.3 eV below oxide Ec
- Density proportional to dose
- Independent of radiation LET (for low LET)

L. Larcher et al., IEEE-TNS, 1999
Floating Gate Memories

- Electrons stored in the FG
  \[ \rightarrow V_{TH} \text{ grows} \]

- Writing (Flash):
  - Channel Hot Electron tunnelling

- Erasing (Flash):
  - Fowler-Nordheim tunnelling

Main reliability issues:
- Endurance (W/R/E cycles)
- Data retention

Long-term Effects

- Large tails after heavy ions irradiation
- Number of bits in tail does not depend on ion LET (only on fluence)
- $\Delta V_{TH}$ strongly depends on ion LET
- Only hit cells are considered in next experiments

- Only hit FGs were programmed
- After only 30min a clear tail appears...
- …which increases more and more with time

RILC (Radiation Induced Leakage Current)

What’s going on?

- Ion generates a plasma of electrons and holes

Floating gate (electrons stored)

Ion track

- holes
- electrons

Substrate

Larcher et al, T-NS, 2003
Cellere et al, T-NS, 2005
What’s going on?

- Ion generates a plasma of electrons and holes
- Prompt columnar recombination
What’s going on?

- Ion generates a plasma of electrons and holes
- Prompt columnar recombination
- Followed/accompanied by generation of oxide defects

Floating gate (electrons stored)

Tunnel Oxide

Oxide defects

Substrate

Larcher et al, T-NS, 2003
Cellere et al, T-NS, 2005
What’s going on?
- Ion generates a plasma of electrons and holes
- Prompt columnar recombination
- Followed/accompanied by generation of oxide defects

Oxide defects are used by electrons to escape the FG
- multi-Trap Assisted Tunneling (m-TAT)

Larcher et al, T-NS, 2003
Cellere et al, T-NS, 2005
- How can we evaluate the current along this path?
- Consider the ion track
- Randomly generate a Gaussian distribution of defects
- Evaluate the current through each possible path (phonon-assisted)
- Then sum all the currents

\[ I = \sum I_n \]

Larcher et al, T-NS, 2003
Cellere et al, T-NS, 2005, 2006
Long-term Effects

- Symbols → average, experimental data
- Bars → variance (spread) of experimental data
- Lines → calculations

Current as low as 10^{-24}A → 1n(fA)

Larcher et al, T-NS, 2003
Once coupled with a model of the FG cell, the leakage model can be used to derive the $V_{TH}$ evolution over time.

After iodine (LET=64 MeVcm$^2$/mg) irradiation,

Symbols = exp.  
Lines = sim.

Cellere et al, T-NS, 2005
Why Nitrided Oxides?
- Improve dielectric constant
- Reduce leakage current
- Prevent boron penetration
- Better hot carrier reliability

Radiation Hardness
- Suppression of interface states, Nitrogen layer acts as a barrier for Hydrogen diffusion
- Comparable density of oxide charge-traps in SiON and SiO$_2$
High-k Gate Oxides

- Research on radiation effects in high-k oxides far less advanced than in SiO₂
- Different Band Structure
  - Smaller bandgap \( \Rightarrow \) less energy for e-h pair generation
  - Recombination, Charge Yield?
  - Pre-existing defects
  - Different barriers \( \Rightarrow \) different carrier tunneling probabilities

Thick High-k Gate Oxides

- Thicker oxides, a return to charge trapping?
- Significant number of electron traps in HfO$_2$ in addition to hole traps
- Minimal charge trapping for thin HfO$_2$ with buffer SiO$_2$ layer

Gate oxide: 1nm SiO$_2$ + 7.5nm HfO$_2$ EOT = 2.3nm


Thin High-k Gate Oxides

Thicker oxides, a return to charge trapping?

Significant number of electron traps in HfO₂ in addition to hole traps

Minimal charge trapping for thin HfO₂ with buffer SiO₂ layer

Gate oxide: 1nm SiO₂ + 3.0nm HfO₂ EOT = 1.5nm

SOI: Partially Depleted Devices

- Thick buried oxide sensitive to radiation
- Amount of charge trapping depends on SOI wafer technology (SIMOX vs wafer-bonding)
- **Parasitic Source-Drain leakage** develops in partially depleted devices
Threshold voltage shift in the parasitic back gate transistor leads to drain-source leakage

SOI: Fully Depleted Devices

- Thick buried oxide sensitive to radiation
- Amount of charge trapping depends on SOI wafer technology (SIMOX vs wafer-bonding)
- Coupling with the back gate leads to changes in the front gate transistor
Coupling means back gate $V_{th}$ shift leads to changes in front-gate $V_{th}$


$\textbf{k} = \frac{C_{ox2} C_{Si}}{C_{Si} + C_{ox2}}$
Single Event Effects

- Stochastic effects due to a single particle hitting the sensitive area of a device

- SRAM
  - Single Event Upsets (SEU)
  - Single Bit Upsets (SBU)
  - Multiple Cell Upsets (MCU)
  - Multiple Bit Upsets (MBU)

- Combinational Logic
  - Single Event Transients (SET)
Simulated heavy ion e-h track in Si

Fe ions 275 MeV
LET=24 MeV cm$^2$/mg

LET metrics in Si:

1 MeV cm$^2$/mg
6.4 \times 10^4 \text{ e-h pairs/\mu m}
10 \text{ fC/\mu m}

P. Foulliat, EWRHE 2004

Electron-Hole density (cm$^{-3}$)

Heavy ion e-h track in Si vs. CMOS minimum size

CMOS generation

- 0.35 μm
- 0.25 μm
- 0.18 μm
- 0.13 μm
- 90 nm
- 32 nm

DEDHIS Fer 275MeV
Two generations after…
Single Bit Upsets, Neutrons

- SEU/bit constant or even decreasing!
- Area effect wins over reduction in capacitance

N. Seifert, et al., IRPS 2008

Multiple Bit Upsets, Neutrons

Percentage of Multiple Bit Upsets increases (even more for other vendors)

N. Seifert, et al., IRPS 2008
MCU cluster size almost independent of technology node

The number of affected bits grows with each generation

N. Seifert, et al., IRPS 2008
Multiple Bit Upsets, Heavy Ions

Strong dependence on LET

MCU’s dominate at high LET

N. Seifert, et al., IRPS 2008

Reduction of sensitive volume (less charge collection)

Bipolar amplification may increase sensitivity

Bipolar amplification important also on bulk devices
MCUs in some bulk technologies

- occur preferentially along bitlines (inside p-wells)
- increase with increasing supply voltage (contrary to SBU)
- due to bipolar amplification ("battery" effect), increase in well potential due to particle strike affects many devices

G. Gasiot, et al., IRPS 2008
MCUs in SOI
- due to geometrical effects
- devices are separate (no common well)

G. Gasiot, et al., IRPS 2008
Memory elements aren’t the only resource sensitive to ionizing radiation, also **combinatorial logic** can be affected.

Single Event Transients (SET) can originate from particle strikes in **reverse-biased pn junctions** belonging to the combinatorial part of a circuit.

**SETs can eventually propagate** to memory elements and be **latched**.
Logical masking can block SET’s
The higher the frequency, the larger the probability of catching a transient (temporal masking)
Electrical masking…
SET: attenuated propagation

- Low LET below critical LET, attenuated propagation

\[ \text{LET} = 3 \text{ MeV-cm}^2/\text{mg} \]

- 0.18 \( \mu \)m CMOS
- \( V_{DD} = 1.62 \) V
- 10-Inverter Chain

\[ P. \text{ Dodd et al., IEEE-TNS 2004} \]
SET: non-attenuated propagation

- High LET above critical LET, non-attenuated propagation

P. Dodd et al., IEEE-TNS 2004
The higher the LET, the longer the pulse.

Complex dependence on technology.

P. Dodd et al., IEEE-TNS 2004
Critical LET for non-attenuated propagation decreases with feature size.

SOI less sensitive than bulk CMOS (shorter transients)

P. Dodd et al., IEEE-TNS 2004
SETs are expected to dominate the radiation sensitivity in future technologies, for high performance applications.

R. Baumann, IEEE-TDMR 2003
Conclusions

- Simple scaling is no longer enough to sustain the pace of Moore’s law, **new materials and device architectures** have been/will have to be introduced that may affect radiation response.

- **Gate oxide sensitivity** to TID Effects has **improved** thanks to scaling, with no major issue from high-k layers. Isolation oxide may be still a problem.

- **Radiation Induced Leakage Current** can be an issue for the reliability of Flash Memories and DRAMs.

- The presence of the **buried oxide** in SOI may be detrimental to TID sensitivity but help with SEE.

- **Multiple Cell/Bit Upsets** and **Single Event Transients** are a growing concern for digital circuits.
Many thanks to:

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- All the referenced authors

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