Single Event Effects in SRAM based FPGAs

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Introduction

• New constraints ask for the adoption of SRAM-based devices in safety-/mission-critical applications:
  – Low cost
  – Fast and cheap prototyping
  – Reconfigurability

• High reliability levels are mandatory

• Reliability analysis should start from the early design phases
Reliability issue

• SRAM-based FPGAs are particularly sensible to Single Event Upsets (SEUs):
  – Modification of a memory bit (0 $\Rightarrow$ 1, 1 $\Rightarrow$ 0)
  – Produced by energetic heavy particles

• SEUs may hit:
  – User memory bits: transient effect
  – Configuration memory: permanent effect
Proposed approach

Device Characterization
- SRAM-based FPGA device
  - Radiation Testing
    - Device Cross Section

Circuit Analysis
- Register Transfer Model
  - Fault Injection
    - Circuit Error Rate

Circuit Cross Section
Experimental

- SRAM based device:
  - Xilinx Virtex XCV300PQ240-4 FPGA
- Radiation sources:
  - Heavy ions from Tandem accelerator, Laboratori Nazionali di Legnaro, Istituto Nazionale di Fisica Nucleare, Padova, Italy
  - Linear Energy Transfer (LET) from 1.6 (88 MeV C ion) to 63 MeV/mg/cm² (256 MeV I ion)
Measured SEU/SEFI Cross Section

![Graph showing Measured SEU/SEFI Cross Section with different cross sections plotted against LET (MeV cm$^2$ / mg). The graph includes lines and markers for Configuration memory cross section, C6288_4 SEFI cross section, and B14 SEFI cross section.]
SEU Cross Section per bit

Cross Section per bit [cm$^2$/bit]

LET [MeV cm$^2$/mg]

Device cross section per bit
LUT
IO
INTERCONNECT
INTERNAL_IC
Circuit Analysis

• Exploits simulation-based fault injection targeting:
  – Transient faults in user memory
  – Permanent faults in the configuration memory
• Works on Register Transfer descriptions
• Exploits a fault model that considers:
  – Faults in Configurable Logic Blocks (CLBs)
  – Faults in Routing resources
Fault model

RT-level behavioral model

Logic synthesis

Reference RT-level structural model

Place & Route

Reference Configuration memory

Faulty RT-level structural model

Faulty Configuration memory

Analysis

Fault injection

Compare

?
Virtex XCV300 TILE matrix
SEUs in the CLB bits

• Look Up Table defect
  – Change in the implemented logic function

• MUX defect
  – Change of the connections among LUTs, Flip-flops and outputs in the CLB

• Initialisation defect
  – Change of behaviour of the internal components of the CLB
SEUs in routing resources

• Open
• Bridge
• Input antenna
• Output antenna
• Conflict
• None
• Other
Fault free circuit
Bridge
Antenna

Net_1

Net_x_i

Net_x_o

Net_2

IN_0, IN_1, IN_2, IN_3, IN_4, IN_5, IN_6, IN_7, IN_8, IN_9, IN_10, IN_11

OUT_0, OUT_1, OUT_2, OUT_3, OUT_4, OUT_5, OUT_6, OUT_7
# Frequency of SEFIs

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<tr>
<th></th>
<th>SEFIs</th>
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<tbody>
<tr>
<td></td>
<td>[#]</td>
<td>%</td>
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<tr>
<td><strong>CLB</strong></td>
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</tr>
<tr>
<td>LUT</td>
<td>36</td>
<td>7.9</td>
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<tr>
<td>MUX</td>
<td>54</td>
<td>11.9</td>
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<tr>
<td>Inizialization</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td><strong>Routing</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open</td>
<td>108</td>
<td>23.8</td>
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<tr>
<td>Bridge</td>
<td>66</td>
<td>14.5</td>
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</tr>
<tr>
<td>Output Antenna</td>
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<td>0</td>
<td></td>
</tr>
<tr>
<td>Input Antenna</td>
<td>13</td>
<td>2.8</td>
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<tr>
<td>Conflict</td>
<td>145</td>
<td>31.9</td>
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<tr>
<td>None</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Others</td>
<td>32</td>
<td>7.0</td>
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</tr>
<tr>
<td><strong>Total</strong></td>
<td>454</td>
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Conclusions

• Effective analysis of SRAM-based FPGA requires to consider faults in configuration memory
• Faults in configuration memory modify implemented circuit functionality
• New hybrid approach:
  – Radiation testing: performed once for each device, application-independent
  – Fault injection: application-dependent, exploits an ad-hoc fault simulator