Destructive Single-Event Effects in Semiconductor Devices and ICs

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***Abstract*—Developments in the field of destructive single-event effects over the last 40 years are reviewed. Single-event latchup, single-event burnout, single-event gate rupture, and single-event snap-back are discussed beginning with the first observation of each effect, its phenomenology, and the development of present day understanding of the mechanisms involved.**

I. Introduction

SINCE THE first predictions of single-event upset (SEU) in microelectronics in 1962 by Wallmark and Marcus [1], researchers and engineers who rely on space-borne systems have been concerned about the effects of cosmic rays on mission reliability. This concern was realized in 1975 when an anomaly in a spacecraft system was first attributed to the passage of an energetic heavy-ion [2]. Since that time, a long list of single-event effects in semiconductor devices and integrated circuits have been compiled. Some of these effects result in a "soft-error," one that causes no permanent damage and can be reset by applying the correct signals to the device. Other effects are not as benign and result in permanent degradation or even destruction of the device. These so-called "hard errors" are the subject of this paper.

This paper will present the development of the science of destructive single-event effects over the last four decades. Four primary areas have developed in this field based on the type of effect. These are single-event latchup (SEL), single-event burnout (SEB), single-event gate rupture (SEGR), and single-event snapback (SESB). Single hard errors (SHE), a degradation of transistor performance due to total ionizing dose deposition from a single ion strike, is beyond the scope of this review. These catastrophic failure modes can occur in many different types of semiconductor devices. For example, SEL is possible in bulk CMOS technologies or in some SOI technologies when n- and p-type devices are built into common silicon islands. It has been observed in space cosmic ray environments and terrestrial neutron accelerated tests. SEB occurs primarily in power transistors, such as power MOSFETs, bipolar transistors, and IGFETs used in space, but has also been observed in high voltage diodes in terrestrial applications. Nonvolatile memories, power MOSFET, and MOS-based digital and linear ICs have exhibited single event gate rupture. Snap-back, also known as single transistor latchup, occurs in MOS technologies in both bulk and SOI substrates. Each area is covered as a separate topic in this paper, highlighting some of the major findings that led to our current understanding of these effects and the researchers who played major roles in these developments.

For reference, the reader is referred to a detailed review of single-event effects published in 1996, covering research in these areas up to that point in time [3].

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II. Destructive Single-Event Effects

A. Latchup

Latchup is a potentially catastrophic condition where a low resistance path develops between power supply and ground on a device that remains after the triggering event is removed. When currents are sufficiently high metal traces can vaporize, bond wires can fuse open, and silicon regions can be melted due to thermal runaway. Once latched, this high current condition will continue until power is removed from the device or it fails catastrophically. While latchup is troublesome in ground-based systems and can result in low system reliability and expensive cures, it can be disastrous in space-based systems leading to system failure and often the loss of an entire mission at a significant cost.

Latchup dates back to the development of the thyristor switch first conceived by Shockley and Ebers in the early 1950s [4], [5]. The detailed principles of operation and first working device were developed by Moll in 1956 [6]. The thyristor is a multilayered *pnpn* device that can be switched from a high to low impedance state capable of handling currents on the order of 10^3 amps. It has wide application in motor controllers and in high power converter systems, among others.

As seen in Fig. 1, the IV curve for a *pnpn* device is multivalued; that is, there are two separate regions of behavior in a structure capable of latchup. The first, region I, is marked by low current at all voltages out to a maximum where electrical breakdown occurs. This is the normal operational mode for reverse biased pn junctions in ICs prior to latchup. When latchup occurs, the device transitions rapidly to a high current-low voltage state (region III) determined by the intersection of the load line and the IV characteristic. Connecting these two regions is a region of negative resistance (region II). The load line is a function of the impedance between the power supply and the device. The minimum voltage and current in latchup is defined as V_H and I_H, the holding voltage and current, respectively.

A more detailed understanding of the mechanism for latchup can be obtained by examining a cross section of a CMOS circuit [7], as shown in Fig. 2(a). In forming a p-well region for n-channel transistors electrically isolated from p-channel transistors, two parasitic bipolar devices are naturally formed.

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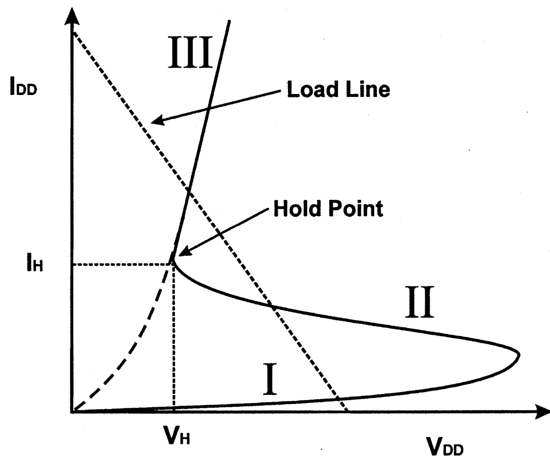

Fig. 1. IV characteristic for latchup.

The collector, base, and emitter of a vertical npn transistor are formed by the n-substrate, p-well, and n+ diffusions, respectively. Similarly, a pnp lateral transistor is formed by p+ diffusions, the n-substrate, and p-well regions. A bias network for these parasitics is formed by the spreading resistance between the base (n+ substrate contact) and emitter (p-diffusion) of the lateral pnp, and the base (p-well contact) and emitter (n-diffusion) of the vertical npn transistors. A simplified circuit diagram illustrating the interconnection of these elements is shown in Fig. 2(b).

Latchup is triggered when any source of excess carriers turns on the vertical npn or lateral pnp transistor. When this happens in the lateral pnp, for example, the collector current for the pnp feeds into the base of the npn and is amplified, causing more npn collector current, and consequently, a larger voltage drop across Rs, thereby driving the lateral pnp harder. This regeneration leads to a rapid switch from a blocking state (regions I) to a latched state (region II). Latchup can also be triggered by excess current in the p-well leading to turn on of the vertical npn. Latchup can only be sustained when the gain product of the parasitics exceeds 1, the bias network supports a forward bias at both emitters, and the load line for the power supply can provide enough current to sustain a latchup condition. For an in-depth review of the physics of electrical latchup the reader is referred to an excellent treatment of the subject by Troutman [8].

The first focus on this effect due to radiation occurred in the early 1960s when it was observed that transient radiation could trigger latchup in bipolar integrated circuits [9]–[11]. Leavy and Poll [11] attributed failures in triple- and quad-diffused ICs under high dose-rate irradiation to the triggering of *pnpn* action in these devices by radiation-induced excess photocurrents. Their analysis was confirmed by measurements, which showed that radiation-induced latchup occurred only in devices that could be electrically triggered into latchup. Gregory and Shafer [12] significantly extended this work by showing that latchup could also occur in CMOS IC technologies under exposure to transient radiation. They laid the foundation for this study in MOS based IC technologies and established the rule of thumb that the gain product $h_{FEnpn} \times h_{FEpnp}$ must be greater than one for latchup to occur. In this work, Gregory and Shafer

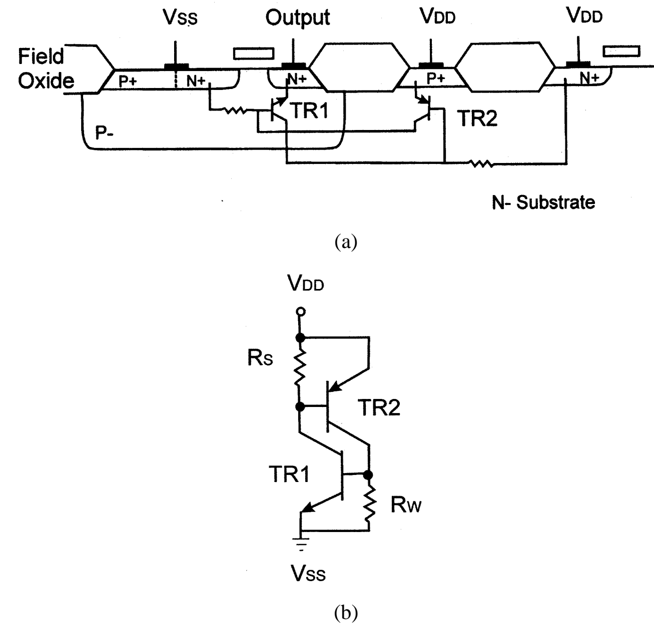

Fig. 2. Structure leading to latchup in CMOS technologies. (a) Cross section of a bulk CMOS technology on n-substrate material. (b) Equivalent circuit (after Soliman [7]).

also suggested the key process mitigation techniques that are possible, including reducing the parasitic bipolar gain, use of thin epitaxial layers on heavily doped substrates, use of n+ and p+ guard rings, and use of dielectric isolation, such as SOS or SOI, which eliminate the four-layer *pnpn* paths required for latchup. Layout techniques were also recommended to minimize spreading resistance drop in wells and the substrate. Sivo *et al.* showed a strong temperature dependence of latchup in CMOS ICs exposed to transient radiation, an effect that at the time was attributed to an increase in bipolar gain with temperature [13].

In 1979, while demonstrating that energetic heavy ions did indeed cause upset in Schottky TTL static RAM ICs of the type that had exhibited upset in space [2], Kolasinski *et al.* [14] also observed single-event latchup in 1 K- and 4 K-bit CMOS memories. This work also exposed devices at nonnormal angles of incidence relative to the direction of the ion beam as a way to explore a wide range of ion paths through the sensitive volume. Researchers were finding that upset and latchup could not be induced by protons and neutrons in state of the art devices at that time [15].

A typical latchup curve is shown in Fig. 3, which plots latchup cross section as a function of heavy-ion linear energy transfer (LET). As in the case of SEU and other single-event effects, cross section here is a measure of the area of a device that is sensitive to latchup, while LET is a measure of the energy deposited by an ion as it passes through the semiconductor material. LET has units of energy loss per unit areal density (MeV-cm^2/mg) or charge generated per unit pathlength (pC/μm).[1] An SEL curve typically rises from a threshold through a shoulder region and asymptotically approaches a saturation cross section. Unlike SEU, it is usually difficult to measure an abrupt threshold.

[1]In silicon, 100 MeV-cm^2/mg is roughly the equivalent of 1 pC/μm.

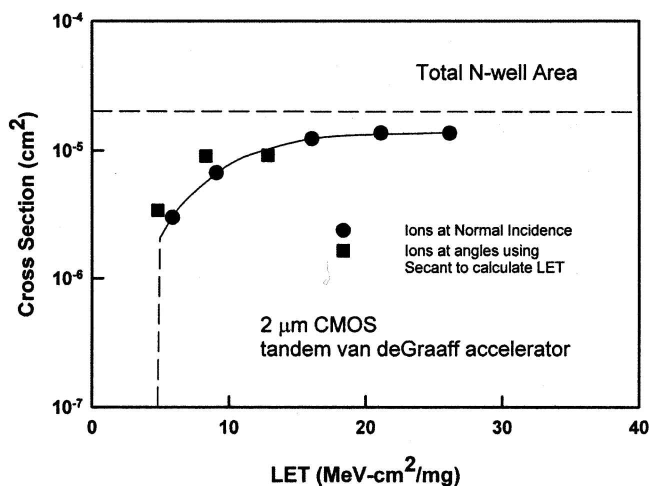

Fig. 3. Single-event upset cross section showing a threshold region, rising through a gradual shoulder to a saturation cross section. Note that for this part the saturation cross section is slightly below the total n-well area (after Johnston [17]).

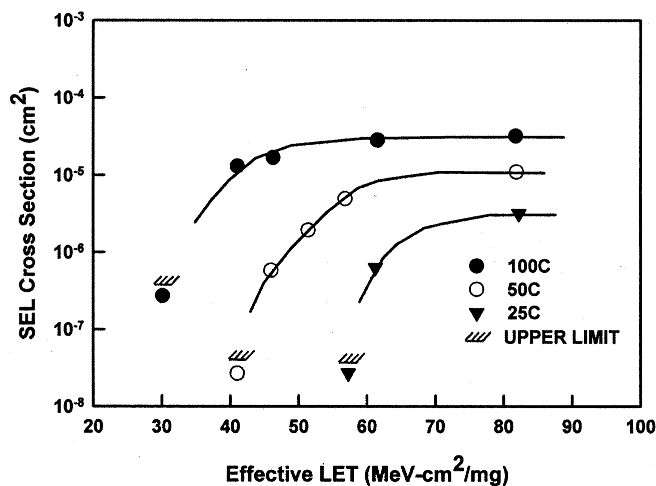

Fig. 4. Temperature dependence of SEL (after Kolasinski [14]).

Other researchers quickly confirmed the existence of SEL. In an effort to find less expensive methods to screen devices for latchup, Stephen *et al.* [16] in 1983 demonstrated that SEL could be stimulated in CMOS devices using Cf-252 fission fragments as well as energetic heavy ions, although the cross sections measured were about a factor of 10 higher with Cf-252 than with 67-MeV Kr ions. This was speculated to be due to differences in energy, and consequently LET, between the two sources. Significantly, no upsets could be attributed to alphas or fast neutrons from the Cf-252 source during these tests on 2-μm feature size devices. However, using Cf-252 as a quantitative tool has proved to be difficult due to uncertainty in LET of the fission fragments. Additional limitations in the use of Cf-252 for the study of SEL due to limited penetration range were uncovered in later work by Johnston *et al.* in 1990 [17].

As more data became available, it became apparent that there was significant variation in measurements of threshold LET and saturation cross section on like devices from one researcher to another. Saturation cross section often differed by orders of magnitude. Many of the insights into measurement variability would not emerge until the 1990s. While the latchup effect in a device is the same independent of the radiation source, the triggering mechanism for latchup by a single heavy ion is significantly different from transient radiation induced latchup. In the case of transient radiation, the entire substrate is flooded with excess carriers, so latchup can be triggered in any of a number of nodes of a complex circuit. In addition, as long as the radiation is uniform and a circuit can latchup there is no doubt that a dose rate threshold can be found that exceeds the threshold. In the former case, the ion must deposit sufficient energy in specific locations to begin the regenerative latchup process. There may be many latchup sensitive locations, and the latchup threshold may differ with the latchup path.

By the mid 1980s single particle-induced latchup was a well-established effect. Important features of latchup were yet to be resolved, however. Among these were the effects of temperature on SEL, developing modeling tools, and determining the critical factors affecting latchup sensitivity. Kolasinski *et al.* [18], in a clean study of temperature dependence, showed that increasing temperature resulted in a decrease in latchup threshold and increase in cross section with increasing temperature (Fig. 4). In addition, parts which did not latch at room temperature could easily latch-up when tested at elevated temperature. This showed the importance of testing devices at the highest use temperature during hardness assurance tests.

Rollins *et al.* [19] made the first attempt to use modern transport codes to model SEL using a two-dimensional (2-D) version of the PISCES device analysis program. This work followed earlier demonstrations of 2-D modeling of SEU in CMOS devices by Fu *et al.* [20]. Using specialized test structures, Uins *et al.*studied the effects of geometry variations on SEL sensitivity and observed that the regions most sensitive to latchup occurred between the in-well emitter and well edge. Good agreement was shown between simulations and cyclotron measurements of latchup threshold LET with light ions, but the models were not able to fit latchup threshold for ions of Ar and heavier ions. This was attributed to difficulties in correctly modeling the cylindrical strike geometry using a 2-D Cartesian code. These issues were not resolved until the advent of 3-D codes in the 1990s.

In a detailed study of latchup in CMOS ICs using heavy ions, Cf-252, and a pulsed laser, Johnston and Hughlock [17] confirmed that the threshold region for single-event latchup is triggered by charge deposition in the well area of the vertical bipolar parasitic transistor. This is typically the transistor with the highest gain and has the largest sensitive area. Because this region is furthest from the well contact, ion strikes in region 1 (Fig. 5) experience the largest lateral resistance and consequently are first to turn on the vertical bipolar transistor. Strikes in region 2 have a lower lateral resistance, but still can cause sufficient voltage drop to trigger latchup, while strikes in region 3 cause too small a voltage drop to cause latchup. The variation in latchup sensitivity with location explains the gradual rise in latchup cross section with increasing LET (Fig. 3). Pulsed laser tests showed strikes that were close to, but missed, the well diffusion also contributed to latchup if the charge plasma was suffi-

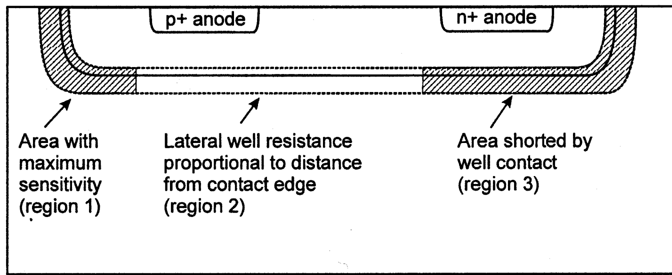

Fig. 5. Latchup sensitivity as a function of position in an n-well CMOS technology. Region 1, the area furthest from the npwell contact, is most sensitive to SEL (after Johnston, [17]).

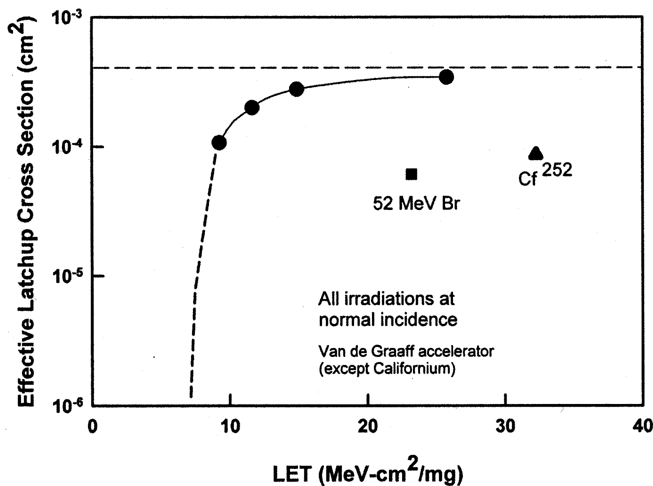

Fig. 6. Latchup from heavy ions compared to 52-MeV Br and Cf-252 fission fragments. The large discrepancy between heavy ions and the lower cross sections measured with 25-MeV Br and Cf-252 are attributed to shorter particle ranges in silicon (after Johnston [17]).

ciently dense that enough charge to trigger latchup could diffuse to the well junction. Latchup could also be triggered by strikes near the emitter outside the well, but threshold LET was about three times higher. Diffusion of charge from strikes was also shown to be important for these locations. Analyzing the time to latchup using a pulsed laser, they also determined that latchup is a much slower process than SEU, with a delay of 30–50 ns for latchup in test structures compared to trigger times on the order of ns for upset in typical CMOS memories. This relatively slow triggering time allows much more charge collection from diffusion, consistent with the above findings.

Comparing Cf-252 and heavy ion induced latchup, Johnston and Hughlock also showed that the penetration range of an ion affects latchup cross section. In Fig. 6, the latchup cross section with ion LET shows a threshold region near 6 MeV-cm^2/mg which rises rapidly through a shoulder region to an asymptotic saturation region near 5×10^{-4}cm^2. These data were taken with ions with ranges greater than 25 μm ensuring a constant LET through a depth of 4 to 10 μm. The cross section using 52-MeV Br ions was significantly lower, while the Cf-252 cross section was a factor of 5 $\times$ lower. Both of these sources had comparable ranges in Si, but Br is mono-energetic leading to an easier interpretation of the data compared to Cf-252. The conclusion is that depth of penetration is a significant consideration in measuring SEL, especially given the importance of charge diffusion. Johnston recommended using ions with constant LET to depths of at least 10 μm to ensure uniform charge deposition in the regions of interest for SEL. Note that this is significantly deeper than is normally used for SEU in CMOS ICs.

Following their work of 1990, Johnston *et al.* conducted an in depth study of the effect of temperature on SEL in 1991 [21]. Using test structures with bulk n-well and p-well CMOS processes, epitaxial n-well based structures, and 64 K SRAM with a bulk p-well CMOS process, they showed that latchup threshold is determined by total charge collected and triggering sensitivity. The first term is weakly dependent on temperature but depends strongly on doping, while triggering sensitivity increases $\sim$2.5$\times$ with an increase in temperature from 25 to 100 C, primarily due to increasing voltage drop in the well as spreading resistance increases. This effect was shown to be independent of the substrate type and differences in processing for the devices tested. Cross section was shown to increase $\sim$2$\times$ due to increasing diffusive charge collection. With increasing charge collection, regions with a lower resistance to the well contact could achieve the same emitter forward biasing and trigger latchup. Additional latchup paths were not necessary to explain increases in saturation cross section with temperature.

As devices continued to migrate to smaller geometries, SEL sensitivity also increased. Significant developments in SEL study from the early 1990s focused on proton induced latchup. In 1992, an on-orbit observation of latchup was reported by Adams *et al.* [22] in an instrument that contained significant signal processing capabilities using microprocessors and solid state memories on board the ESA Earth Resources Satellite ERS-1. Latchups occurred at an altitude of 784 km during transits of the South Atlantic Anomaly, a region of intense proton flux off the eastern coast of South America. Subsequent ground testing of an equivalent engineering model of this instrument determined that the CMOS memories had SEL thresholds of less than 3 MeV-cm^2/mg, and could be upset with protons at energies below 33 MeV. An increase in cross section with angle of incidence was also observed. The memories were fabricated in a 2-μm poly gate, bulk CMOS technology on n-type substrates and no epitaxial layer. It was later shown that latchup in these devices was due to energetic recoiling nuclear fragments from a proton spallation reaction and not from alphas or direct ionization by the primary proton beam [23]. These simulations also explained the angular dependence of latchup observed by Adams *et al.* in that the strongly forward-scattering recoil fragments deposit more charge to trigger latchup when parallel with the long dimension of the sensitive volume. That same year, proton-induced latchup was measured by Nichols *et al.* in 32-bit commercial microprocessors known to have a very low heavy-ion latchup threshold [24].

By the mid 1990s, researchers were attempting to connect the latchup sensitivity observed from heavy ion strikes to that from proton irradiation. An additional problem was the variability seen in proton latchup cross sections observed in different devices. About 1 in 10^5 protons interact with a silicon lattice atom to produce an energetic recoil ion [25], so to first order one might expect to have a proton SEL saturation cross section that is 10^5 lower than with heavy ions. What researchers were finding was

a difference of greater than 10^8 in some cases [26], even when heavy-ion latchup threshold was extremely low. Particles of most interest for proton latchup are recoiling atoms with energies in the 5–15 MeV range, which have ranges in silicon of about 3 μm. Johnston *et al.* demonstrated that differences can be explained when one considers the vertical structure of the device, substrate doping, and charge collection depth in the device. Earlier models assumed that since the recoil range was short, the charge collection volume would also be limited. Johnston *et al.* showed that, in lightly doped substrates typical of bulk CMOS, charge from short-range recoils can be collected at distances 10 μm or greater below the vertical transistor base where latchup is first initiated due to the long time required for the latchup process (~20 ns). Simulations of heavy-ions in the same structure exhibit equilibrium collection depths greater than 100 μm. Using the measured heavy ion latchup cross section at an LET threshold equivalent to 0.46 pC as an estimate of the area sensitive to 10 MeV recoils, they were able to estimate the proton cross section within a factor of two for five different part types. They also showed that as proton energy increases, recoil energy increases, leading to an increase in the sensitive volume depth and its lateral extent, explaining a gradual increase in cross section with increasing energy. This model successfully accounted for the observed discrepancy in heavy ion and proton latchup cross sections.

Heavy ion latchup has also been observed in insulated gate bipolar transistors (IGBTs) [27]. This class of device has a four layer *pnpn* structure that make it susceptible to latchup. The observed effect is consistent with the previously presented model of latchup showing a region where latchup could be triggered but not sustained if load resistance was high enough to limit current during latchup. At lower resistances, latchup could be sustained until burnout. Techniques to harden IGBTs to latchup by modifying the p+ emitter plug were predicted by Lorfevre *et al.*, using a 2-D device simulator. By decreasing the distance from the p+ plug to the p-emitter and driving this diffusion deeper, the current required to forward bias this emitter base junction was significantly increased, causing an increase in latchup threshold and a reduction in cross section [27].

Much effort has been put into developing methods to harden ICs against latchup. Many of these build on the techniques first proposed by Gregory *et al.* [12] and bear further discussion here. An initial approach to mitigate latchup relied on reducing bipolar gain through neutron irradiation of bulk technologies and was effectively used in Sandia National Laboratories' bulk 4/3 micron CMOS technology [28]. This technique was superceded by use of lightly doped epitaxial silicon layers on heavily doped substrates as the technology to grow well controlled epitaxial layers matured. N+ and P+ guard rings have been used in commercial technologies as a way to achieve radiation hardeness by design [8]. Most recently, latchup can be eliminated completely by not allowing the existence of four-layer *pnpn* structures through the use of isolating substrates, such as SOI or SOS. Trends for future technologies suggest that latchup may not be possible as power supply voltages drop in deep submicron technologies latchup because the minimum holding voltage is about 1.0 V.

The best course of action when selecting parts for use in a space environment, of course, is to use parts that are not prone to latchup. Many times this approach is not possible because of performance requirements of the system or a lack of hardened parts. In these cases, damage to parts has been avoided by using circumvention techniques that remove power from the device when latchup is detected. A recent study by Becker *et al.* has shown that this widely used approach may prevent catastrophic latchup but could miss latent damage that occurs in metal traces on the IC [29]. In a series of tests on state-of-the-art components using a pulsed laser, latent damage was observed in about 30% of parts that latched up but were protected using a standard protection scheme. Reductions in aluminum metal cross section by two orders of magnitude were observed when high currents resulted in extreme extrusion of material from metal lines. This could lead to current densities on the order of 10^7 A/cm^2, which make these parts vulnerable to early electromigration failure [30].

B. SEB

While the previous section describes destructive single-event effects observed in four-layer structures, this section highlights a failure mechanism observed in power bipolar transistors and MOSFETs. This effect, known as single-event burnout (SEB), occurs when the passage of a heavy ion causes a power FET to enter second breakdown. If not rapidly quenched, the resultant high current causes the device to go into thermal runaway resulting in destructive failure. Single-event gate rupture (SEGR) is often observed simultaneously with SEB in power MOSFETs. This effect will be discussed in the next section. Power MOSFETs have many advantages in space systems in that they have fast switching times, high current capability, low on-resistance, and low gate currents. They are used in many on-board space systems, such as, battery charge assemblies, power supply electronics, power conditioning systems, momentum wheels, and controllers.

Observation of this effect was first published in 1986 by a group of researchers from Aerospace Corp who reported on a destructive "latched current" effect in a number of different n-type power MOSFETs from several suppliers [31]. In this study using Cf-252, destructive failure was observed under fission fragment flux when the drain to source bias exceeded about 50% of the maximum rating of the transistor. They attributed the failure to a turnon of the parasitic vertical emitter base junction as current is collected following an ion strike. They speculated that under high voltage bias, avalanche occurred in the collector which drove the device into thermal runaway. It was noted that the limited range of Cf-252 fission fragments may have contributed to the wide variation in V_{DS} at SEB observed in devices of the same type from the same manufacturer as well as different manufacturers of the same part type. An optical image of burnout in an IRF150 transistor is shown in Fig. 7, where burnout occurred over the drain region of a single cell of the device [32]. It is also worth noting that in the case of SEB, there was no indication at this time of on-orbit failures due to this effect. In 1987, it was estimated that there were ten spacecraft in orbit using some 300 power MOSFETs of the IRF150 type with the measured thresholds and saturation cross sections on these

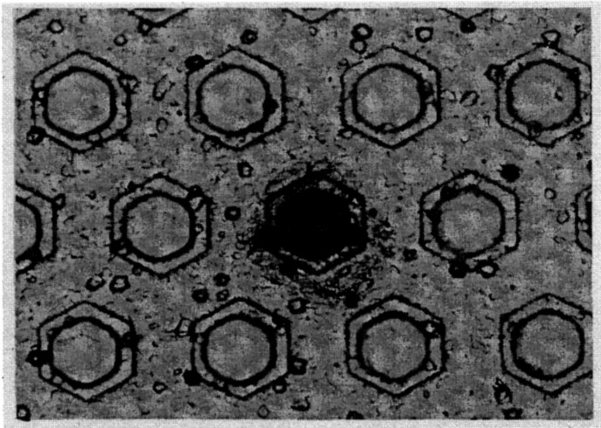

Fig. 7. SEB in a hex power MOSFET (after Stassinopoulos [32]).

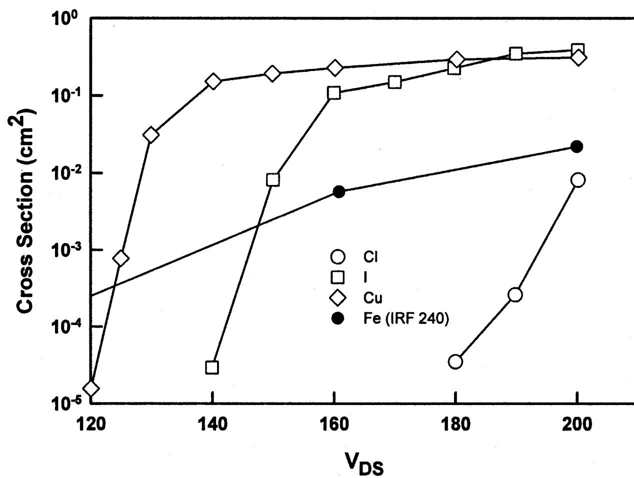

Fig. 8. SEB cross sections as a function of drain to source voltage V_{DS}, for a 2N6766 power MOSFET. Threshold V_{DS} generally decreases with increasing LET, except when the ion range is short compared to the active region of the device. Response from Fe is discussed in the text (after Oberg [34]).

parts, it was estimated that the probability of observing SEB was much less than one [33].

A more detailed study of SEB was performed the following year independently by Oberg *et al.* [34] and Fischer [35] using techniques that prevented burnout by limiting current with a series resistor and removing power within 1 μs of detection of a high current condition. Because a single part can be triggered into SEB many times, many more experiments can be performed in a shorter time using fewer parts with this approach. For the parts they tested, Oberg *et al.* also noted that the energy stored in the device itself was not sufficient to result in burnout. When plotting SEB cross section, Oberg *et al.* observed that threshold V_{DS} generally decreases with increasing LET (see Fig. 8). In these tests, the LET for 90-MeV Cl is 16 MeV-cm^2/mg, 90-MeV I is 30–40 MeV-cm^2/mg, and 200-MeV Cu is 28 MeV-cm^2/mg. Even though the surface LET of the Cu ions is lower than that of I, Cu ions deposit more energy in the active region of the device because of a longer range. Exposure to very high energy Fe at three energies between 16 and 280 MeV/amu exhibited a gradually increasing cross section that was above comparable LET ions at low bias and nearly two orders of magnitude below ions

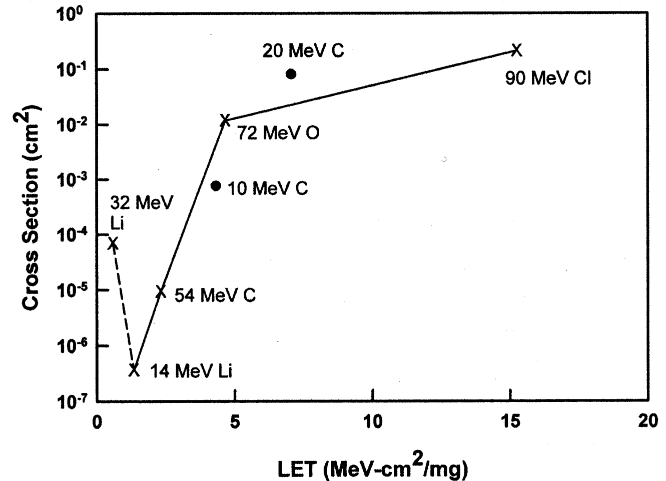

Fig. 9. Cross section for SEB versus LET (after Oberg [34]).

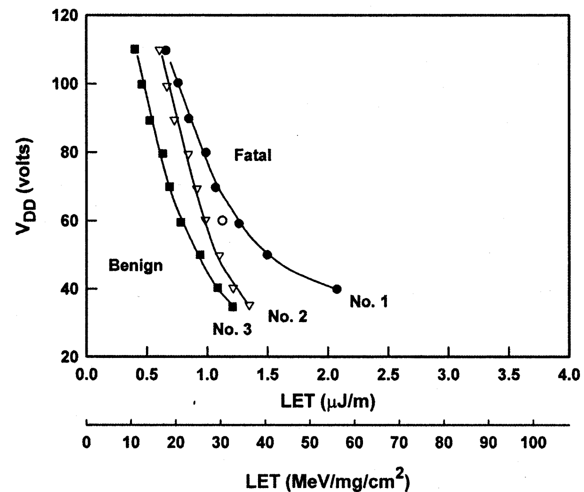

Fig. 10. SEB testing using laser simulation of heavy ion exposure. LET scale is estimated from measured incident laser energy, the absorption coefficient, surface layer transmission, energy required to optically generate an electron-hole pair and ratio of device response time and the pulse width. Three different parts of the IRF 120 MOSFET were used in the experiments (after Richter [36]).

with comparable LET at high bias. This unusual data was not fully explained at the time, but as will be shown later, can be explained in terms of energy deposition in the epitaxial layer. They also observed a clear threshold in LET at fixed V_{DS}, as low at 0.5 MeV-cm^2/mg when biased at BV_{DSS} (Fig. 9). Finally, they observed that cross section decreased with increasing angle of incidence for a given ion except when V_{DS} was above threshold, indicating that the cosine law for effective LET does not apply [34] (graphic not shown).

In the same year, Richter *et al.* demonstrated using IRF120 n-MOSFETs that SEB could be simulated using a pulsed Nd : Yg laser at 1060 nm wavelength with $>$700 μm penetration depth in Si as long as there were regions in the design that were optically transparent (see Fig. 10) [36]. Their results compared favorably to SEB data from Oberg [34] with 250-MeV Cu ions, shown as a single point in Fig. 10. Note that plotting V_{DD} versus LET provides a clear delineation of safe and fatal regions of operation for system designers.

In an attempt to explain the lack of failures in space systems, Brucker *et al.* performed a study of discrete power MOSFETs and a flight prototype power converter board designed with the same type of device [33]. No failures were observed in the power converter board when exposed to a flux of 600 MeV/amu Fe ions that were filtered to produce a spectrum similar to that observed at geosynchronous altitudes. Tests on discrete devices in the same beam showed a threshold at 80 V, while tests on a lower energy accelerator using 85-MeV Cl ions measured a threshold for SEB at 110 V, about 50% higher than earlier data from Waskiewicz [31]. The authors concluded that the lack of failures in space was due to harder parts being used in the space-qualified units compared to parts used in earlier tests. However, it is important to note that while in orbit power FETs on the power conditioning board were operated dynamically with a 25% percent duty cycle, while the discrete parts were tested in a static mode. This difference can account for the lack of SEB observed in actual space systems at that time.

A better understanding of the physics of SEB was developed with the publication of several detailed efforts to measure and model the effect [35], [37]–[39] soon after the initial experimental data was presented. Fischer [35] performed a set of tests to measure the drain current waveforms in tests on n-channel power MOSFETs and complementary p-channel devices with matched ratings. By setting the value of an external capacitor, Fischer controlled the amount of power available for destructive burnout and was able to initiate a high current condition that did not lead to thermal runaway and burnout. When more energy was stored using a larger capacitor the same device could be triggered into burnout. N-channel devices failed at V_{DS} equal to 22% to 90% of the rated breakdown voltage of the devices, while similar P-channel devices did not experience SEB up to their rated breakdown voltage. This is consistent with a model for current induced avalanche (CIA) leading to second breakdown developed by Wrobel *et al.* to explain avalanche breakdown during high dose rate irradiation in both DMOS power MOSFETs and npn transistors constructed with lightly doped epi layers [37].

Hohl and Galloway [38] developed an analytical model of SEB in order to study sensitivity of burnout to device parameters. They determined that the electric field intensity in the lightly doped n-epi region was the main contributor to SEB sensitivity. As shown in Fig. 11, a heavy-ion strike through the source (emitter) region generates a dense plasma of electrons and holes along the track of the ion strike. Electrons flow to the drain (collector) region, while holes are swept into the p-body (base) diffusion. As excess holes move through the p-body spreading resistance to the ground contact a voltage drop develops that forward biases the parasitic base-emitter junction formed by the p-body and source junction. Forward biasing leads to further electron injection into the lightly doped epi region, which under high field conditions then generates additional holes through avalanche multiplication. Current in the epi-layer increases regeneratively until the device enters second breakdown and thermal runaway. It was noted that there are conditions where burnout will not occur. Depending on drain to source bias for a particular ion strike, the currents within the device will either regeneratively increase until burnout or will die out with no lasting damage to the device. In their work, Hohl and Galloway showed that power MOSFETs can be hardened to SEB by reducing the distance from the p+ plug to the body region, but this solution is limited by lithography and maximum operating voltage of the device.

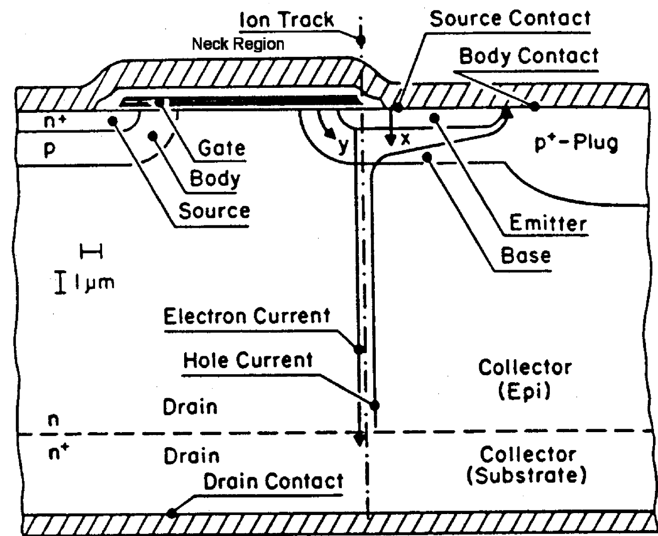

Fig. 11. Cross section of a vertical power MOSFET showing source diffusion, p-body region which forms the channel with p+ plug, the drain region formed by the lightly doped epitaxial layer, and heavily doped substrate (after Hohl [37]).

Hohl and Johnson [39], in 1989, explored the change in electric field intensity with SEB, showing that with increasing collector current the peak electric field shifts from near the base-collector junction to the epi-substrate transition with a rapid increase in hole generation at this location, consistent with a current induced avalanche (CIA) model proposed by Wrobel [37]. At this point the maximum hole generation from impact ionization occurs. They also noted that regenerative feedback depends on the gain of the parasitic npn transistor, spreading resistance in the base region, and avalanche multiplication in the drain region. Their work indicated that SEB occurs first where the highest emitter base voltage can be attained, that is, at the edge of the n+ source furthest from the source-p+ plug contact to ground.

To withstand a higher reverse voltage, the epi layer thickness is increased and the doping level is reduced. While this leads to a higher standoff voltage, it also makes a device more sensitive to SEB. In some cases, SEB is not detected in 100 V devices operated at 100% of rated voltage, while it is easily observed at the same LET for 400-V devices operated at close to 50% of full rated voltage. At lower doping levels it is easier for the peak electric field to shift from the base collector junction to the epi-substrate transition.

In the same year, Titus *et al.* performed an investigation into ways to harden power MOSFETs against SEB and SEGR [40]. Their approach was directed at ways to reduce the npn bipolar action by suppressing turnon, reducing peak electric field in the epi region, and reducing electric field transients along the gate oxide interface (discussed in SEGR section). Although the details of the design and process modifications were not disclosed, they were able to demonstrate devices that did not burnout at

94% of rated BV_{DSS}, and, with additional changes ("NS" design), devices that were not susceptible to SEB with ions up to 63 MeV-cm^2/mg (307 MeV I, range = 30 μm). Improved SEB and SEGR hardness came with some reduction in electrical performance—a 20× increase in on-resistance. They expected further improvements in the layout of the NS design to result in on-resistance lower than equivalent commercial devices while retaining SEB immunity.

A statistically significant test comparing static versus dynamic bias was not conducted until 1991, when Calvel *et al.* [41] observed that the saturation cross section for SEB in dynamic mode was two orders of magnitude lower than static mode, although similar LET thresholds were measured. This test compared 20 devices operated in static mode with 30 high reliability flight-qualified devices operated in dynamic mode. They estimated the SEB rate in a 90% worst case geosynchronous environment to be 1.3×10^{-4} and 1.4×10^{-10} errors/bit-day in the static and dynamic mode, respectively. At this low rate in dynamic operation, no on-orbit failures would be expected in a ten-year mission using 30 devices. Later data indicated that the difference between static and dynamic bias may be explained by self-heating in circuits when operated at higher frequency [32]. Effect of temperature on SEB is discussed later in this section.

At this same time, SEB in bipolar transistors was first experimentally verified by Titus *et al.* [42]. Like power MOSFETs, these transistors had a lightly doped epitaxial structure that promoted the avalanche mechanism necessary for SEB. A key result of this work was measurement of SEB voltage thresholds below BV_{CEO}, which until this time had been considered the highest safe operating condition for bipolar transistors. Using an analytical model of SEB following Hohl *et al.* [39], these researchers also explored the dependence of SEB on design parameters such as n+ emitter stripe width and current density, finding that narrow stripes and increased base doping lead to improved SEB burnout performance consistent with lowering the base-emitter voltage drop.

In the early 1990s, SEB research continued with attempts to explain the effects of ion range on sensitivity and to estimate SEB rate during space missions. Methods to estimate single-event rates in space rely on models of the heavy ion energy and flux in space under different conditions of space weather, SEB threshold determined from measurement or models, and estimates of the charge collection volume [43]. Stassinopoulos *et al.* showed that burnout at a fixed bias depends on charge distribution along the ion track and not just the surface LET of the ion used [32]. They showed that charge generation at least as deep as the epi-substrate junction contributes to SEB. In addition, in calculating critical charge to burnout, they found evidence of an energy dependence, with higher energy ions having a lower threshold than lower energy ions with similar LET. Other researchers [44] have explained energy dependent effects on lower charge recombination with higher ion energy due to a larger track diameter. Estimates of SEB rate in several model environments showed a factor of 10× increase in SEB rate with a 2× decrease in charge collection depth, illustrating that the most conservative estimates of SEB rate should be made using the thickness of the n-epi region below the p-base.

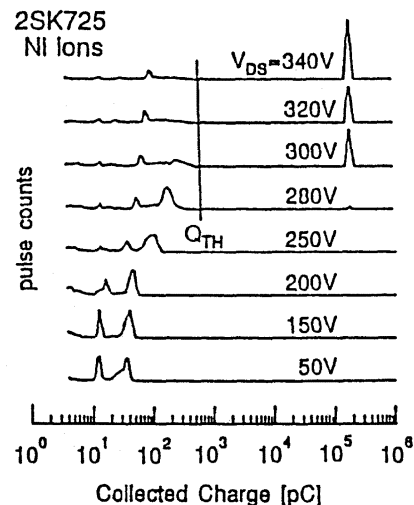

Fig. 12. SEB charge collection measured using pulse height analysis technique. Q_{th} is determined by the maximum rightward shift in peaks until the large peak, about 10^5 pc is observed indicating the occurrence of SEB (after Kuboyama [45]).

The critical charge to trigger SEB has been measured by Kuboyama *et al.* using a charge sensitive pre-amp and pulse-height analyzer system [45], like those typically used in ion beam charge collection measurement techniques [46], [47]. Critical charge, coupled with the dimensions of the sensitive volume, is key to estimating error rate in space environments. When measuring charge in the drain node of the power MOSFET during a heavy ion strike, a peak in the collected charge occurs at low voltage or low LET that has been identified with charge collection in the drain depletion region (see Fig. 12). With increasing LET or V_{DS}, a second peak appears to the right of the first that is associated with transistor action in the base emitter junction of the vertical parasitic transistor, and both peaks move gradually to higher charge. When SEB occurs, a high charge peak appears corresponding to the runaway current avalanche condition. The highest charge measured just before the onset of SEB corresponds to the critical current to trigger SEB. This value, Q_{th}, stays constant under any condition that can cause SEB, indicating that it is dependent on device design only and not the operating conditions or ion triggering SEB. No follow-on work using this technique has attempted to relate Q_{th} to estimates of sensitive volume and measured SEB thresholds, which may be useful in better estimating SEB rates.

Unlike latchup, increased temperature reduces susceptibility to SEB, through its effect on impact ionization in the base-collector space charge region. Impact ionization rate decreases with increasing temperature, causing a reduced hole current flow into the base region and a lower base emitter voltage at the source region. By incorporating the effects of temperature into an analytical model for burnout, Johnson *et al.* demonstrated a higher critical current density for burnout at a given V_{DS} and estimated an increase of 3%–5% per 100 C [48]. As shown in Fig. 13, this results in a large increase in V_{DS} threshold. In this work, Johnson also explained the shape of the SEB versus LET curve in terms of the influence of strike location on triggering the emitter base

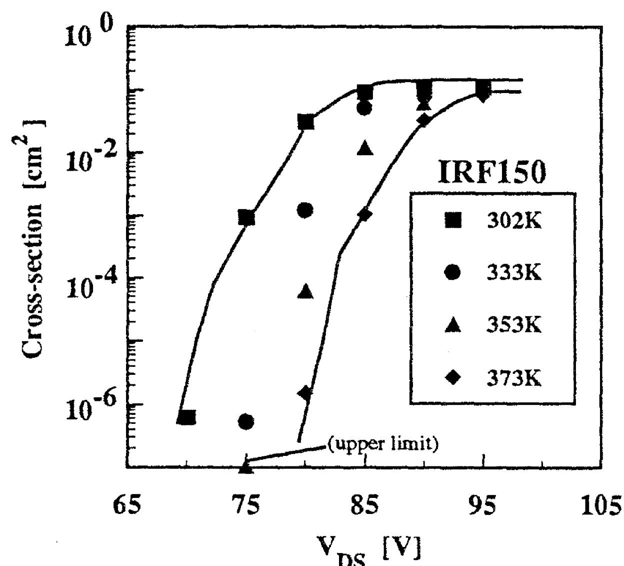

Fig. 13. Dependence of SEB on temperature (after Johnson [48]).

parasitic transistor. Strikes furthest from the body ground contact were first to trigger SEB and required the smallest LET or V_{DS}, while strikes moving closer to the ground contact required higher LET or bias to trigger SEB. This leads to increasing area that is sensitive to SEB as bias or LET increases, until, at saturation, the entire area of the source region is sensitive to SEB. A more detailed study of ion impact location on SEB with 2-D Medici simulations was published by Dachs *et al.* in 1994, confirming that the neck and channel regions furthest from the body contact are most sensitive to SEB [49]. The neck region is the space between adjacent p-source diffusions where the drain region extends to the Si-SiO_2 interface. The poly-silicon layer over this region is often referred to as the Si plate.

In addition to being triggered by heavy ions, devices with LET threshold below about 15 MeV-cm^2/mg can also be triggered into burnout by protons [50] and neutrons [51] through nuclear interactions with lattice and dopant atoms in the device. The primary means of interaction is not through direct ionization as with heavy ions, but through spallation reactions and recoil Si atoms that result in higher LET particles. Proton SEBs have been observed in 200-V power MOSFETs in the Cosmic Ray Upset Experiment (CRUX) on the APEX satellite [52] at dipole shell values <2, due to flux in the proton belt and the South Atlantic Anomaly. Their measured SEB rate correlated very well with that estimated by Oberg *et al.* [51] from ground data with 148-MeV proton data. From neutron data obtained on the Los Alamos WNR terrestrial neutron simulator, Oberg also concluded that SEB would be a problem with avionics and potentially with ground based systems due to terrestrial neutrons. For a 500-V MOSFET, they estimated rates of 2×10^{-3} and 7×10^{-6} SEB/day at 40 000 ft and ground level, respectively. Neutron induced burnout was confirmed in ground level device by Normand *et al.* in a study of high voltage ($\sim$5 kV) diodes and thyristors used in train engines [53], although this was likely caused by avalanche breakdown alone, since the regenerative injection mechanism from emitter biasing cannot exist in a power diode. This suggests that SEB mechanism is dominated by avalanche multiplication at the epitaxial-substrate junction and is exacerbated in power MOSFETs by bipolar amplification with the emitter junction.

Although hardened technologies have been developed, a full range of devices for space application may not be available due to market forces that are driving many suppliers of radiation hardened parts to shift their business focus to higher volume markets. SEB continues to be a concern in commercial components and must be considered as part of a hardness assurance plan for use of any commercial power devices in space based applications. In addition, the occurrence of SEB from terrestrial neutrons indicates a reliability concern for future generation technologies.

C. SEGR

SEGR, a condition where the gate dielectric isolating the gate and channel regions fails, was first observed in MNOS transistors that are the basis for nonvolatile memories, such as erasable alterable read only memories (EAROMS). Experimental evidence for this destructive effect was first observed in cyclotron tests simulating cosmic ray environments [54] and was subsequently confirmed in more detailed tests [55]. MNOS transistors have a thin oxide layer ($\sim$2 nm) through which charge tunnels into a thicker nitride layer ($\sim$40 nm) where it is trapped, holding a specific logic state after power is removed. In a study by Pickel in 1985 using Cf-252 fission fragments, a definite LET threshold of 28–31 MeV-cm^2/mg was observed for dielectric rupture when plotting electric field to breakdown, E_{BD}, versus fragment LET [56]. The proposed mechanism for failure in these devices was Frenkel–Poole conductivity, which is exponentially dependent on temperature [57]. In this model, localized heating by carriers along the path of the initial ion strike increases conductivity through the nitride layer leading to an increased current and even more heating. Current increases regeneratively until a critical current density is reached and the film ruptures. At this point, the entire potential across the dielectric collapses across the thin tunneling oxide, exceeding its dielectric strength and causes permanent failure of the full dielectric stack. This model requires self-heating to sustain the initial current and Frenkel–Poole conductivity for current regeneration and subsequent failure.

A study of gate rupture in Al and poly-silicon gate capacitors by Wrobel in 1987 found a linear relationship between E_{BD} and 1/LET for MNOS structures and an inverse square root of LET dependence for oxides and was explained in terms of conduction through a plasma-induced pipe along the heavy ion track [58]. Self-heating as current conducts through this pipe leads to thermal runway and dielectric failure. The first observation of angular dependence was documented in this work showing an increase in failure threshold as the angle of incidence increases from normal (0°) consistent with an increasing path length for a conductive pipe through the oxide. In the same year, Fischer [35]measured SEGR in p-channel power MOSFETs when irradiated with Au ions with 0 V on the gate electrode and $V_{DS} = 36$ V. Gate rupture was explained in terms of collapse of the drain-to-channel capacitance that normally holds off the large drain voltage from the gate-to-channel under the neck region of the device due to passage of the energetic heavy

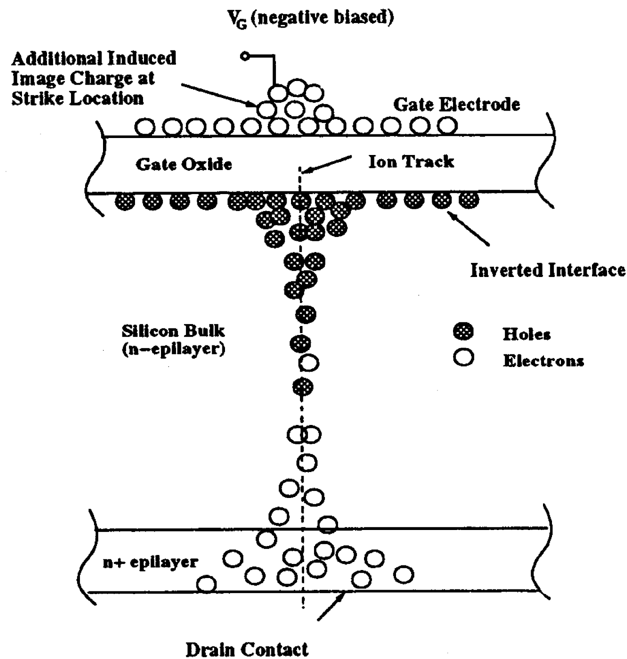

Fig. 14. Illustration of electron and hole distribution after a heavy ion strike. Holes pooling at the Si–SiO_2 interface result in a transient increase in the electric field across the oxide (after Allenspach [61]).

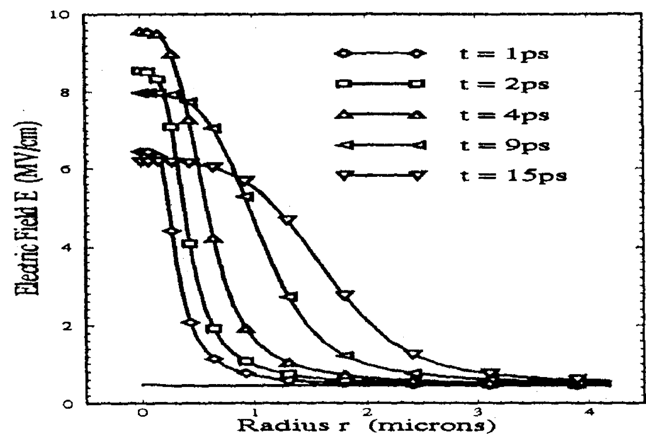

Fig. 15. Peak electric field strength at the Si–SiO_2 interface as a function of radial distance from the heavy ion strike and time following the strike (after Brews [60]).

ion. Further experimental evidence of SEGR was presented by Milgram in MOS capacitors used as radiation detectors [59].

1) Mechanism for SEGR: A model of SEGR including the effects of charge transport in the substrate was first presented by Brews *et al.* in 1993 [60]. Following a heavy-ion strike through the neck region into the substrate, the dense plasma of electrons and holes along the ion track separate under the influence of the drain bias. Electrons are rapidly swept to the n+ substrate where they no longer influence behavior, while holes transport toward the oxide end of the plasma surface and then radially through the surface accumulation layer to the p-channel where they are collected (see Fig. 14). While these holes pool up against the Si/SiO_2 interface, they induce an image charge on the gate electrode leading to a transient increase in the electric field across the gate dielectric. This transient field increases as more holes pool at the oxide interface and then decreases as excess holes diffuse laterally and are collected. This effect is shown in Fig. 15, where numerical simulations using cylindrical geometry showed that surface electric field peaks at values above the intrinsic breakdown strength of the oxide ~4 ps after an ion strike. An extension to this model was proposed by Allenspach *et al.* the next year to include the effects of transport in the oxide itself [61]. Here, the effects of the transient field at the oxide interface due to hole pooling also leads to an increased field across the oxide as in Brews' model. However, the increased field reduces recombination of electrons and holes along the ion track in the oxide itself, causing increased hole trapping in the oxide, increased leakage current, and subsequent breakdown of the oxide.

2) Empirical Expressions for Space System Designers: Unlike SEL and SEB, no way has been found to prevent destructive burnout once SEGR was triggered, so up to this point, SEGR had been studied experimentally with only a limited number of samples. The study of SEGR in power MOSFETs accelerated rapidly with the development of SEB hardened devices as discussed in a following section. As noted by Nichols *et al.*, once the SEB failure mode was reduced, failures due to SEGR were more readily observed in cyclotron experiments [62] and more detailed models soon emerged.

Statistically significant tests were first reported in 1994, when Wheatley *et al.* developed an empirical model useful for space system designers based on tests of more than 450 samples that were not susceptible to SEB but did fail due to SEGR [63]. For these tests the gate voltage was biased negatively, causing the channel region to accumulate and inducing an inversion layer at the oxide-silicon interface in the neck region. Drains were biased with positive voltage as in normal use. Under these bias conditions the voltage across the oxide is just V_{GS} minus the potential drop in Si to invert the surface (~1 V). This allows the drain and gate bias to be independently varied. Shown in Fig. 16, the data are presented as pairs of V_{DS} and V_{GS} where SEGR occurs for a given ion or LET. With increasing V_{DS} the gate voltage for SEGR, V_{GS}, decreases linearly with a given ion and LET. This is described by the relationship

$$V_{GS} = (0.84)\,(V_{DS})\left(1 - \exp\left(\frac{-LET}{17.8}\right)\right) - \left(\frac{50}{1 + \frac{LET}{B}}\right) \tag{1}$$

where $B = 53$ MeV-cm^2/mg. The first half of this equation is derived from the slope of V_{GS} versus V_{DS} and describes the response of the substrate as a function of V_{DS}. The second half is derived from the condition when $V_{DS} = 0$ and describes the effect of ions on just the oxide. For this study LET increased from 3.4 to 82.2 for ions of F to Au, respectively. Note that with increasing LET the curves move up and to the left, indicating that SEGR occurs at lower values of V_{GS} and V_{DS}. The dotted line in the figure shows the maximum operating region specified by the manufacturer. Close inspection shows that ions with LET of 18.8 (Ti) and higher can cause SEGR when a device is operated in this region. The dashed line on the right-hand side

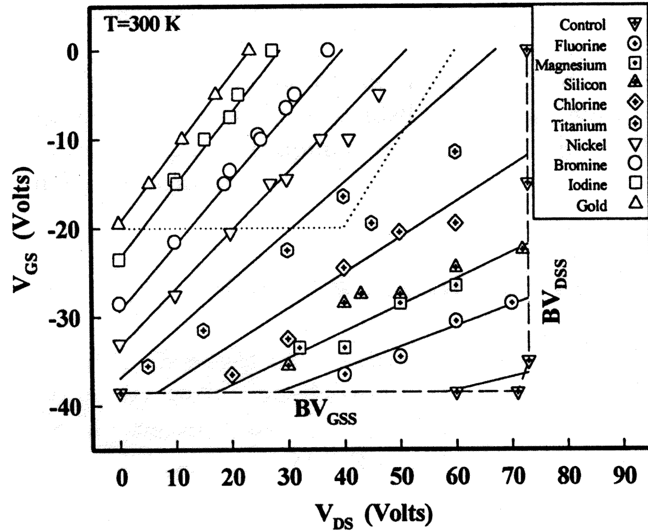

Fig. 16. Dependence of SEGR on gate and drain bias voltages and ion LET. The breakdown limits of the device are shown as dashed lines for gate breakdown BV_{DSS} and drain breakdown BV_{GSS} (after Wheatley [63]).

shows the operational limit of the MOSFET due to drain breakdown BV_{DSS}, independent of V_{GS}, while the bottom limit is the oxide breakdown limit BV_{GSS}, independent of V_{DS} without ion irradiation.

In 1995, a pair of studies explored the effects of technology trends on SEGR susceptibility in vertical power MOSFETs. Decreasing gate oxide thickness in MOS technologies leads to a decrease in the amount of charged trapped in the oxide following radiation and therefore an increased radiation hardness. The same scaling trends were being followed in power MOSFETs, so it was important to determine if decreased oxide thickness changed the SEGR response. An empirical study by Titus *et al.* found a decreasing critical voltage to breakdown, but that the critical electric field to rupture remained constant over the range of thickness explored in this study, 30 to 150 nm [64]. It was also shown that varying oxide thickness had no effect on the substrate response. This information was included in an updated empirical model for SEGR

$$V_{GS} = (0.87)\,(V_{DS})\left(1 - \exp\left(\frac{-LET}{18}\right)\right) - \left(\frac{10^7 Tox/\cos(\theta)^n}{1+\frac{LET}{B}}\right). \quad (2)$$

Note that the first half of the empirical SEGR equation is unchanged from (1) except for minor changes to the fitting factors, while the numerator of the second half fitting oxide response now reflects the accepted dielectric strength for oxides in this thickness range. Changes with angle of incidence were fit by $1/\cos(\theta)^n$ with $n = 0.7$, slightly less than the dependence expected for increased ion path length through the oxide. Data and model values are compared in Fig. 17. In this work, Titus *et al.* also showed that channel type did not affect SEGR, with n- and p-channel power MOSFETs showing the same SEGR sensitivity. This is a somewhat surprising result, since given the effect of substrate charge on field transients at the oxide interface, one might expect to see more rapid removal of electrons compared

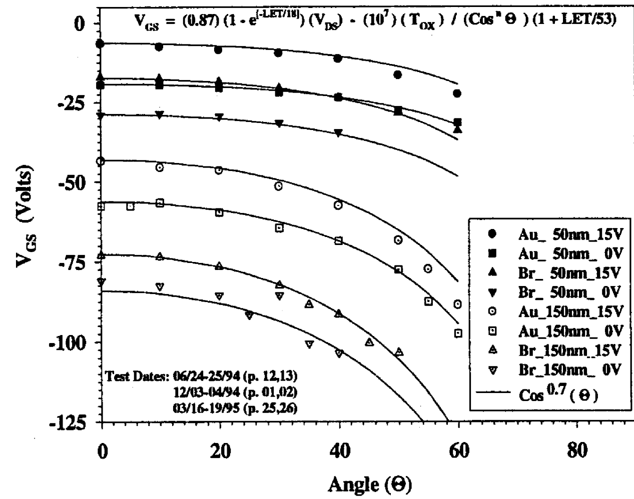

Fig. 17. Effect of ion angle of incidence on SEGR (after Titus [64]).

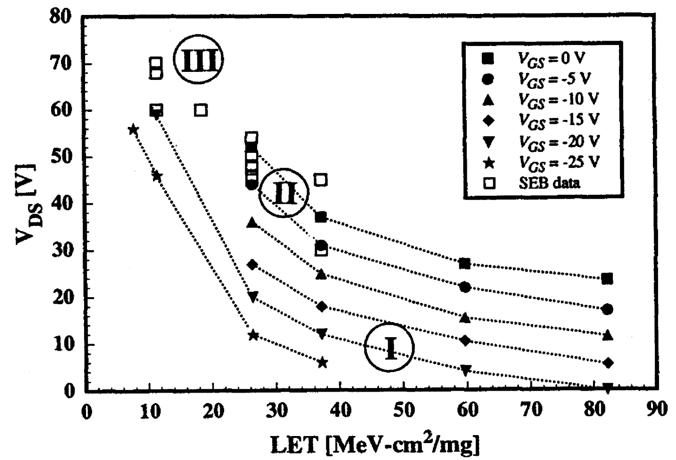

Fig. 18. Regions of varying SEB and SEGR sensitivity as a function of LET and bias voltages, V_{DS} and V_{GS}. SEGR only is observed in region I where V_{DS} is low. SEB begins to occur in region II as V_{DS} increases, while in region III, SEB dominates (after Allenspach [66]).

to holes and a commensurate decrease in the substrate response. This result was confirmed in tests of hardened devices [65].

Another way of looking at bias sensitivity illuminates the way operation of a device affects susceptibility to SEB and SEGR [66]. This is shown in Fig. 18, where three regions of response are observed. At low values of V_{DS} (region I), only SEGR is observed, although a substrate response can still be seen. Note the gradual decrease in V_{GS} with increasing V_{DS} by moving vertically along a line of constant LET for LET $>$ 40 MeV-cm^2/mg. As V_{DS} increases, both SEB and SEGR can occur (region II) while at higher values of V_{DS} (region III) SEB dominates the response.

Allenspach *et al.* [67] modeled the effect of oxide thickness on similar devices using a combination of the empirical oxide response equation and simulations of the peak electric field at the interface and showed results that matched the data of Titus very well. In this work, the magnitude of the transient field across the oxide was determined by subtracting the simulated dc gate field, E_{DC}, with no ion perturbation from the simulated peak field at the silicon surface, E_p, with an ion strike to give the maximum

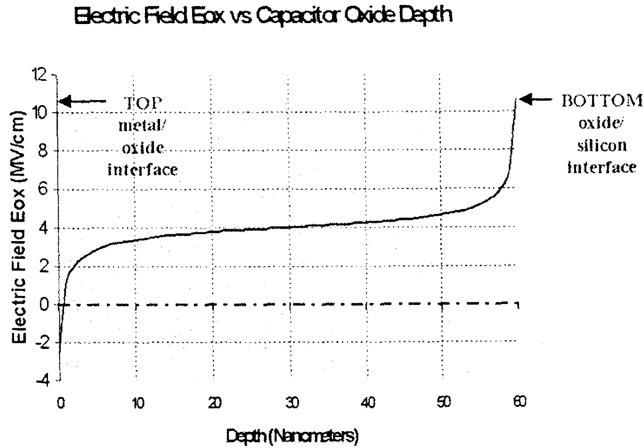

Fig. 19. Electric field strength versus depth in the oxide. Peak electric field occurs at the Si–SiO$_2$ interface due to electron transport to the anode (Boruta [69]).

combined field across the dielectric, $E_{tr\,\max}$. When subtracted from the critical field to breakdown, E_{CR}, estimated from the second half of (2), the accepted value of V_{GS} for breakdown results. This approach is expressed as

$$E_{tr\,\max} = E_p - E_{DC} \tag{3}$$

and

$$V_{GScr} = t_{ox} \times (E_{CR} - E_{tr\,\max}) \tag{4}$$

where E_{CR} is predicted from the empirical oxide response equation. Although somewhat convoluted, this technique showed that 2-D cylindrical models of the time correctly captured the substrate response.

Only recently has a model of SEGR in oxides been proposed based on electrostatics and carrier dynamics following a heavy ion strike. Building on an empirical model of Sexton *et al.* [68] that explained SEGR in terms of a combination of currents from the heavy-ion strike and the externally applied voltage, Boruta *et al.* developed a physics-based analytical model that includes electric field strengths in the oxide from the externally applied potential and the field arising from electron and hole transport and recombination after generation by passage of a heavy ion [69]. At high electric fields, electrons are rapidly swept out of the oxide to the positively biased gate electrode while holes are essentially immobile in the time frame of picoseconds that SEGR occurs. Rather than result in a linear increase in electric field versus distance in the oxide expected for a uniform distribution of holes, a distribution that peaks at the silicon-oxide interface results when taking into account recombination in the track, as shown in Fig.19. Thus, breakdown occurs near the negative electrode first where the oxide electric field reaches its maximum. From this physics based model, the empirical fitting term B in the denominator of (1) and (2) can be evaluated from first principles.

3) Temperature Effects: The effect of temperature on SEGR was first observed by Nichols *et al.* [62] but was first explained by Mouret *et al.* using a 2-D cylindrical model of the MOSFET [70] and the ATLAS-II code.[2] Their simulations predicted that SEGR susceptibility varies to the square root of temperature and can be explained by the decreased mobility of holes at higher temperature. They hypothesized that at this condition, holes that pool at the oxide interface move more slowly toward the body region and result in a higher transient electric field. Experiments over the next two years, however, did not confirm this change in SEGR threshold with temperature [64], [65].

4) Angle Effects: A decreasing SEGR susceptibility with angle observed first by Nichols was originally explained in terms of a conductive pipe model proposed by Wrobel [58]. Mouret *et al.* [70] explained a reduced substrate response by noting that holes disperse over a wider region at the surface as the ion track passes obliquely through the substrate. This leads to a lower concentration of holes at the surface and a lower voltage transient. Sexton *et al.* [68] showed that angular dependence of SEGR for thin oxides ($<$18 nm) in capacitors was well explained by the conductive pipe model with ion track diameters of 6 and 8 nm for Br and Au ions, respectively. They noted that SEGR dependence on angle vanished as the oxide thickness approached the estimated conductive pipe diameter, a strong factor supporting this model.

5) Location Dependence and Hardening Against SEGR: With the utility of models established, a detailed study of the positional dependence of both SEB and SEGR was undertaken the following year by Allenspach *et al.* [67] using a 2-D rectangular code. This study demonstrated that SEB and SEGR have somewhat different positional sensitivities. SEB and SEGR both occur in the neck region of a device. While SEB diminishes somewhat in the channel and p+ body region, SEGR is less likely to occur in these areas, and in the source region only SEB occurs, but at very high LET. This information is useful in devising ways to harden devices to both SEB and SEGR. By reducing the poly silicon plate extending over the neck region SEGR can be reduced significantly. Further improvements are gained by extending the p+ plug under the n source region, causing a reduction of SEGR in the channel regions. This results from holes being swept away from the oxide interface more quickly so they are less likely to pool at the surface.

The culmination of efforts to develop radiation hardened power MOSFETs was presented in a 1996 paper by Wheatley *et al.* on 18 device types with various die size, rated blocking voltage, channel conductivity, and temperature [65]. Most notable in this work is a significant change in the slope of V_{GS} versus V_{DS} curves versus ion LET that are the basis for the empirical expression for SEGR. Instead of a linear decrease in V_{GS} with increasing V_{DS}, the curves saturate in V_{GS} (not shown). This was attributed to the width of silicon above the neck region, with increasing silicon overlap resulting in increased dependence on LET. Since hardened devices have significant modifications to the structure of the active regions and the epitaxial region, this may be an indication of a screening effect of the substrate voltage from the oxide. Further improvements in hardness and electrical performance were

[2]SILVACO Int., *ATLAS II, 2D Device Simulation Framework, User Manual*, Santa Clara, CA, USA, July 1993.

reported in 2001 by Savage *et al.* with a stripe geometry that eliminates high electric fields at poly-gate corners and with a greatly reduced neck region [71].

Super junction (SJ) MOSFETs have superior performance characteristics compared to standard high-voltage vertical power MOSFETs due to deep n- and p-type pillars that span the depth of the epi region. The p-pillar is aligned underneath the source, while the n-pillar is aligned with the edge of the channel region, providing a conducting path to the n+ substrate. A study of SEB and SEGR in super-junction MOSFETs [72] using analytical modeling and numerical simulation showed a reduced sensitivity to both SEB and SEGR. This engineered substrate yields an exact balance between the n- and p-pillars so that the lateral electric field between these regions is horizontal and sweeps holes from a heavy ion strike into the p-pillar where they are collected and have no effect on SEB or SEGR. Reduced hole current reduces avalanche multiplication in the substrate, resulting in a 150 V increase in the threshold for SEB. A reduced substrate response also leads to a higher SEGR threshold.

SEGR has recently been observed in linear circuits [73], [75] indicating that SEGR is a reliability concern for more than power MOSFETs when used in space-based applications. In OP27 and AMP-01 op amps, failure was observed at typical operating voltages at normal incidence and was traced to high fields across large area capacitors with 46- to 61-nm oxides [75], respectively. Simulations showed critical electric fields as low as 3.4 and 4.3 MV/cm in these devices when exposed to Au ions, consistent with historical trends for these thick oxides.

6) SEGR Cross Sections: Until the mid 90s, SEGR data was always presented as shown in Figs. 16 and 17. Johnson *et al.* introduced a way to carefully measure increased gate current indicating SEGR and quickly terminates in the ion beam to get an accurate reading of fluence to SEGR [76]. As shown in Fig. 20, this leads to a cross section versus V_{GS} or V_{DS} curve, similar to the more traditional way SEU is plotted. This plot shows an abrupt threshold rising through a shoulder region to saturation at high V_{GS}. Through comparison of measured SEGR curves to simulations, Johnson *et al.* [76] related this to variation in sensitivity with location, showing that SEGR in the most sensitive neck region corresponds to threshold. With small increases in V_{GS}, ion strikes in the channel region and then under the source can trigger SEGR, resulting in an increase in area sensitive to SEGR. Saturation cross section is the cumulative area sensitive to SEGR. While this result is obtained with rather limited statistics, the curves tend to be well behaved and are intuitively appealing.

7) Dependence on Ion Energy: A number of studies into the dependence of SEGR on ion energy were conducted in the second half of the 1990s with some interesting, and as yet unexplained, results [77]–[80]. These studies used a variety of ions with energies from 54 MeV to 2 GeV, covering the range of ion energies typically used in laboratory simulations and comparing to the lower range of ion energies found in the space environment. In this way, comparisons can be made in the SEGR response to ions with the same LET but with different atomic number and energy. The first study by Titus *et al.* in 1996 [77] found the highest SEGR sensitivity (lowest measured

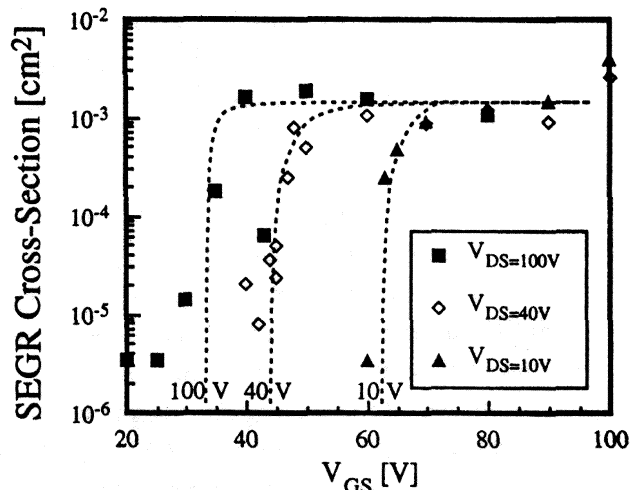

Fig. 20. Cross section for SEGR versus gate voltage, V_{GS} (after Johnson [76]).

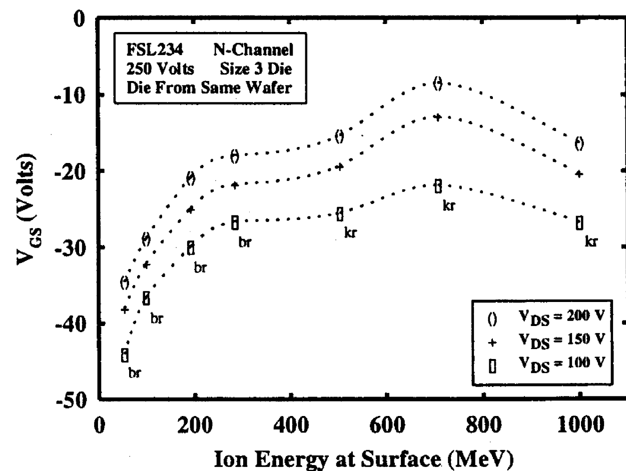

Fig. 21. Dependence of SEGR on ion energy indicating a peak at the point of maximum energy deposition in the epitaxial region and the transition layer to the heavily doped substrate (after Titus [77]).

V_{GS} failure at a given V_{DS}) did not occur at the highest LET particle, but at an intermediate LET value (708-MeV Kr with an LET of 32 MeV-cm^2/mg). SEGR sensitivity was lower at the two energies on either side of this peak, 1 GeV- and 504-MeV Kr with LETs of 28 and 36 MeV-cm^2/mg, respectively. This is shown in Fig. 21. Note that the failure voltage for 54-MeV Br was significantly higher, even though it had the same surface LET as 708-MeV Kr. These initial experiments were conducted using biases that result in both a substrate and capacitor SEGR effect. These results were explained in terms of the integrated LET profile over the depth of the epitaxial layer and suggested that maximum energy deposition in the epitaxial region is a better predictor than surface LET. This conclusion was consistent with existing theory at the time. The researchers also suggested that charge carriers from deep in the device influenced SEGR.

This neat picture of SEGR was altered by a follow-on study by Titus *et al.* in 1998 [78] using a $V_{DS} = 0$ bias that eliminated the substrate effect so that only SEGR due to the capac-

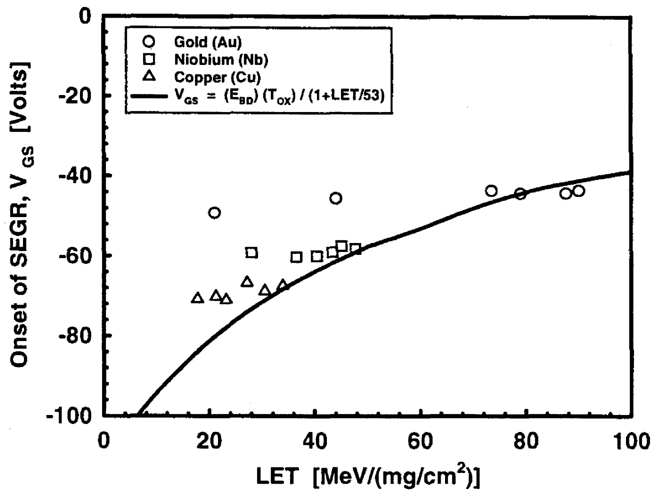

Fig. 22. Dependence of SEGR on atomic number compared to the empirical LET model (after Titus [78]).

itor response is observed. Using more ions and higher energies than the initial study they found that the SEGR threshold is dependent on Z to first order, as shown in Fig. 22. Since gate dielectrics are only tens of nanometers thick in these devices, surface LET is proportional to the amount of energy deposited in the oxide through direct ionization. One would therefore expect ions with the same LET to have the same response, which is clearly not the case in this data. This result could not be explained in terms of ion track properties, such as plasma density and radius, or with nuclear stopping. The authors concluded that the SEGR failure mechanism is a complex function of factors other than just ionization, but did not eliminate charge collection in the oxide as a primary effect. A modified empirical expression when $V_{DS} = 0$ based on Z instead of LET was proposed for just the oxide response

$$E_{\mathrm{CRIT}} = \frac{E_{BD}}{\left(1 + \frac{Z}{44}\right)}. \tag{5}$$

An independent study in 1999 using devices with similar oxide thickness but different epitaxial thicknesses found that both the oxide and substrate response could be explained in terms of the energy deposited in these regions. Using a range of ions from Br to Au and energies from 276 MeV to 2 GeV, Selva *et al.* showed that the oxide response at $V_{DS} = 0$ correlated with energy deposited in the oxide [79]. This result is in contrast to the dependence on Z shown in [78]. The substrate response, measured at nonzero V_{GS} and V_{DS} bias conditions, correlated with LET when using a quadratic function in depth that weighted energy deposited near the surface more heavily than energy deposited deeper in the epitaxial layer. This model is consistent with the combined response seen by Titus *et al.* [77]

The final paper on this subject by Titus *et al.* in 2001 confirmed that the substrate SEGR response correlated well with the average LET throughout the lightly doped epi layer and the transition region to the heavily doped substrate [80]. This indicates that energy deposition as a function of depth must be the fundamental indicator of SEGR sensitivity for the substrate response. Fortunately, for the devices in these studies SEGR was worse for ions at lower energies near their peak in LET than the very high energy ions used in these studies, so a part that exhibits SEGR with the standard suite of ions and energies is not likely to rupture at a lower voltage in space, as pointed out by Titus *et al.* [77].

At the time of this writing, the dependence of SEGR on atomic number first shown by Titus *et al.* in 1998 [78] is not fully understood.

8) Proton-Induced SEGR: Proton-induced SEGR was not reported until a paper by Titus *et al.* in 1998 which showed only a gate dielectric response with no substrate response [81]. This result is consistent with short range secondary particles from a proton reaction that can deposit sufficient energy in the oxide to trigger breakdown but cannot deposit sufficient energy to induce a substrate response. The response from 200-MeV protons were consistent with 172-MeV Mg recoils and was bounded by 191-MeV Si. Direct ionization by high energy protons could not induce breakdown.

9) SEGR in Thin Gate Dielectrics: As gate oxides in standard IC technologies have thinned with scaling, they also have become susceptible to SEGR. In 1994 and 1996, SEGR was observed in the antifuse structures of field programmable gate arrays (FPGAs), which have oxide-nitride-oxide dielectric stacks like EAROMs that first exhibited SEGR [82]–[84]. At this time, Johnston *et al.* reported SEGR in 4 Mb DRAMS operated at 5 V and, based on an estimated $1/E^2$ dependence on ion LET, predicted that deep submicron technologies would become sensitive to SEGR from Fe irons near the 2.5 V technology node [85]. If this prediction were borne out, SEGR would become a dominant failure mode for space-based systems using advanced technologies due to the abundance of Fe and Ni ions in the cosmic ray spectrum. However, in a study of SEGR in thin gate oxides, Sexton *et al.* found that as oxides scale to 18 nm and thinner they become less susceptible to SEGR due to increasing dielectric strength for thin oxides, as shown in Fig. 23 [86]. Their data fit a 1/E dependence with LET consistent with Wheatley's first empirical model [64], but with E_0 increasing and a weaker dependence on LET as oxide thickness decreases. They concluded that advanced technologies should become less susceptible to SEGR as gate oxide thickness decreases, as long as devices do not operate at electric field strengths greater than 5 MV/cm.

The following year, a pair of studies focused on whether defects in the oxides play a role in SEGR sensitivity. Johnston *et al.* suggested that SEGR sensitivity in thin oxides depends on heavy ion strikes being coincident with defects in the oxide [87], while Sexton *et al.* [68] showed that defects from prior heavy ion exposure did not affect SEGR threshold. Johnston showed that at a given test voltage many ions may pass through the oxide without causing failure, until one ion coincides with a defect that has a lower failure threshold. SEGR tests with low fluences can overestimate the breakdown voltage because the probability of intersecting a defect is lower than at higher fluences. The difference between apparent and actual failure voltages can be up to 20%. The lower failure threshold in ICs compared to test capacitors may be due to the more complex structure and processing of ICs. They also noted that some circuits with thin oxides may be sufficiently sensitive to rupture at normal operating voltages. Sexton *et al.* determined that heavy ion exposures at less than the

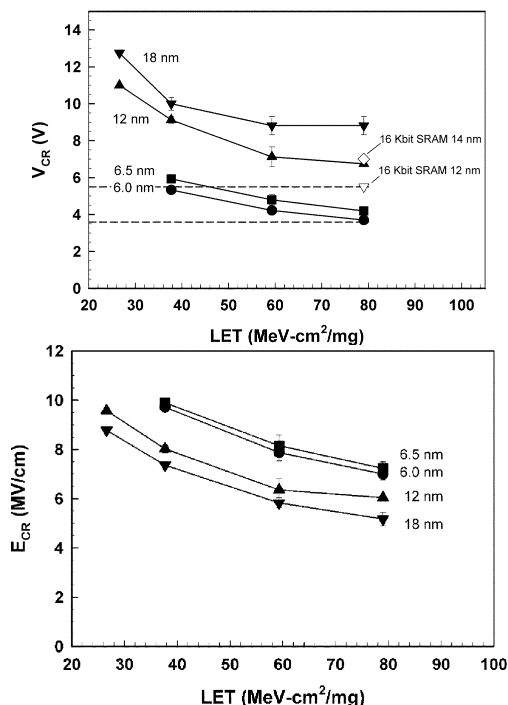

Fig. 23. SEGR as a function of heavy-ion LET for thin gate oxides. Although the voltage to breakdown decreases with oxide thickness, the electric field for SEGR shows an inverse dependence on thickness. Dashed lines show maximum operating voltage at 5.5 V and 3.6 V (after Sexton [86]).

critical voltage led to an increase in radiation induced leakage current (RILC), but not to an increase in SEGR sensitivity for 7 nm oxides and nitrided oxides up to fluences of 10^8 ions/cm^2 [68]. Both hard and soft breakdown were observed in 5-nm oxides, similar to data from Johnston [87] and other researchers showing both types of breakdown at this thickness.

A study by Massengill *et al.* of ultra-thin oxides and alternate high-k dielectrics [88] being considered for advanced technologies showed similar trends for hard breakdown as Sexton *et al.* [68], with no significant dependence on prior heavy ion fluence. They concluded that critical voltage to breakdown should be well above the operating voltages predicted by the National Technology Roadmap when these materials are expected to be introduced. Their data, shown in Fig. 24, fit a power dissipation model with V_{BD} proportional to square root of physical oxide thickness. They also found that radiation induced leakage current (RILC), also known as radiation soft breakdown (RSB), should not be a significant reliability concern for space environments due to the requirement for high fluence and high LET to produce enough cumulative damage to affect circuit operation.

10) System Impacts of Variations in Part Hardness: The topic of error rate prediction is covered in a companion paper in this TRANSACTIONS [43]. Because SEGR is more difficult to trigger at nonnormal angles of incidence, the classical error rate prediction methods using a sensitive volume described by a right-rectangular parallelpiped (RPP) model does not apply. Two studies exploring SEGR at the system level were published recently that put system risk assessment on a more firm foundation. A study in 1999 by Titus *et al.* used Monte Carlo techniques to develop confidence limits for very early failure in systems with 10 to 10 000 power transistors [89].

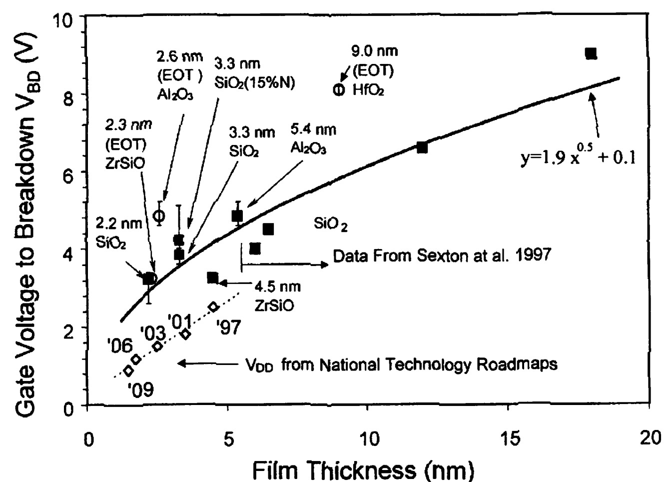

Fig. 24. Voltage to breakdown as a function of film thickness for SiO_2 and alternate dielectrics being considered for deep submicron technologies (after Massengill, *et al.* [88]).

Considering the effects of SEGR sensitive area (SSA), integral LET flux, duty cycle, and solid angle, the authors developed a risk assessment approach for varying orbit conditions and shielding that is useful for system designers to evaluate components based on the criticality of failure in a given circuit. This technique was extended in 2001 to include nonhomogeneous populations of components [90]. Nonhomogeneous component failure distributions can be a factor when using commercial off-the-shelf (COTS) components that have no fabrication lot traceability. Additionally, it is often difficult to obtain lot-tolerance-percent-defective (LTPD) data from manufacturers of radiation-hardened components. This information is essential to using this protocol, which allows designers to explore design tradeoffs, like lower gate biases, to reduce system vulnerability to component SEGR variability.

D. Snap Back

The final subject of this paper deals with single-event induced snap back (SES), a stable regenerative condition similar to latchup, caused by drain-to-source breakdown in normal n-MOS transistors. Like latchup, a high current condition results that can cause permanent damage to a device. Unlike latchup, a p-n-p-n four layer structure is not necessary for snap back. For this reason, it is often referred to as transistor latchup. Snap back was reported in 1979 in electrical studies of breakdown characteristics of technologies of that era [91], but the first report of radiation-induced snapback was published in 1984 by Ochoa *et al.* [92] in transient radiation studies.

Snap back is initiated by avalanche breakdown of the drain junction, current injection into the n-MOS transistor body, or by excess body current after a high dose rate radiation pulse or a heavy ion strike. During a radiation event, excess current near the drain junction results in avalanche multiplication and injection of holes that flow in the body region to the body contact and cause the potential at the source-body junction to increase. If an avalanche condition is sustained long enough due to a sufficiently large current pulse, the source-substrate junction becomes forward biased turning on the parasitic npn bipolar

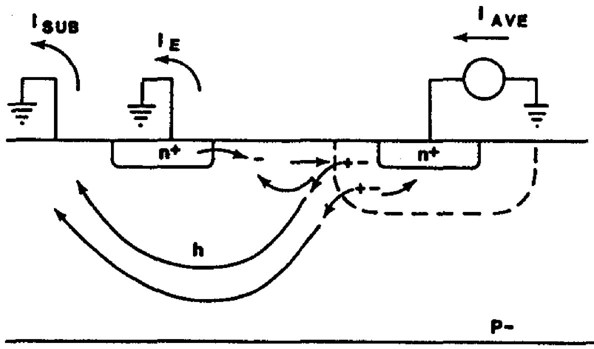

Fig. 25. Illustration of the mechanism for snap back. Avalanche multiplication in the drain region from an excess current trigger causes hole current to flow toward the substrate contact, which raises the potential at the n+ source/substrate junction. As this junction becomes forward biased, additional electron injection from the source gets avalanche multiplied at the drain causings more hole current and a regenerative "single transitor latch" condition (after Ochoa [92]).

transistor and injecting electrons into the substrate. As these feed into the drain additional avalanche multiplication occurs, causing increased substrate current, completing the regenerative feedback mechanism. This chain of events is shown pictorially in Fig. 25. Snap back cannot be sustained unless sufficient current is provided by an external circuit. For this reason, it is normally observed in I/O circuits of an IC with large-drive pull up transistors. The snap back condition can be removed by turning the channel region on and dropping the drain bias level below where avalanche multiplication will occur. Snap back does not occur in p-channel transistors due to the lower avalanche multiplication factor for holes compared to electrons.

Heavy ion induced snap back was reported by Koga *et al.* in 1989 [93] in heavy ion studies of 3-μm generation technologies operated at 10 V. As shown in Fig. 26, threshold for SES moved to a lower voltage and saturation cross section increased as ion LET or angle increased. This is due to increasing current injection into the drain junction as more electron-hole pairs are generated in or near the drain depletion region. In this study, Koga showed that the area sensitive to snap back was a small portion of the total drain area. He also predicted that with the shorter channel lengths of future generation technologies snap back would move toward lower bias levels and could be a further hardness assurance concern.

SOI technologies exhibit discontinuities in the drain IV when body ties are sufficiently removed from the channel regions. Body ties provide an electrical contact to the body region of the transistor, allowing removal of excess charge and providing a stable electrical potential. This floating body effect also is indicative of susceptibility to SES in these technologies [94]. SES in SOI technologies was investigated with 2-D PISCES simulations and experimental measurements showing an increased sensitivity at a gate bias halfway between the drain voltage and ground [95]. This was attributed to a prebiasing of the parasitic bipolar transistor in floating body SOI from impact ionization in the drain region from channel electrons. The authors concluded that SOI technologies would be most sensitive to SES during switching transients. Using 3-D simulations and focused ion microbeam tests, Dodd *et al.* showed that body tie layout

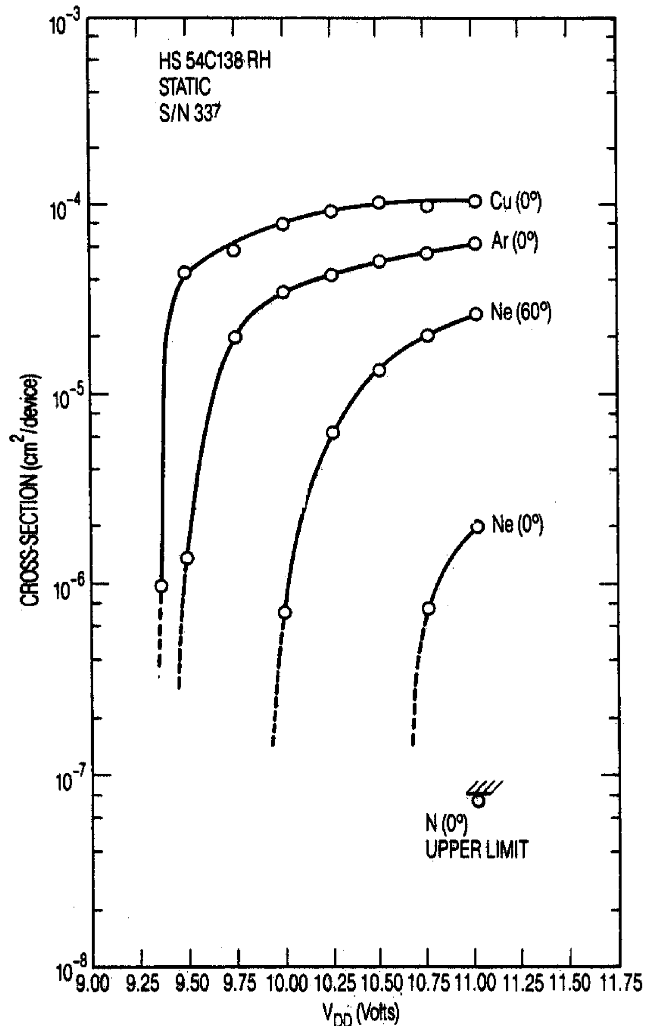

Fig. 26. Snap back cross section versus power supply voltage as a function of ion LET and angle of incidence. After Koga [93].

and transistor width are important factors in determining SES susceptibility in SOI technologies [96]. As the body tie moves further from the source region due to increasing channel width or other layout effects, less avalanche current is required to turn on the parasitic bipolar transistor and snap back can be triggered at lower drain voltage. Body tie design is an important consideration in designing radiation hardened circuits for space applications. In this work, Dodd *et al.* also showed that a window of vulnerability can occur in some circuits when the LET threshold for upset exceeds that for snap back. This can happen when devices are intentionally hardened to upset using feedback resistors, for example, or when an IC is operated at a power supply voltage where SEU sensitivity is lower than SES sensitivity. SES was also observed in commercial ICs operated at high power supply bias. Recommendations for a SES screen consisting of a snap back test just below SEU threshold were recommended during normal SEU testing for parts used in space applications.

As IC technologies continue to shrink in size and SOI technologies become more prevalent in the market, it is likely that snap back will become a significant concern in IC reliability. There is no indication yet that protons or neutrons can trigger snap back, but the possibility needs to be explored in terms of

the competing factors of shrinking geometries, application of fully depleted SOI, and reduced power supply voltages.

III. Summary

In this paper, we have attempted to trace the discovery and development of our present understanding of destructive single-event effects. The failure physics of the known destructive single-event effects as discussed in this review are well understood, and trends for existing technologies are fairly clear. However, this does not preclude the discovery of new effects in new technologies and devices that are yet to be developed. Our present understanding is the result of the efforts of many dedicated researchers who have sought to uncover meaning in often confusing and contradictory results. Their persistence and willingness to share their work openly and to collaborate with their peers has made this journey possible.

To field successful systems in the harsh environment of space it is necessary to apply this understanding by identifying those failure mechanisms unique to space and developing robust mitigation strategies to ensure reliable operation of semiconductor devices and ICs. This requires close collaboration between a team of specialists including component designers, technology development engineers, device physics simulation, systems engineers, and reliability and radiation effects specialists. As terrestrial neutron induced effects are observed, issues that have traditionally been a concern only for space-based systems will also become an issue in commercial systems. We are confident that the radiation effects community will be able to make significant contributions here as they have for space systems.

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