Front-end electronics for silicon trackers

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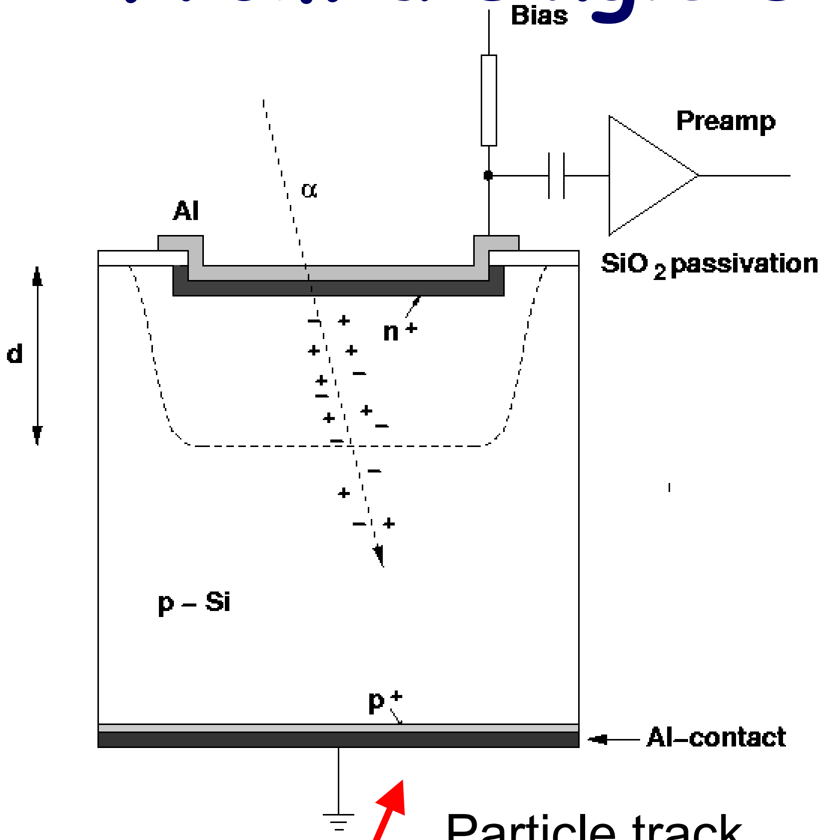
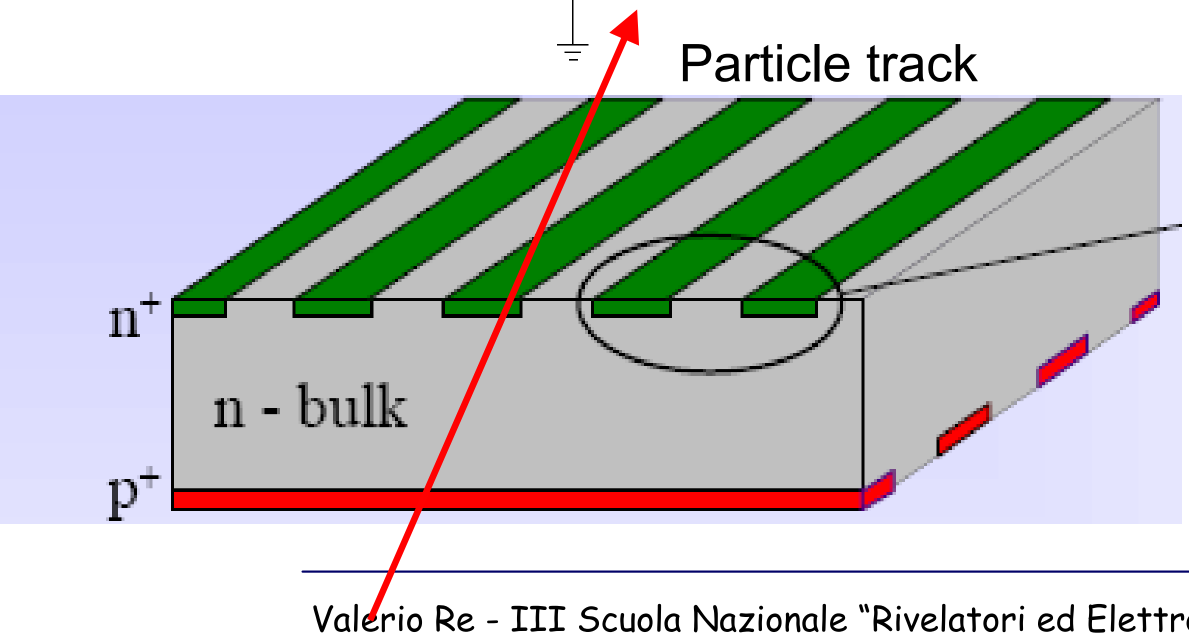
Outline

- Processing of signals from semiconductor detectors: general concepts (amplification, shaping) and electronic noise
- Discussion of fundamental design parameters of front-end electronics for silicon trackers: signal-to-noise ratio, speed, power dissipation, radiation hardness,...
- Architecture of mixed-signal integrated circuits for the readout of silicon pixel and strip detectors for tracking and vertexing in high energy physics experiments

From a single semiconductor sensor…



Ionization sensor converts the energy deposited by a particle to an electrical signal. In a fully-depleted semiconductor sensor, electron-hole pairs are swept to electrodes by an electric field, inducing an electrical current.



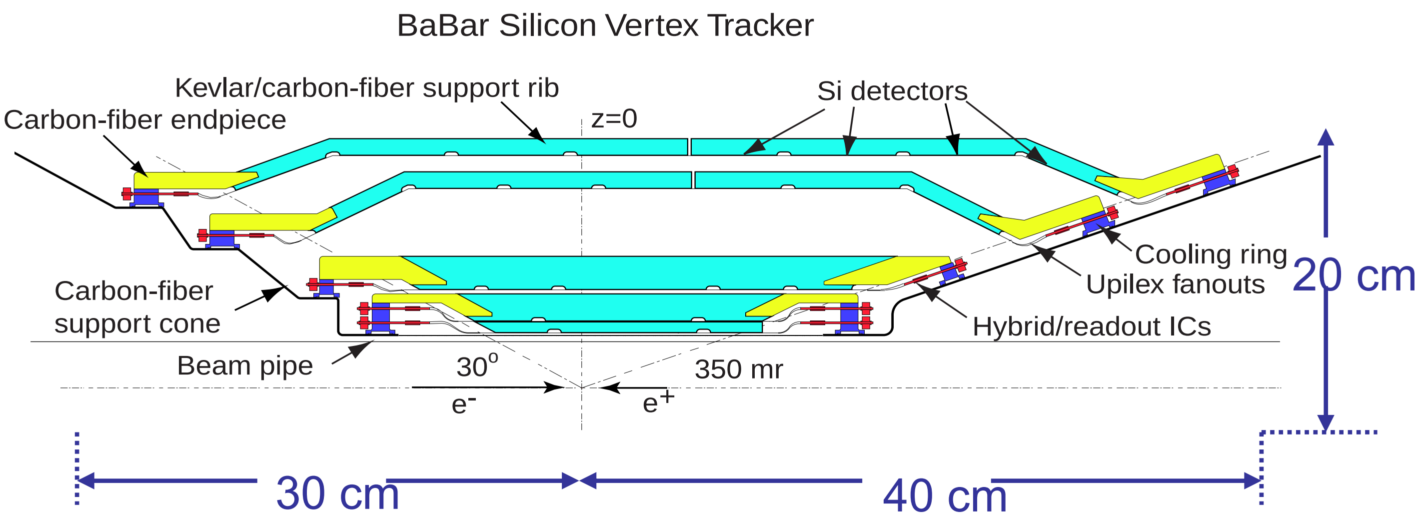
Position-sensitive detector:

Information about the coordinates of the interaction point in a segmented region (presence of a hit, amplitude measurement, timing)

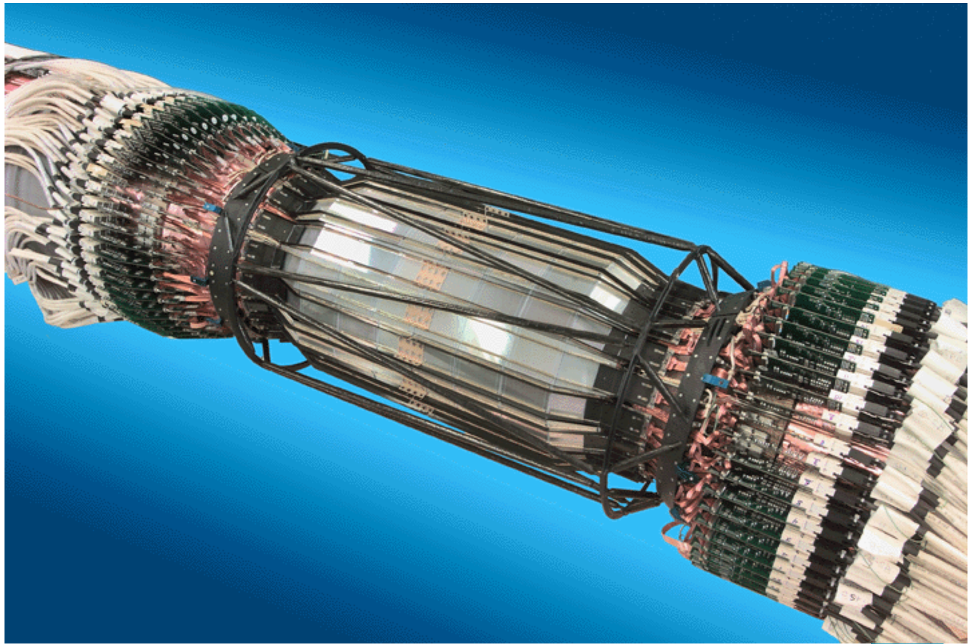
(single-sided or double-sided strip detector, pixel sensors)

…… to a full silicon tracker

Multiple layers of segmented detectors (pixel, strips) provide space points to reconstruct particle trajectories

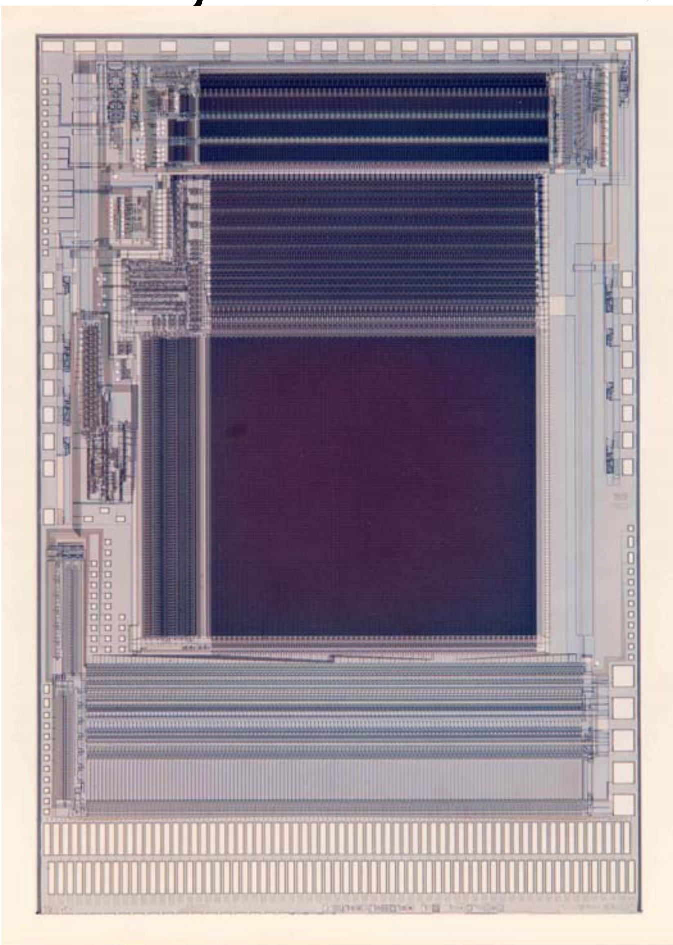


BaBar Silicon Vertex Tracker at the Stanford Linear Accelerator Center, 1999-2008: CP violation in B meson decay



Readout electronics

- Silicon strip detectors need miniaturization of front-end electronics
- They were the driving force for the development of integrated circuits for these applications



This is a mixed-signal chip, with 128-channel analog processing, A/D conversion, data storage and serial data transmission.

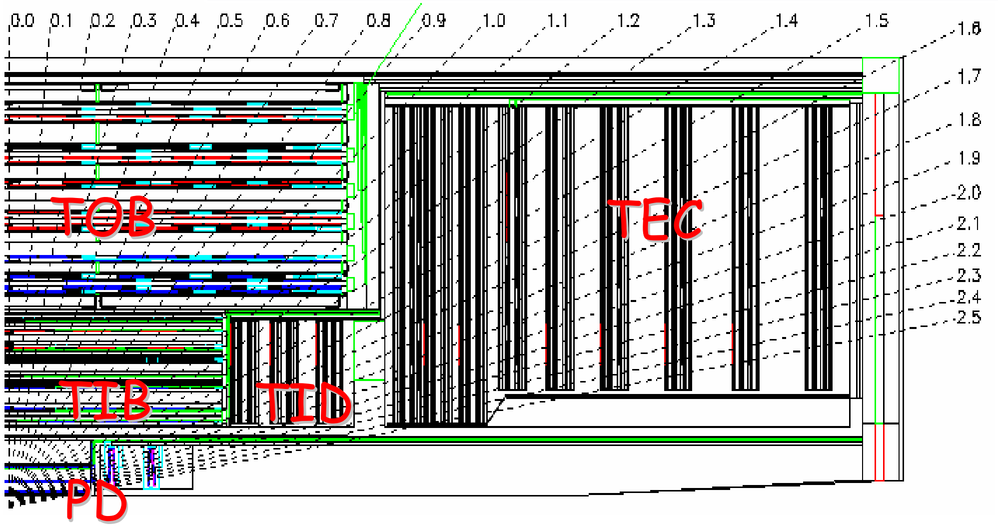
The AToM chip was fabricated in Honeywell rad-hard 0.8 μm CMOS (300k transistors) for the readout of the BaBar SVT.

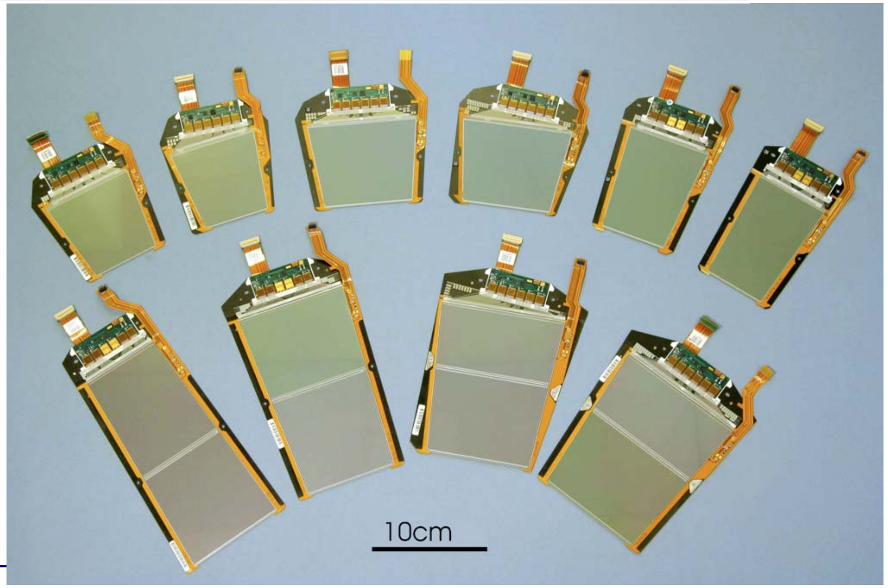
Current CMS Tracker system

- Two main sub-systems: Silicon Strip Tracker and Pixels
  - pixels quickly removable for beam-pipe bake-out or replacement

Microstrip tracker	Pixels
~210 m^2 of silicon, 9.3M channels	~1 m^2 of silicon, 66M channels
73k APV25s, 38k optical links, 440 FEDs	16k ROCs, 2k olinks, 40 FEDs
27 module types	8 module types
~34kW	~3.6kW (post-rad)

Geoff Hall, TIPP09

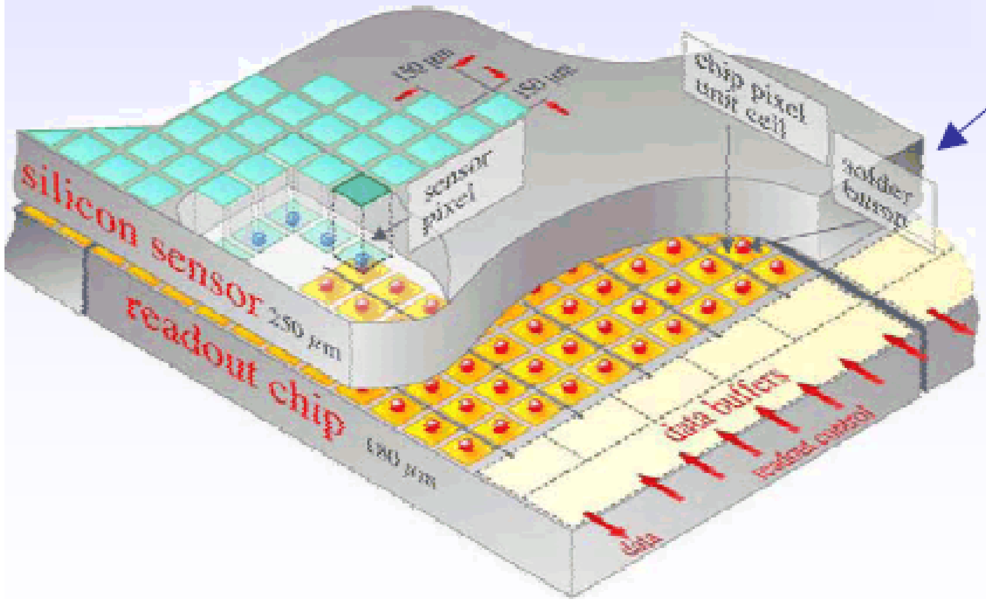




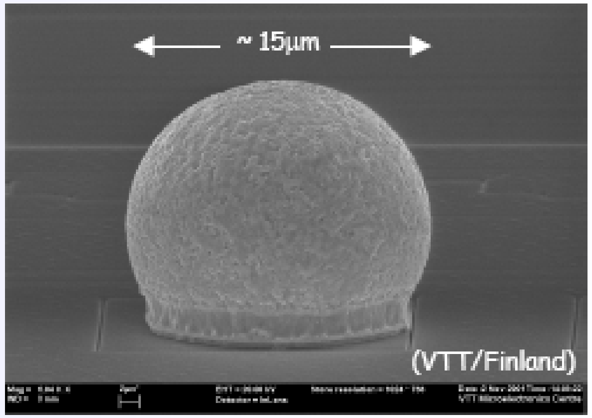
Hybrid pixel sensors

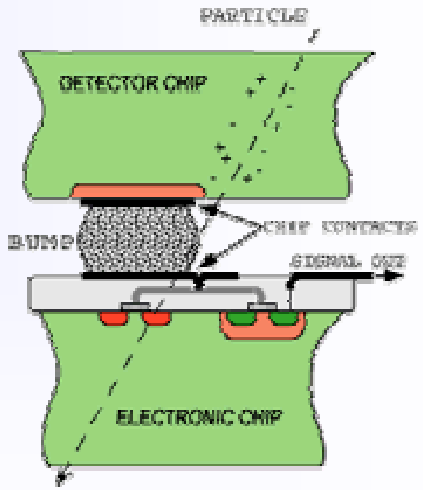
HAPS – Hybrid Active Pixel Sensors

- segment silicon to diode matrix with high granularity
  (⇒ true 2D, no reconstruction ambiguity)
- readout electronic with same geometry
  (every cell connected to its own processing electronics)
- connection by "bump bonding"
- requires sophisticated readout architecture
- Hybrid pixel detectors will be used in LHC experiments:
  ATLAS, ALICE, CMS and LHCb



Solder Bump: Pb-Sn

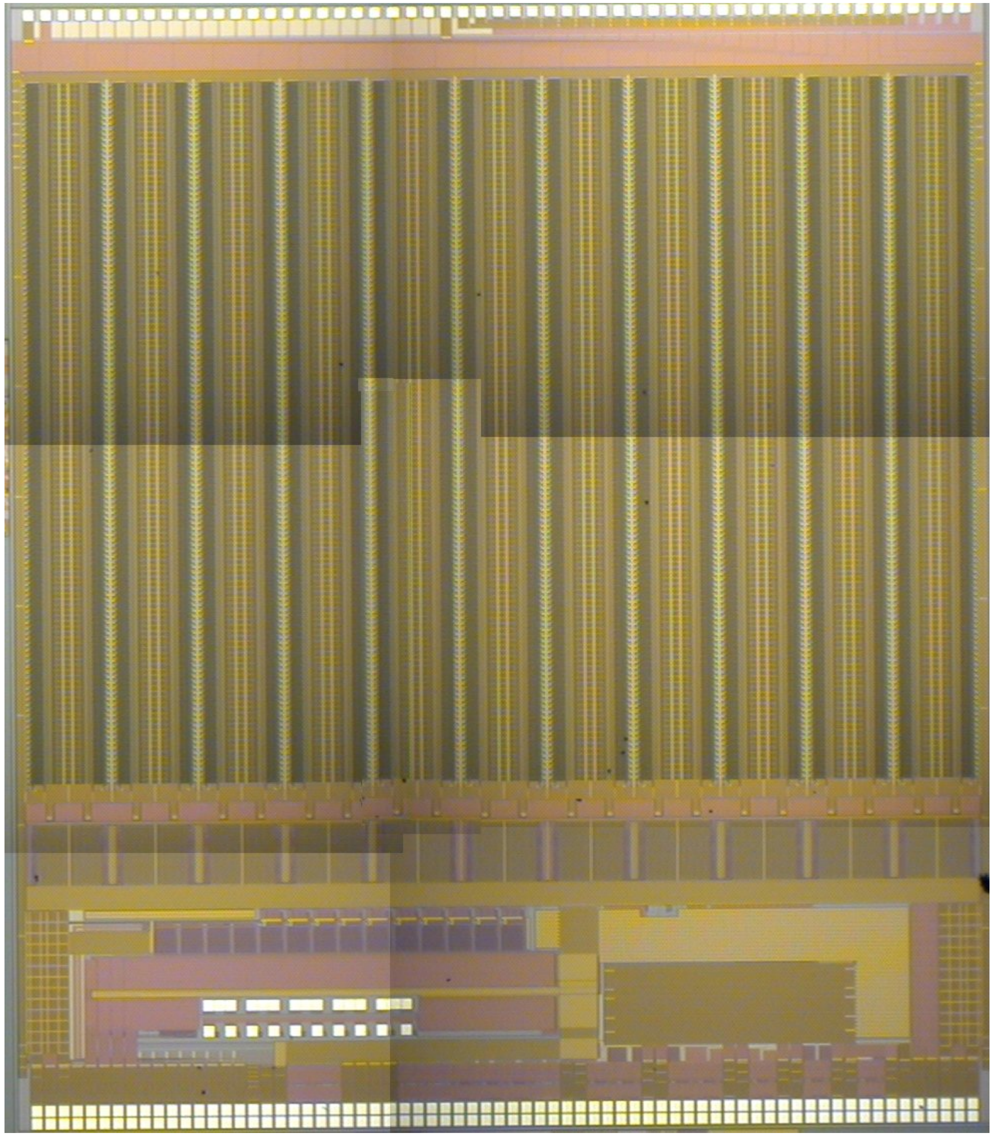




Flip-chip technique

CERN Academic Training Programme 2004/2005

FPIX2 Layout (Pixel readout chip)

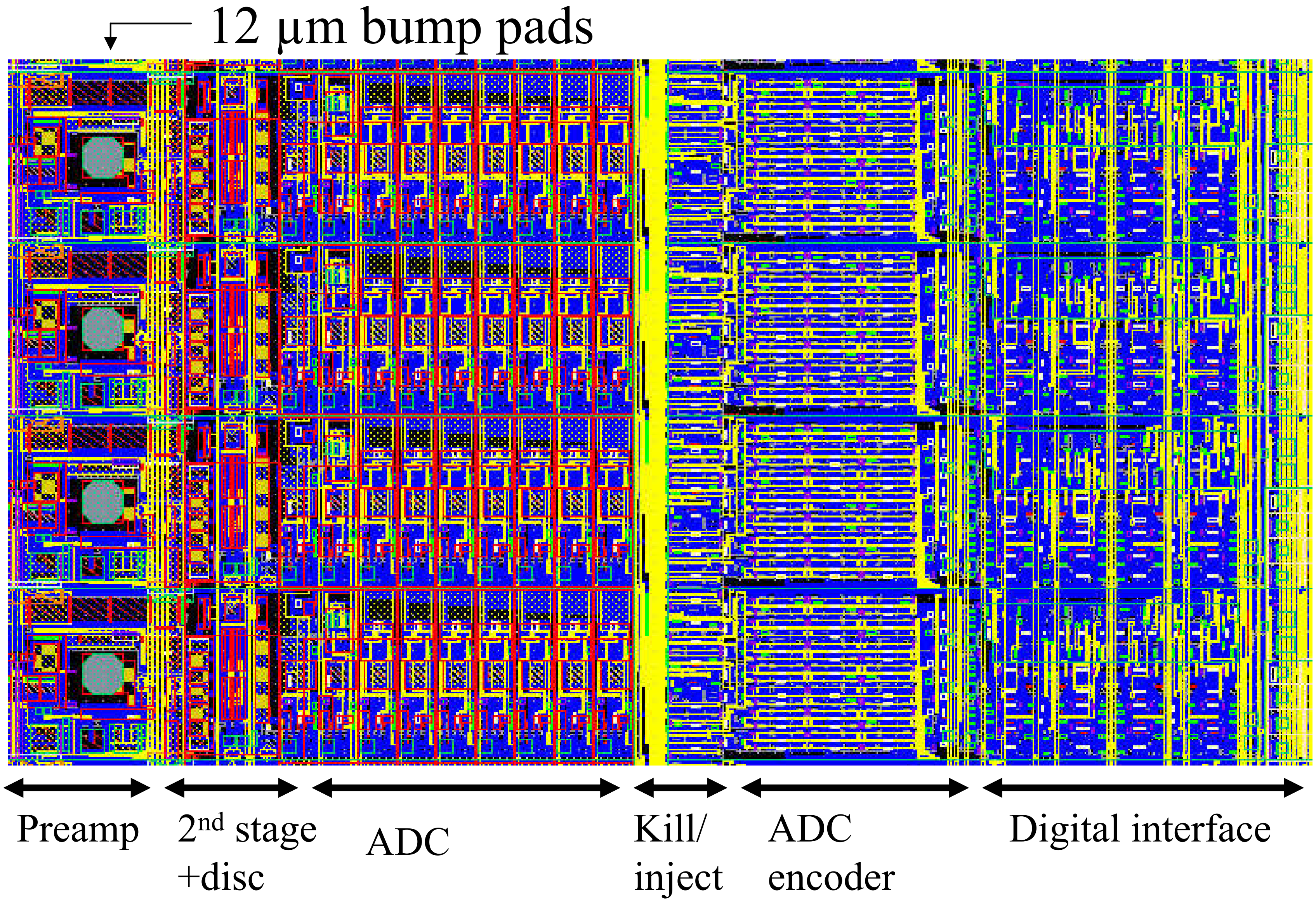


TSMC CMOS 0.25 μm

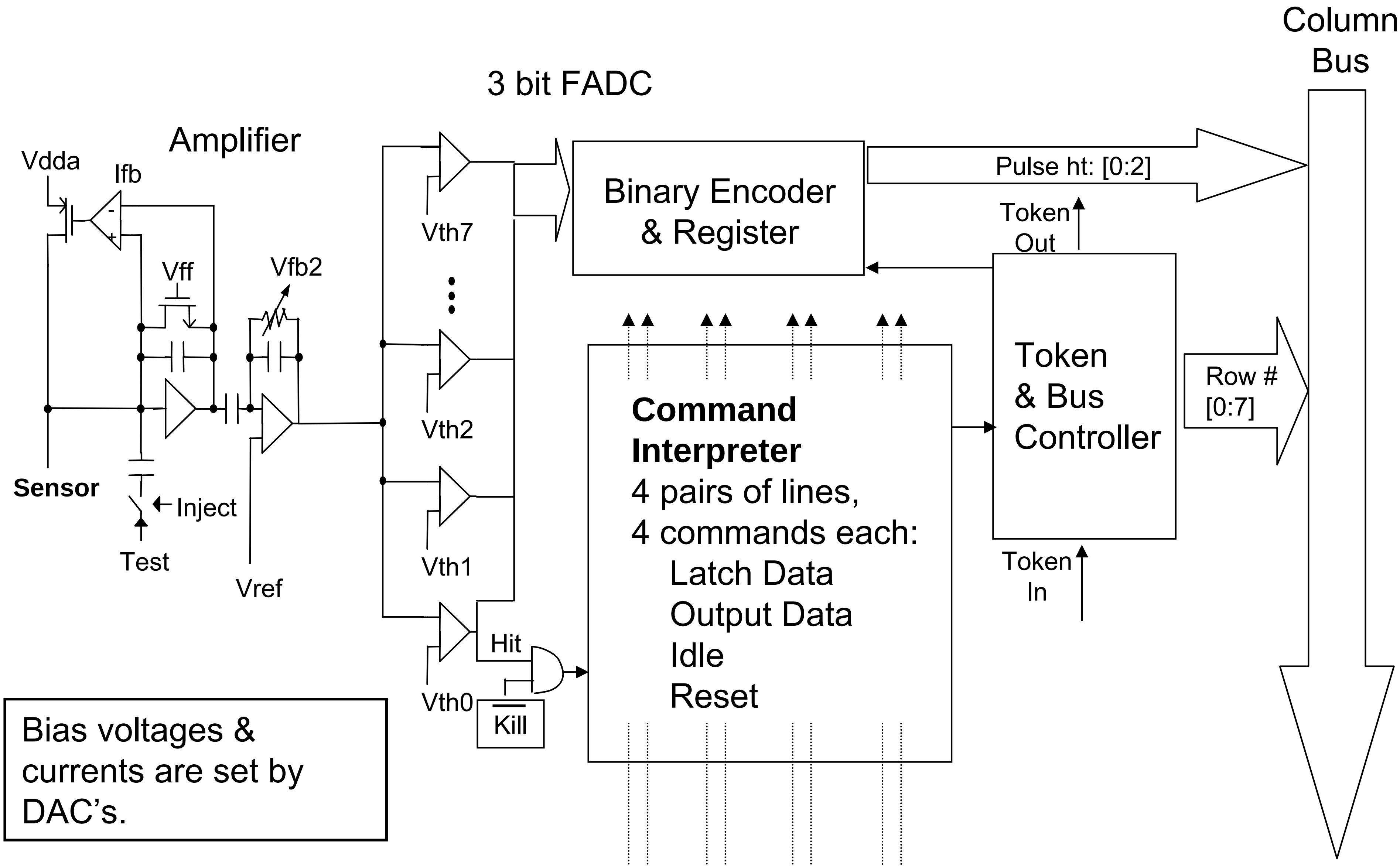
designed by Fermilab

(~ 90 mm^2)

Pixel Cells (four 50 x 400 μm cells)



Pixel Unit Cell



Bias voltages & currents are set by DAC's.

Analog front-end design for detector charge measurements

Radiation detectors

A measure of the information appears in the form of an electric charge, induced on a set of two electrodes, for which ultimately only one parameter (capacitance) is important.

Front-end electronics

amplifying device

(charge-sensitive preamplifier)

filtering, signal shaping

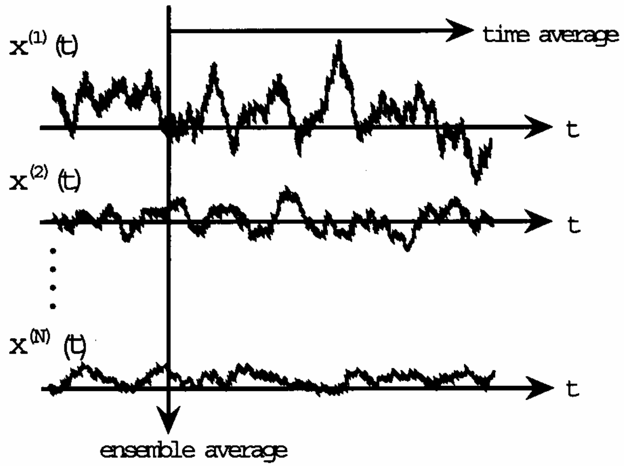
optimize the measurement of a desired quantity such as signal amplitude as a measure of the energy loss of the particle

Effect of electronic noise on charge measurements

Inherent to the conduction of current in an amplifying device is a random component, depending on the principle of operation of the device.

This random component (noise) associated with amplification gives an uncertainty in the measurement of the charge delivered by the detector or of other parameters such as the position of particle incidence on the detector.

Compromises must be made in very large and complex detector systems such as modern silicon trackers.



Statement of the problem of front-end electronics

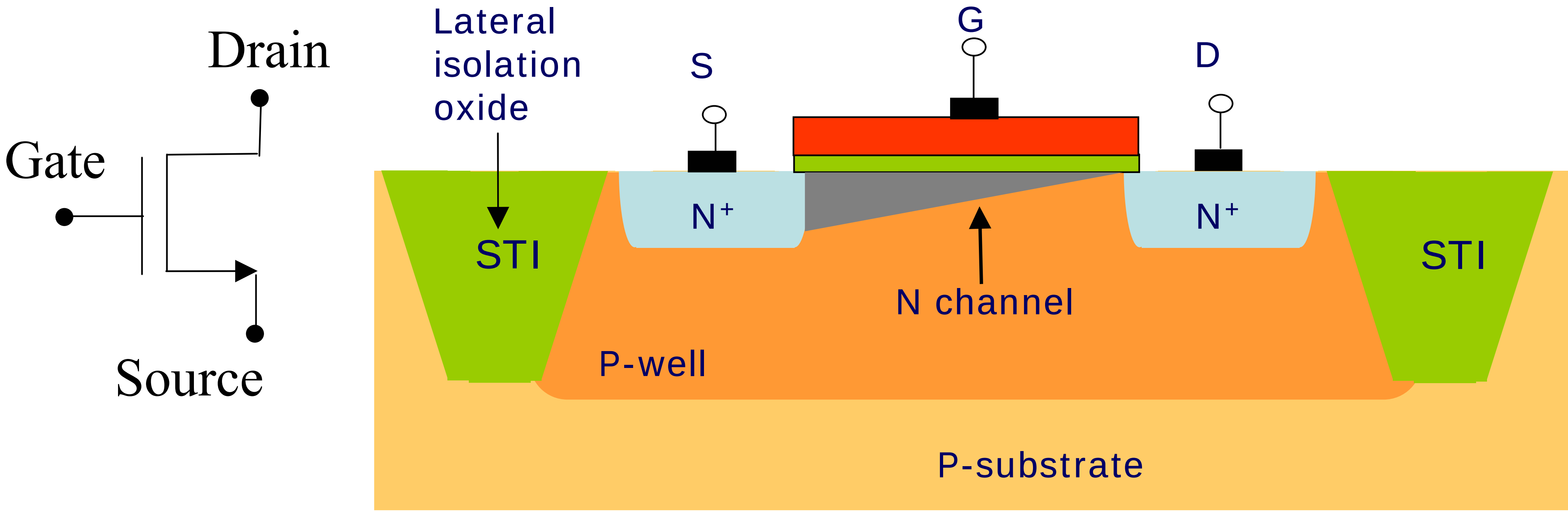
Measurement of a charge delivered by a capacitive source with the best possible accuracy compatible with noise intrinsically present in the amplifying system, and with the constraints set by the different applications.

(noise - power - speed)

The discussion of design of front-end electronics will be based on the nuclear electronics noise theory.

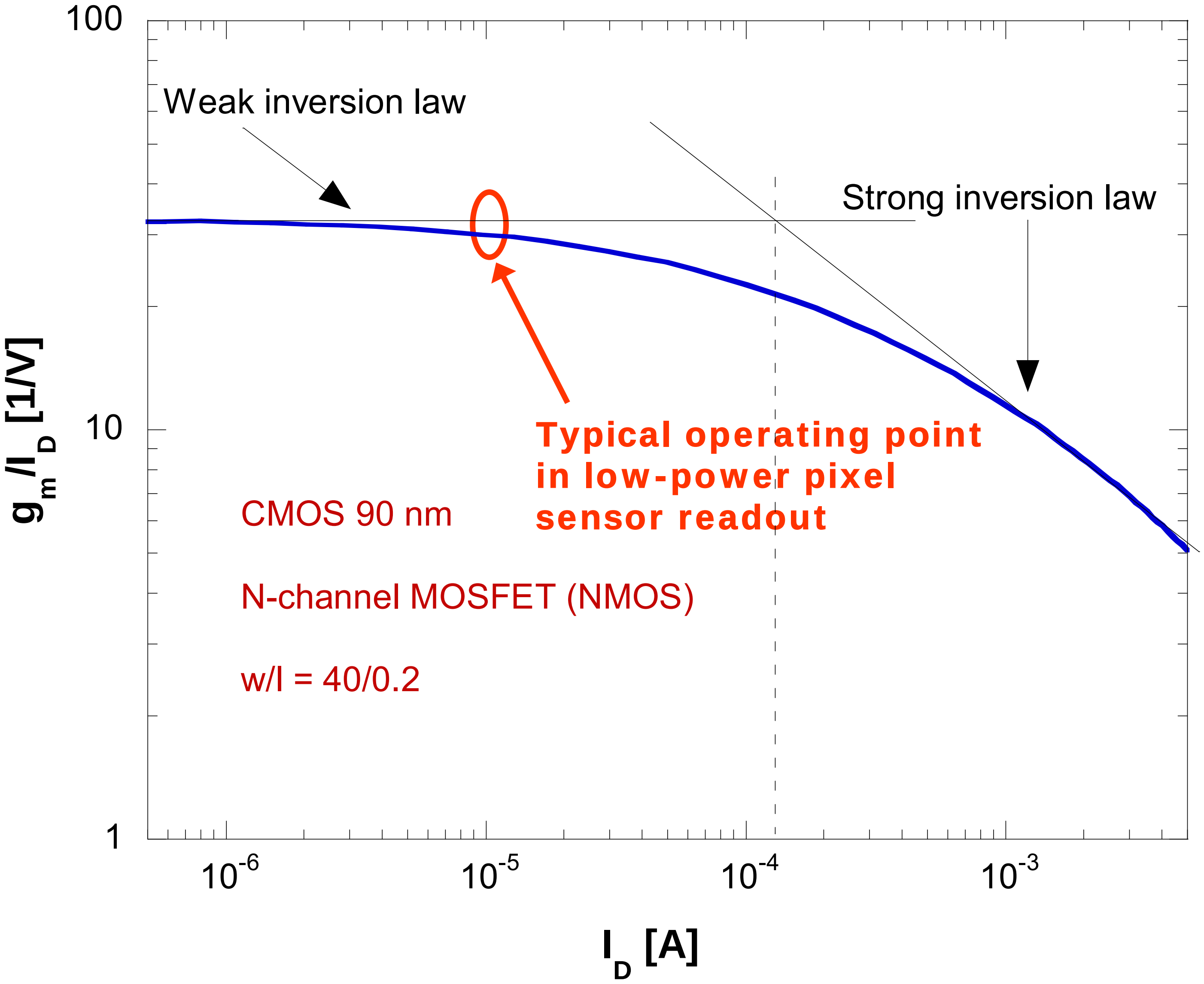
(basic equations recalled for discussion purposes)

Basic element of modern electronics: the MOSFET



- Three-terminal device: an electrode controls the current flow between two electrodes at the end of a conductive channel.
- The transconductance $g_m = dI_D/dV_{GS}$ is the ratio of change in the output (drain) current and of the change in the potential of the control (gate) electrode

MOSFET essential parameters: the transconductance g_m



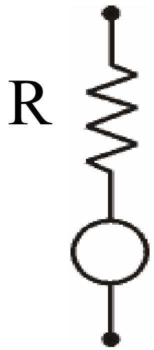
- Under reasonable power dissipation constraints, devices in deep submicron CMOS operate in the weak inversion region
- In weak inversion:

$$g_m = \frac{I_D}{nV_T}$$

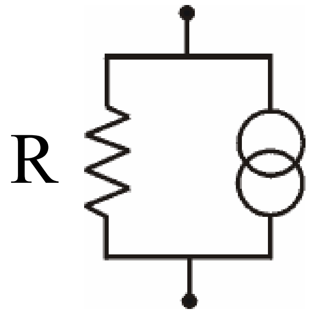
(n =1.2 in 100-nm scale CMOS)

MOSFET essential parameters: channel thermal noise

- Thermal noise arises from random velocity fluctuation of charge carriers due to thermal excitation. The spectral density (noise power per unit frequency bandwidth) is white, i.e. frequency independent. In a resistor, this can be modelled in terms of a fluctuating voltage across the resistor, or of a fluctuating current through the resistor.



$$\frac{\overline{de_R^2}}{df} = 4kTR$$

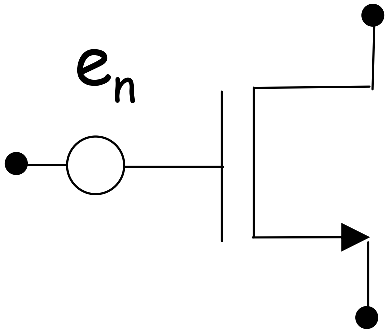


$$\frac{\overline{di_R^2}}{df} = \frac{4kT}{R}$$

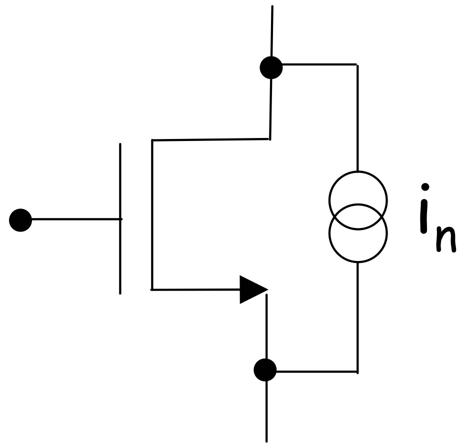
- The channel of a MOSFET can be treated as a variable conductance. Thermal noise is generated by random fluctuations of charge carriers in the channel and can be expressed in terms of the transconductance g_m.

MOSFET essential parameters: channel thermal noise

- Thermal noise in a MOSFET can be represented by a current generator in parallel to the device, or by a voltage generator in series with the gate (fluctuation of the drain current can be seen as due to fluctuations of the gate voltage).



$$\frac{\overline{de_n^2}}{df} = \frac{4kT\,\Gamma}{g_m}$$



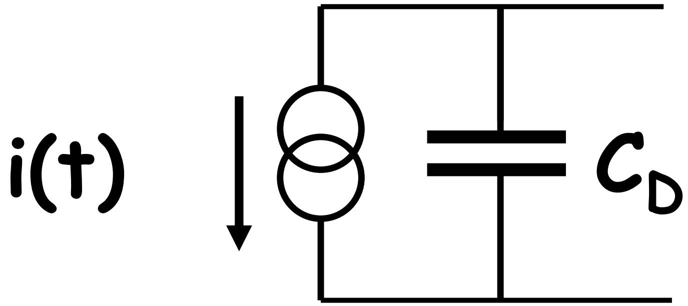
$$\frac{\overline{di_n^2}}{df} = 4kT\,\Gamma g_m$$

k = Boltzmann's constant, T = absolute temperature

Γ = coefficient ($\cong$ 1) dependent on device operating region, short channel effects…

Acquiring the signal from the sensor: the charge-sensitive preamplifier

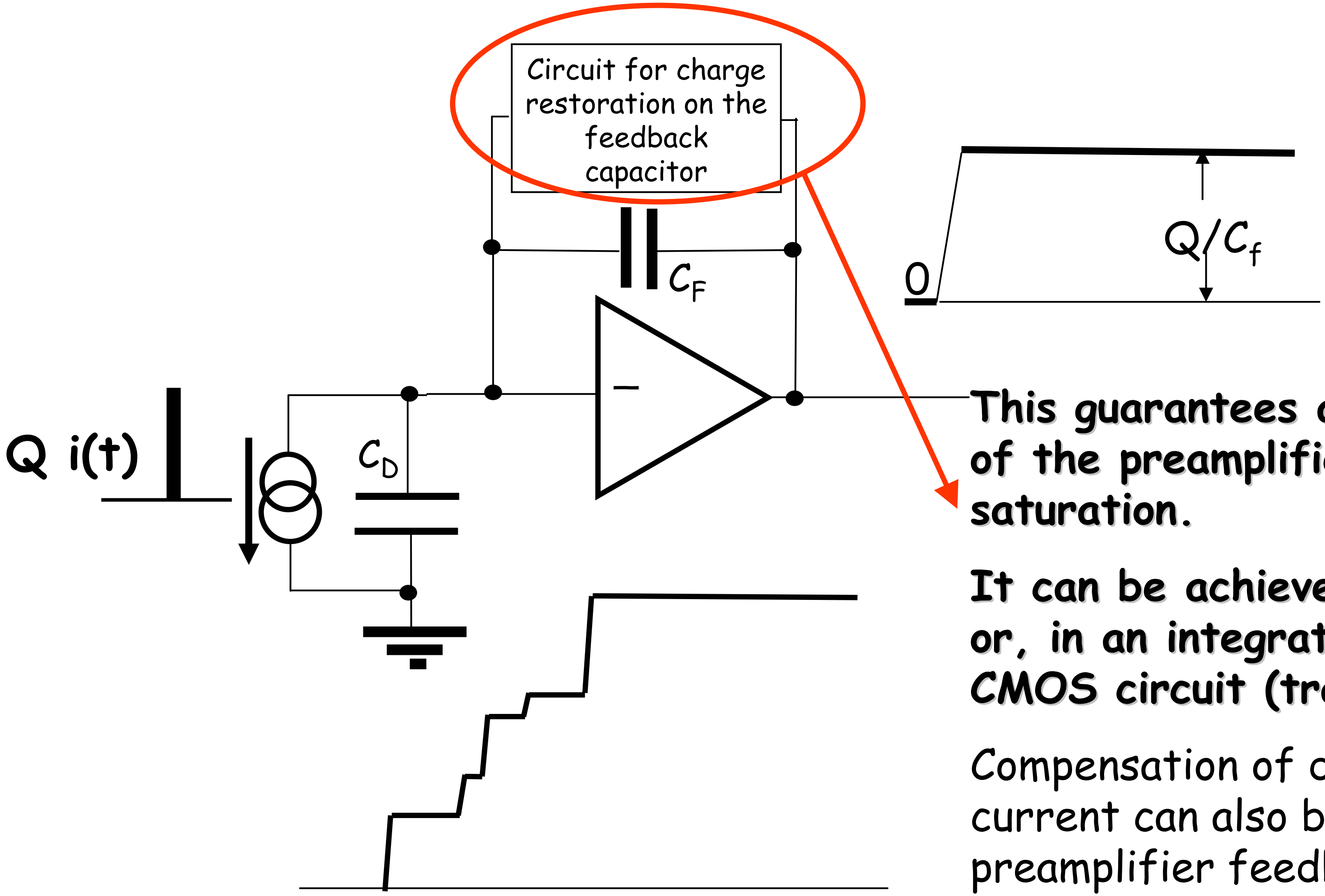
- The detector signal is a current pulse i(t) of short duration
- The physical quantity of interest is the deposited energy, so one has to integrate the sensor signal



$$E_S \div Q_S = \int i(t)dt$$

- The detector capacitance C_D is dependent on geometry (e.g. strip length or pixel size), biasing conditions (full or partial depletion), aging (irradiation)
- Use an integrating preamplifier (charge-sensitive preamplifier), so that charge sensitivity ("gain") is independent of sensor parameters

Acquiring the signal from the sensor: the charge-sensitive preamplifier

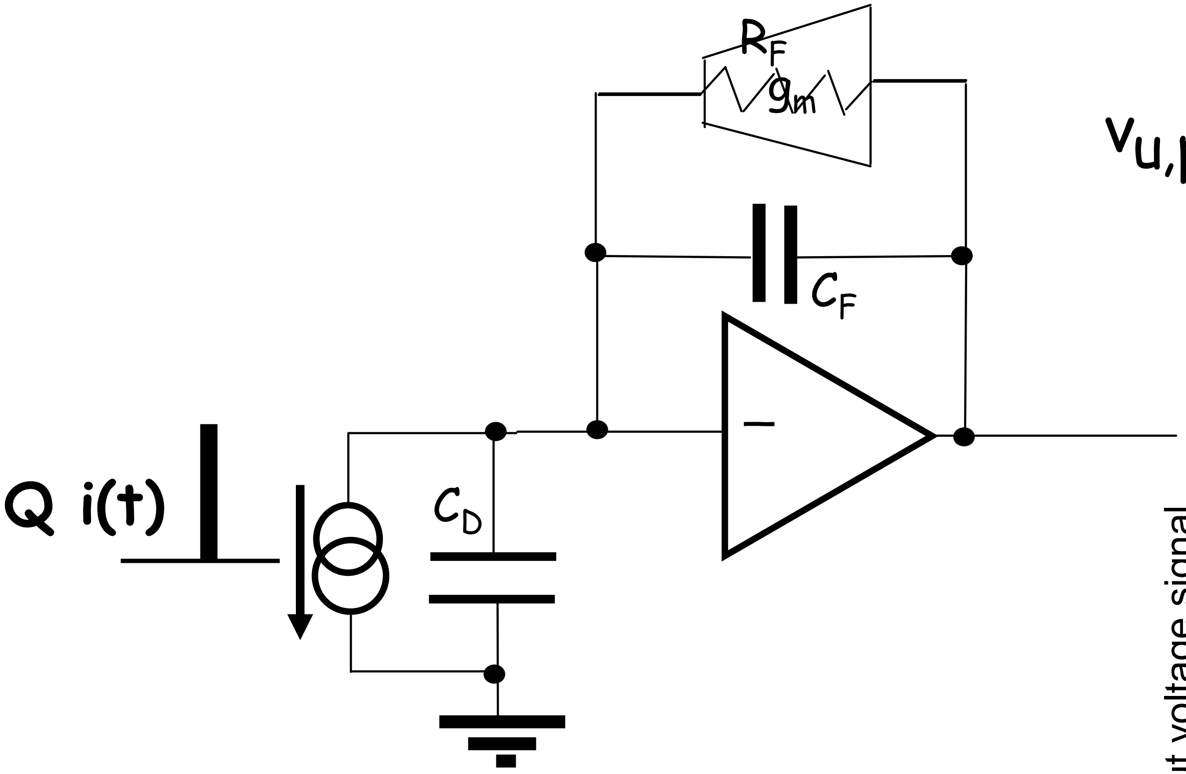


This guarantees a return to baseline of the preamplifier output, avoiding saturation.

It can be achieved with a resistor R_F or, in an integrated circuit, with a CMOS circuit (transconductor).

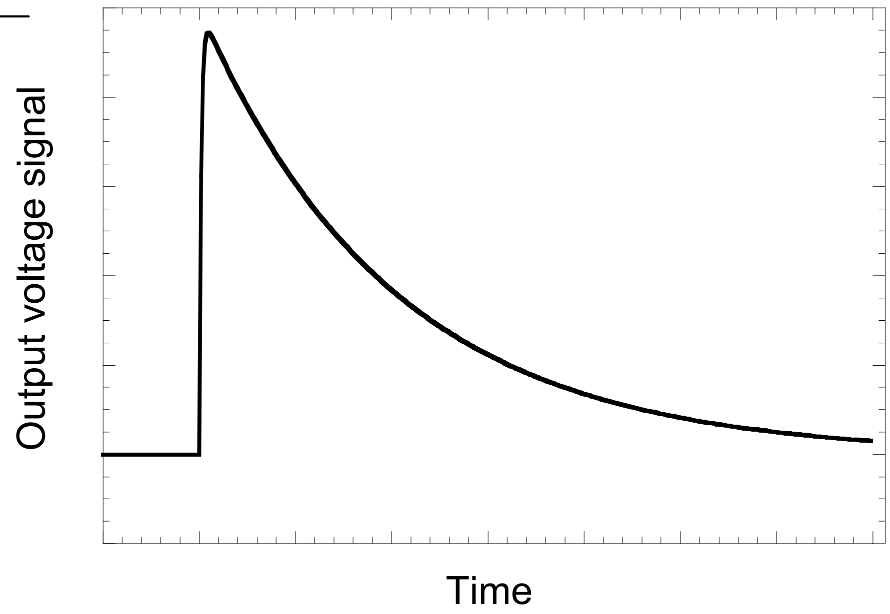
Compensation of detector leakage current can also be performed in the preamplifier feedback (dc coupling)

Acquiring the signal from the sensor: the charge-sensitive preamplifier



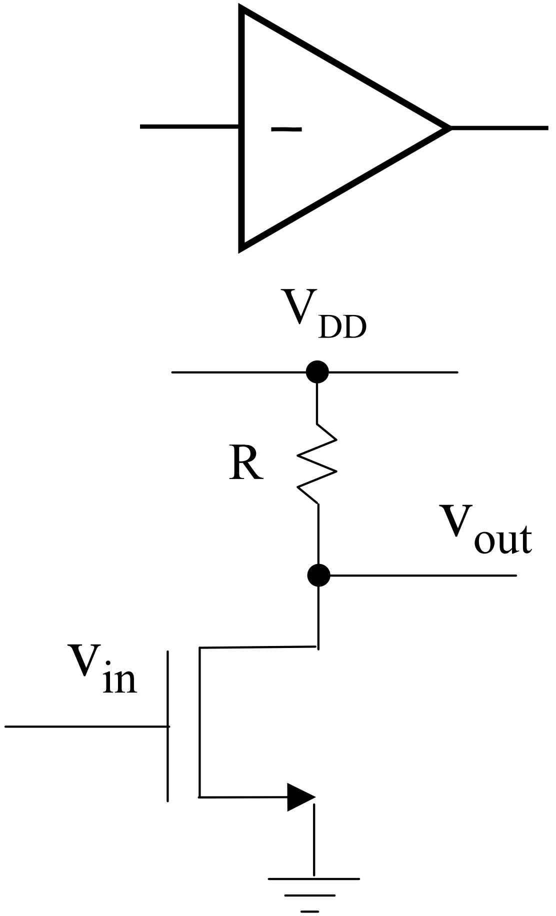
$$v_{u,pre}(t) = \frac{Q}{C_F} e^{-\frac{1}{R_F C_F} t}$$

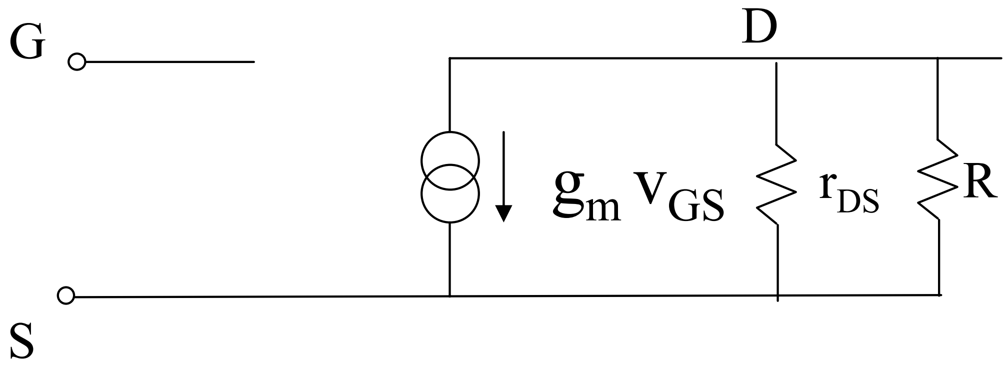
$$v_{u,pre}(t) = \frac{Q}{C_F} e^{-\frac{g_m}{C_F} t}$$



Forward gain stage: CMOS version

- The forward gain stage is an inverting amplifier which can be based on the common source configuration





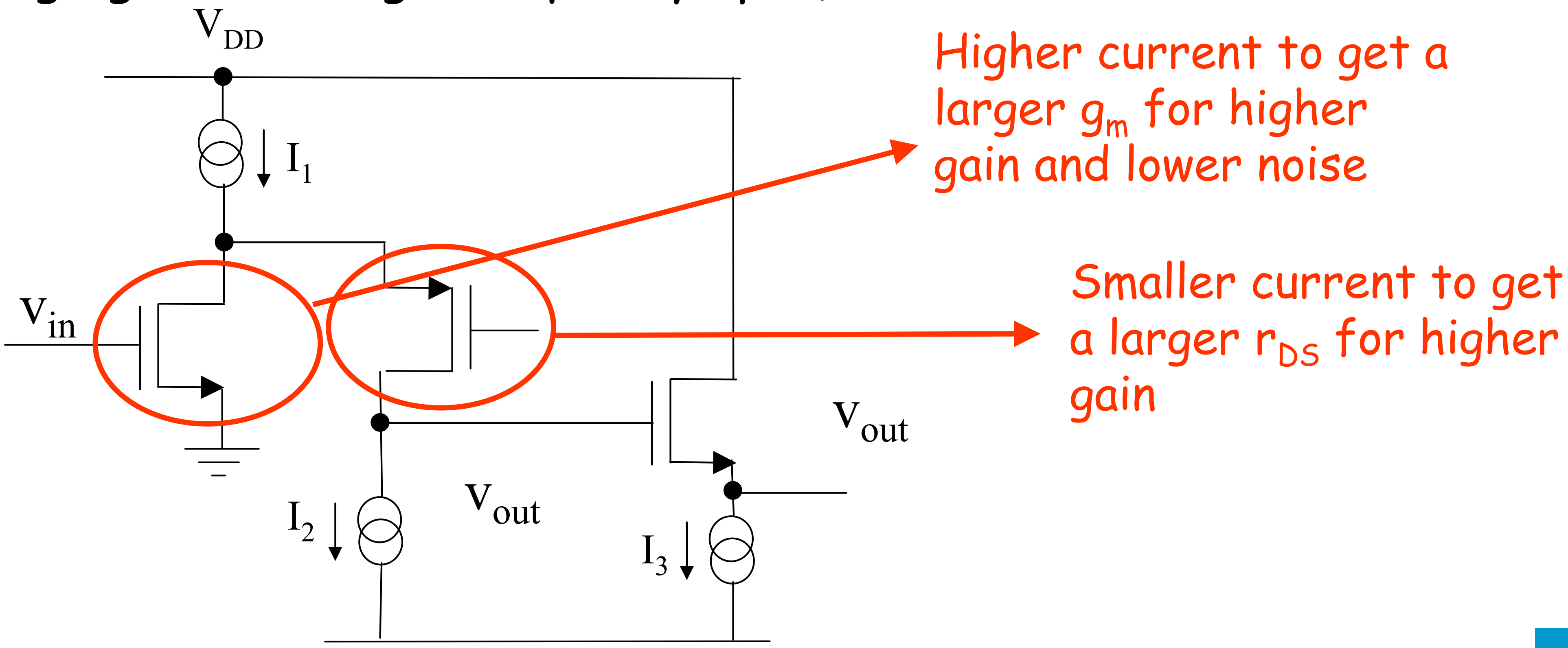
$$\frac{v_{out}}{v_{in}} = -g_m \left(r_{DS} \,//\, R \right)$$

$r_{DS} \div (I_D)^{-1}$

$r_{DS} \div L$ (device gate length)

Forward gain stage: CMOS version

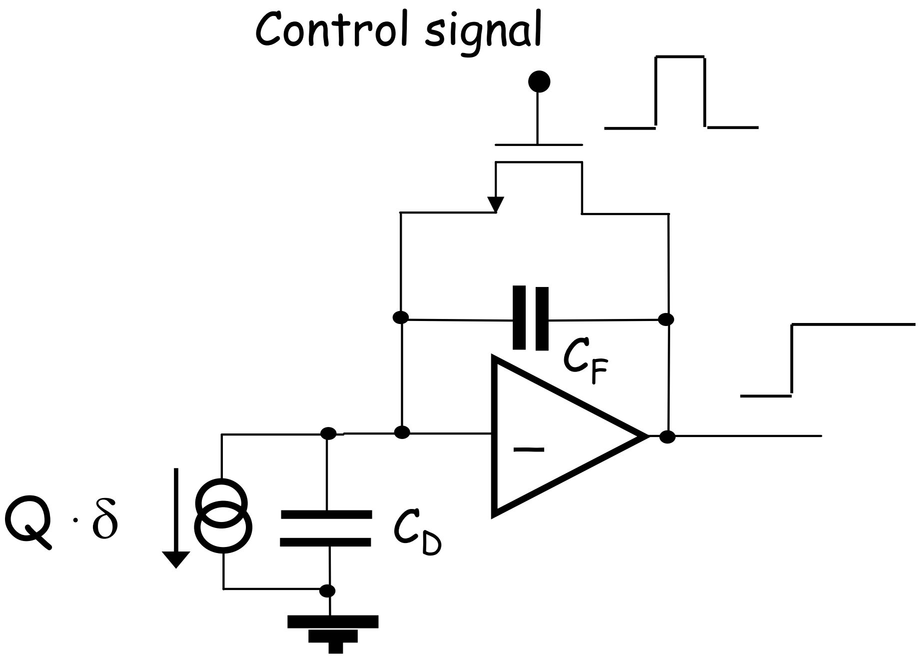
- A higher forward gain can be achieved with a folded cascode configuration. A smaller current in the cascode branch makes it possible to achieve a high output impedance.
- An output source follower can be used to reduce capacitive loading on the high impedance node and increase the frequency bandwidth (high gain in a large frequency span)



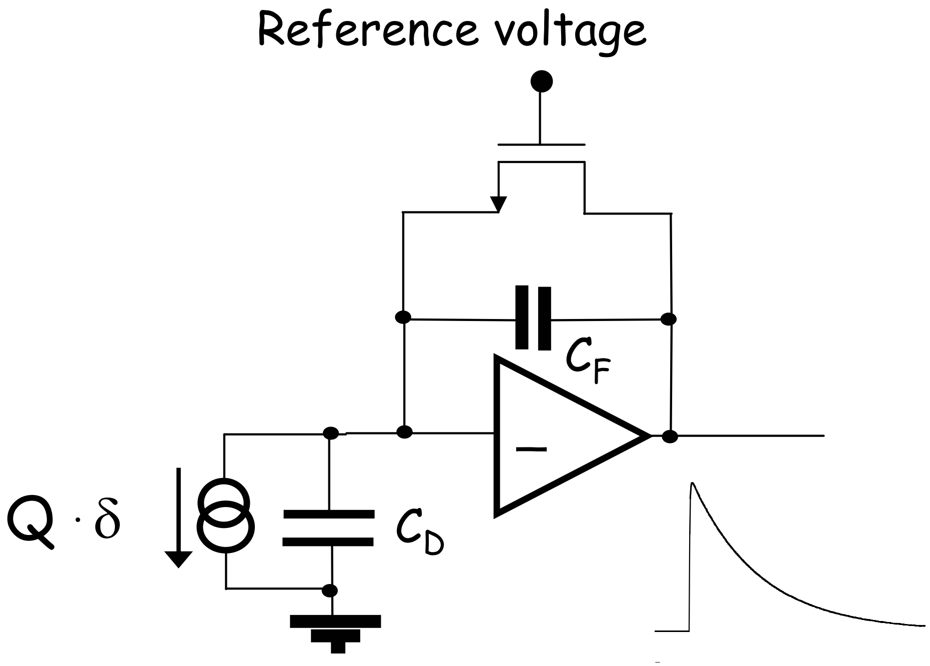
CMOS feedback network

- Single feedback MOSFET

Reset switch



Linear resistor



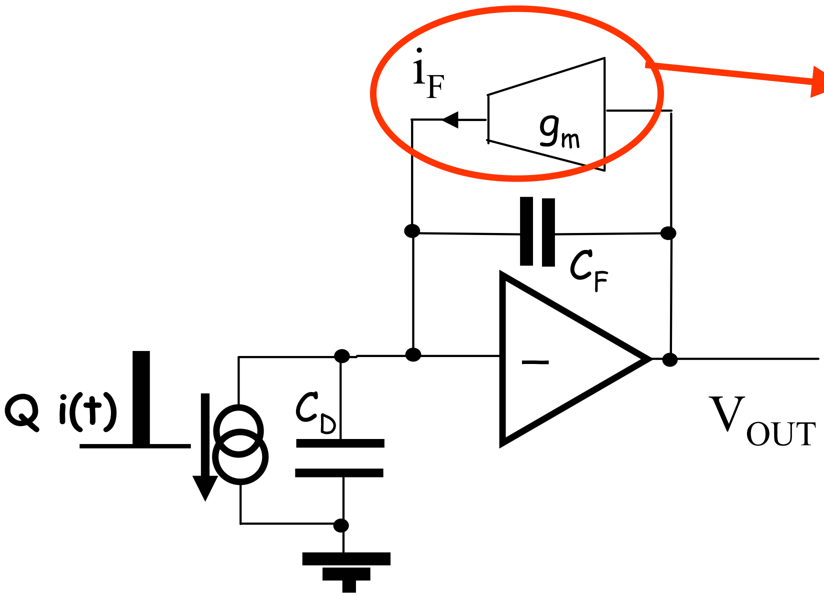
Can be used when you can reset the preamp at fixed times

$$R_{ON} = \frac{L}{W} \frac{1}{\mu_N C_{OX} (V_{GS} - V_T)}$$

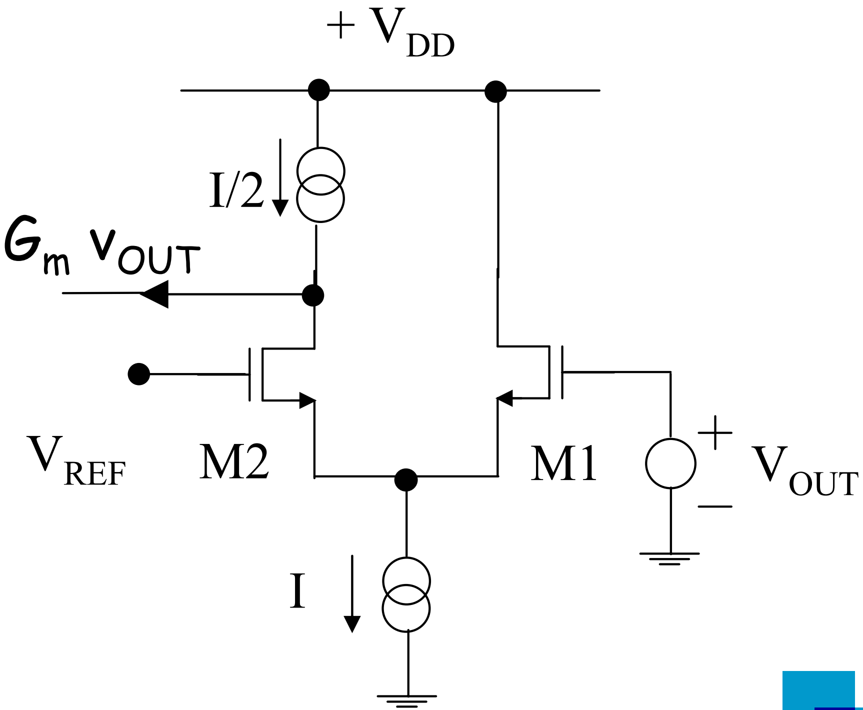
CMOS feedback network

- A large feedback resistor is needed for low noise, since $\frac{\overline{di_R^2}}{df} = \frac{4kT}{R}$

- It is difficult to fabricate a large physical resistor in monolithic form, or to effectively control the resistance of a MOSFET biasd in the linear region
- A large resistor can be simulated by a CMOS circuit, such as a transconductor, which can be considered to be equivalent to a resistor $R = 1/G_m$

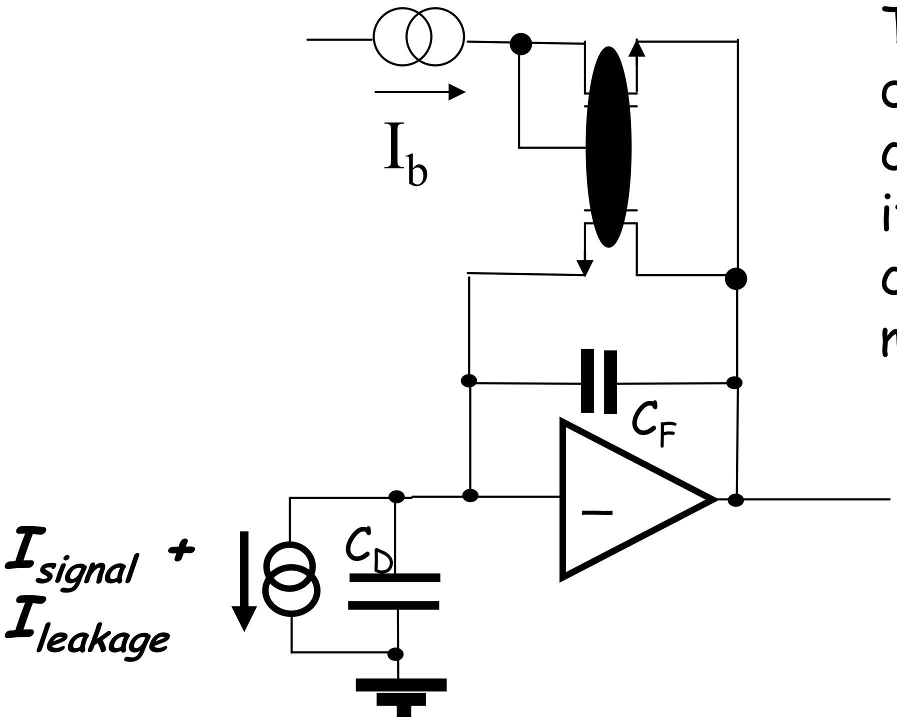


$$i_F = (g_m/2)v_{OUT} = G_m\, v_{OUT}$$

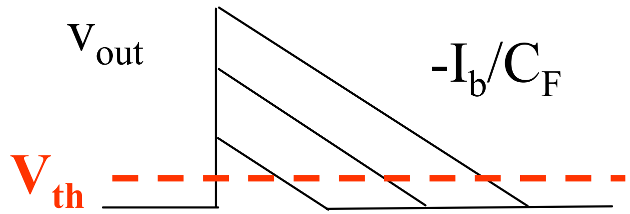


Compensation of detector leakage current

- Irradiated, dc-coupled pixel sensors may have a considerable leakage current, which may saturate the feedback transconductor or, flowing in the feedback resistor, considerably affect the dc voltage at the preamplifier output.
- A CMOS circuit can be designed to accomodate for this leakage current. A popular solution is the following:



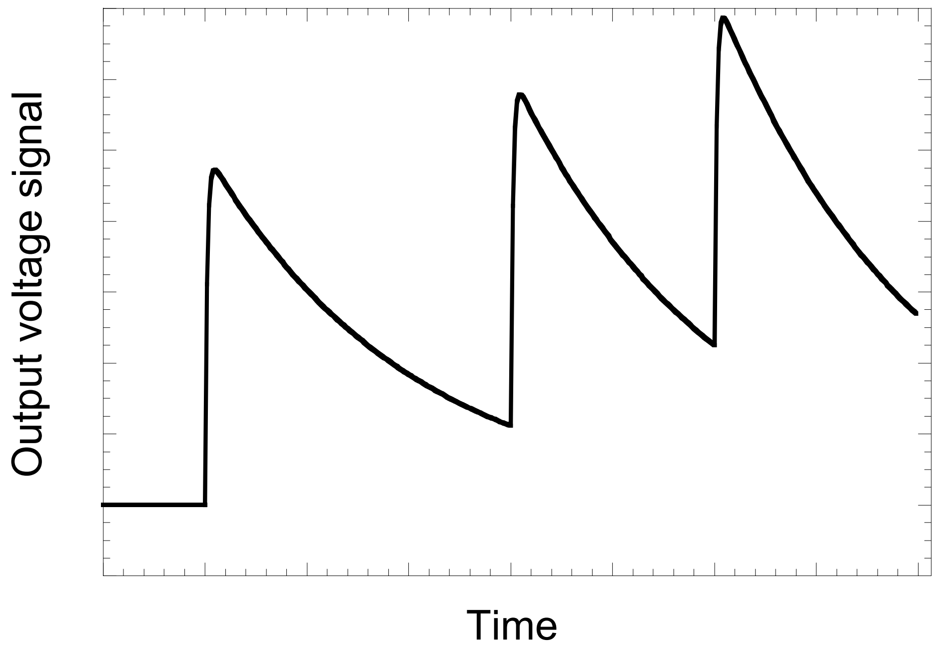
The feedback capacitor is discharged linearly by a constant current. The output signal lends itself to an amplitude-to-time conversion (time-over threshold measurement).



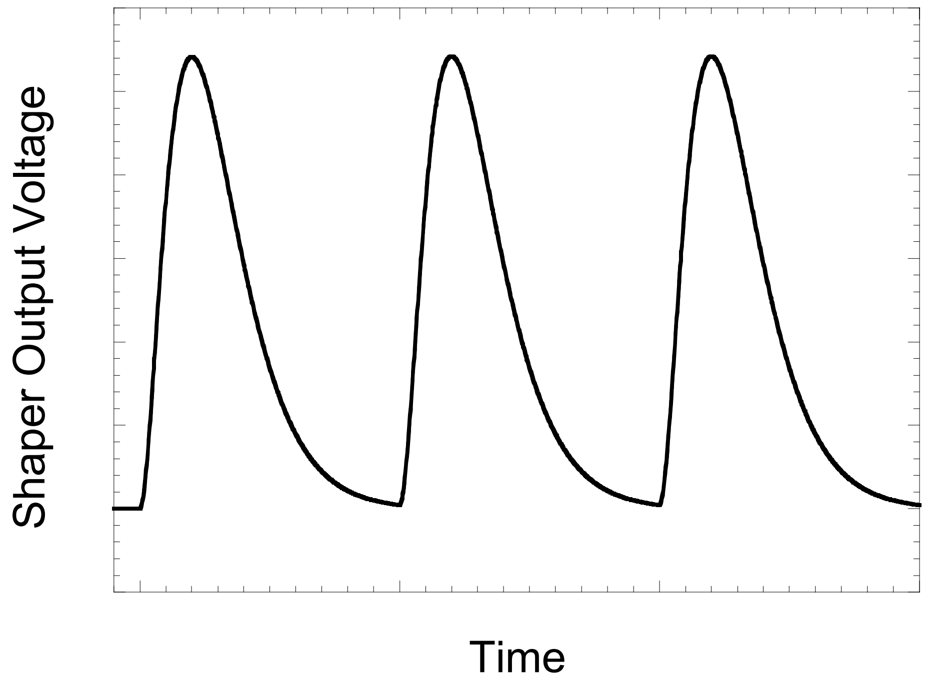
Processing the signal from the sensor: the shaper/filter

- Signal shaping: the voltage step at the preamplifier output has to be constrained to a finite duration to avoid pileup of successive signals

Preamplifier output

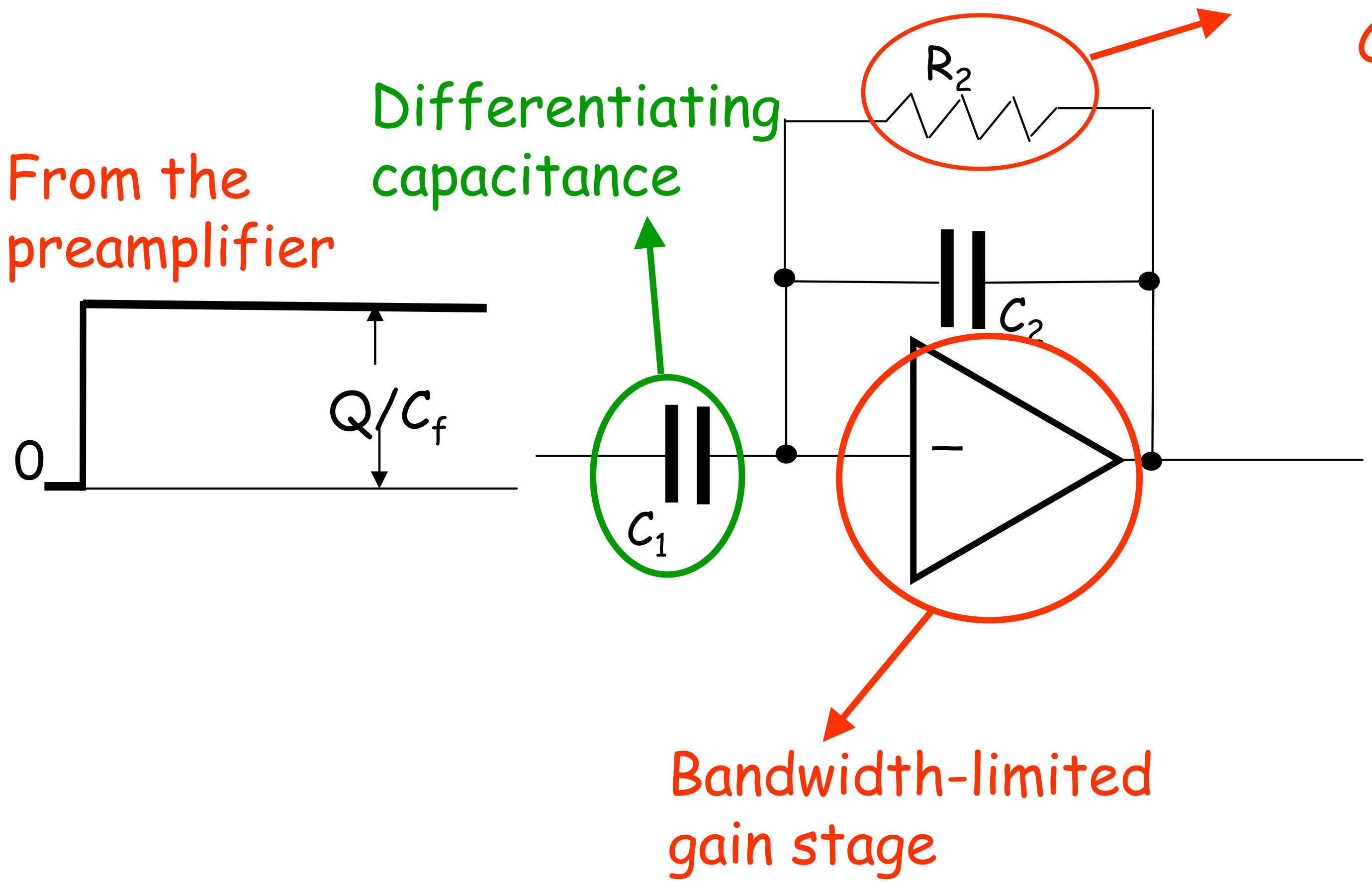


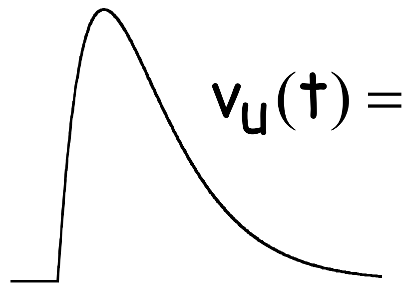
Shaper output



Processing the signal from the sensor: the shaper/filter

- A unipolar "semigaussian" shaper can be built with 1 differentiator (high pass) and n integrators (low-pass).
- This is a compact (n=1) implementation:



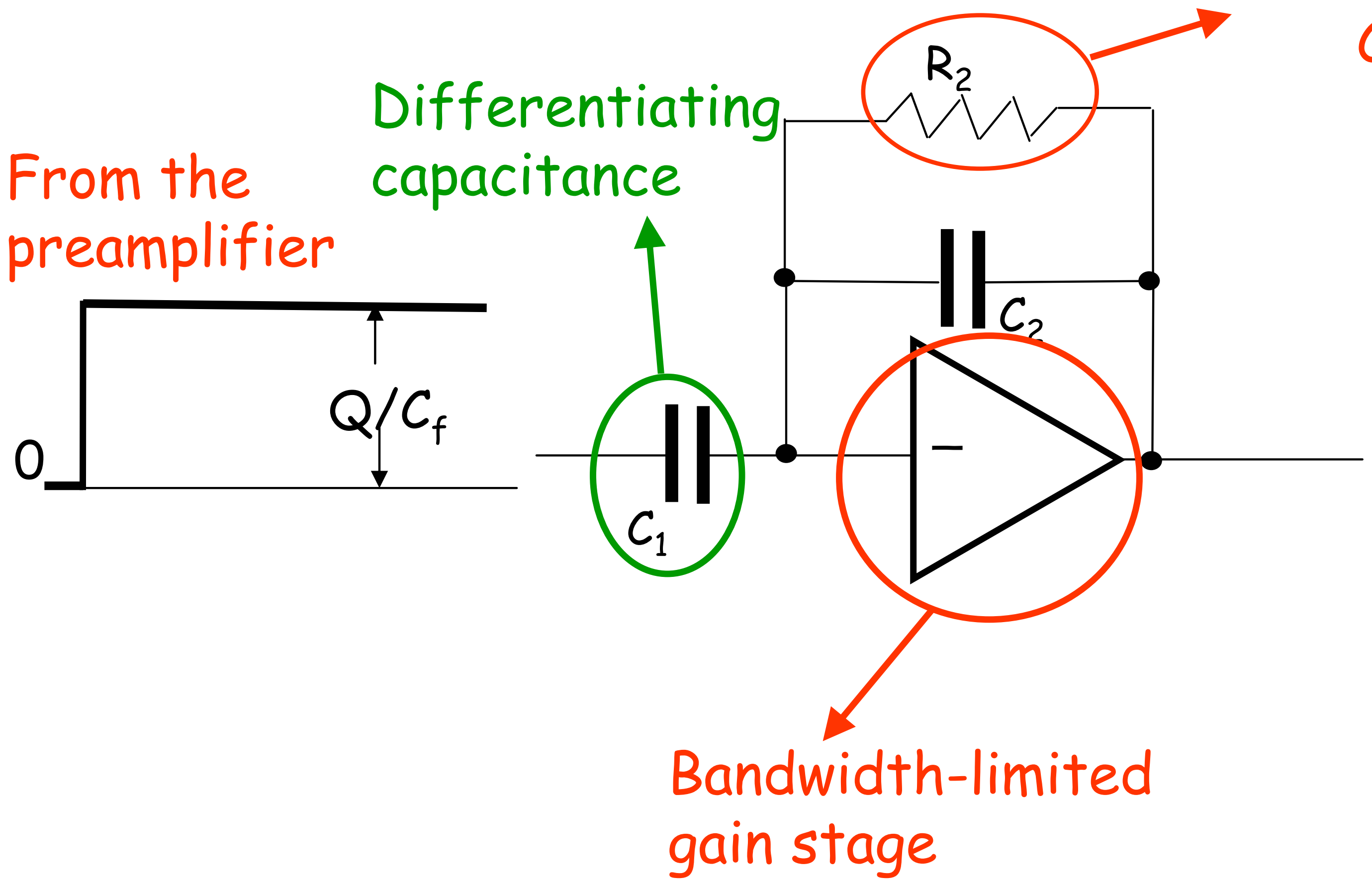


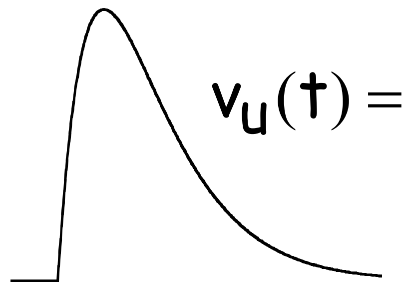
$$v_u(t) = A\frac{Q}{C_F}\frac{t}{\tau}e^{-\frac{t}{\tau}}$$

For correct values of the time constants associated to the feedback network and to the gain stage, the transfer function has two coincident poles

Processing the signal from the sensor: the shaper/filter

- A unipolar "semigaussian" shaper can be built with 1 differentiator (high pass) and n integrators (low-pass).
- This is a compact (n=1) implementation:





$$v_u(t) = A \frac{Q}{C_F} \frac{t}{\tau} e^{-\frac{t}{\tau}}$$

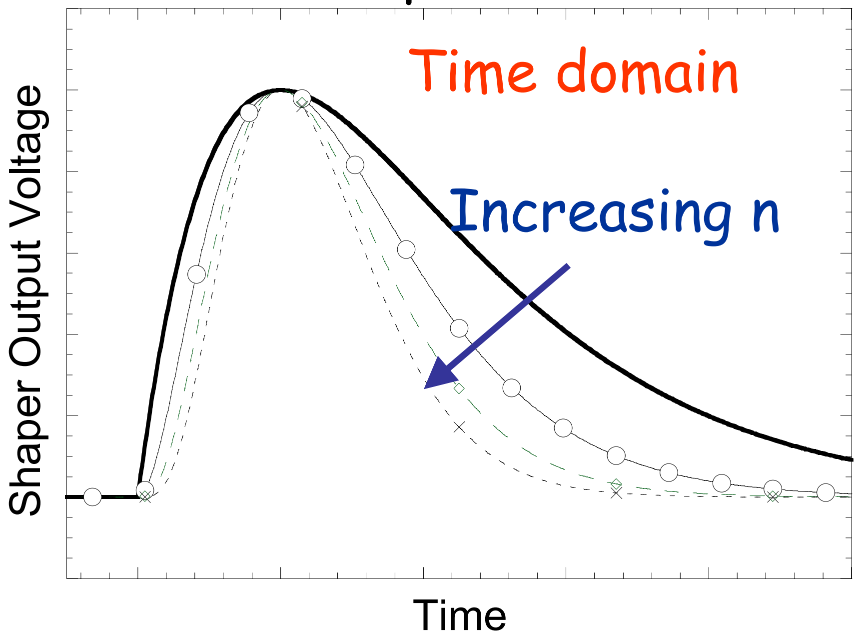
$$T(s) \div \frac{s\tau}{(1+s\tau)^2}$$

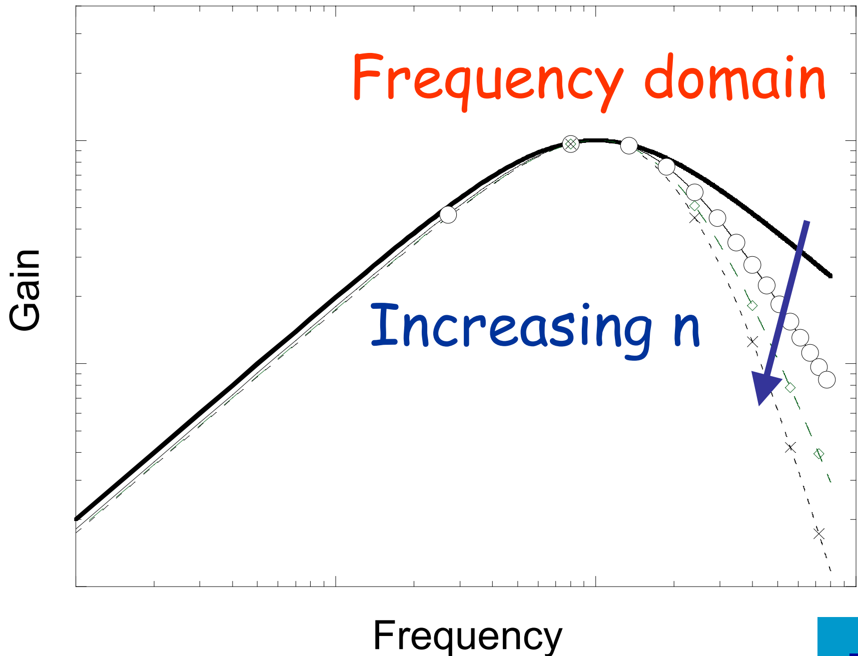
Processing the signal from the sensor: the shaper/filter

- In the AToM (BaBar) and FSSR2 (BTeV) chips (microstrip trackers), a second order (n=2) shaper was implemented with an additional integrator before the shaper.
- For an n^{th}-order unipolar shaper (higher n: more symmetrical pulse, higher signal rates for the same peaking time):

$$v_u(t) = A\frac{Q}{C_F}\left(\frac{t}{\tau}\right)^n e^{-\frac{t}{\tau}}$$

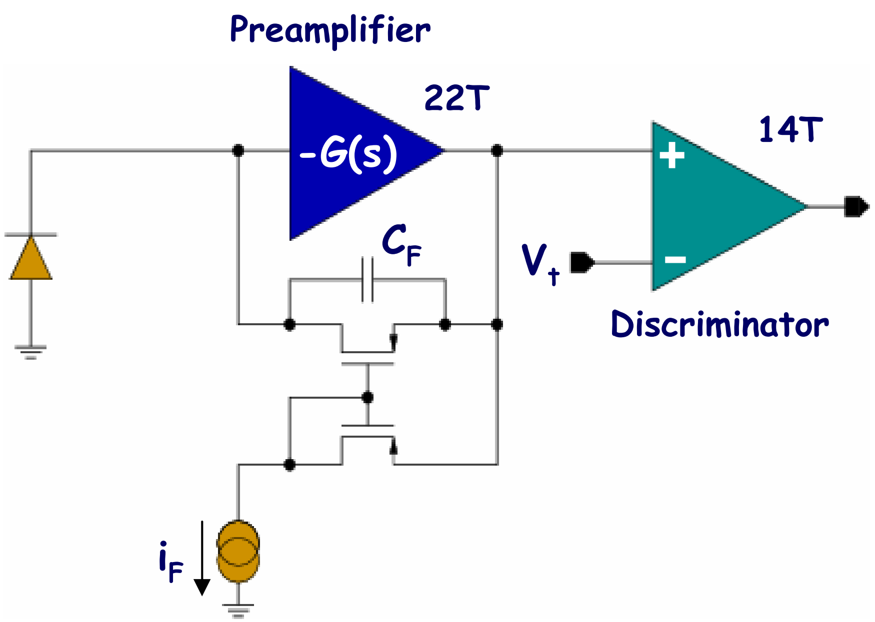
$$T(s) \div \frac{s\tau}{(1+s\tau)^n}$$



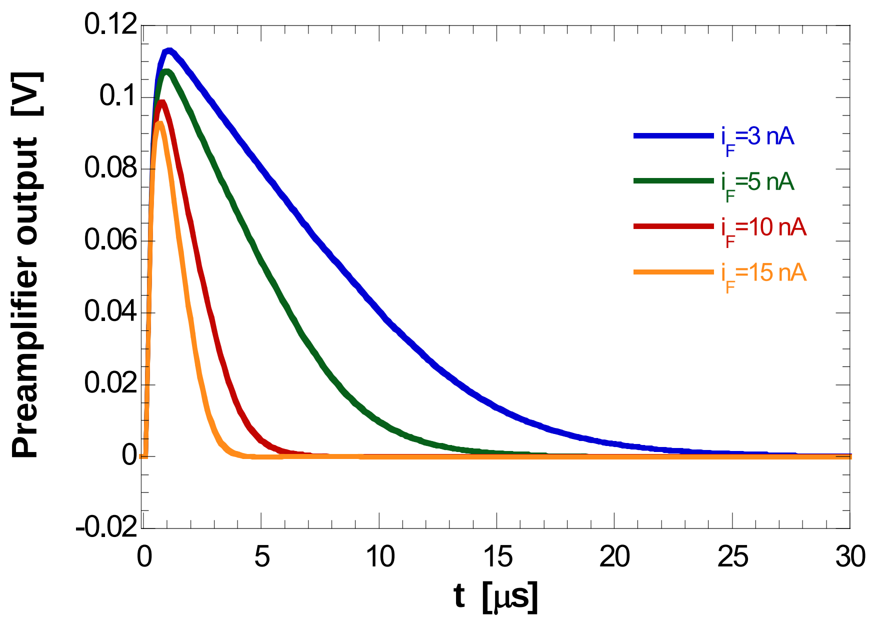


"Shaperless" analog channel

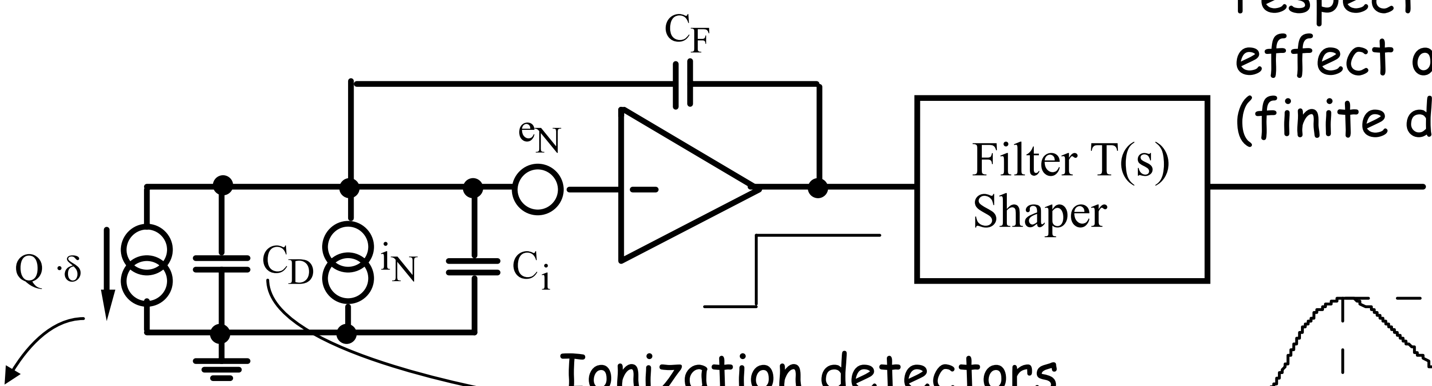
- In future experiments, very small pixels will be needed (< 20x20 μm^2 for ILC VTX) with no room in the pixel for a shaper
- Under these constraints, a viable solution consists in artificially reducing the preamplifier bandwidth



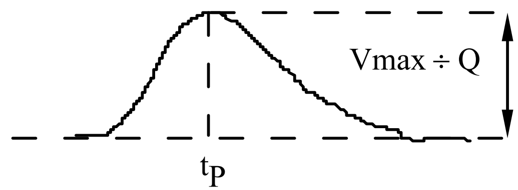
Preamplifier response to an 800 e^- pulse



Charge measuring system and the effect of noise



Filter minimizes the measurement error with respect to noise and the effect of pulse overlap (finite duration)



Charge collection is very fast in semiconductor detectors

Ionization detectors can be modeled as capacitive signal sources

Noise arises from two uncorrelated sources at the input (series and parallel noise):

$$S_{e_N}(\omega) = A_W + \frac{A_f}{f} \qquad S_{I_N}(\omega) = B_W$$

Noise sources

White series noise

$$A_W = 4kT\frac{\Gamma}{g_m}$$

White noise in the main current (drain, collector) of the input device

other components in the input stage

stray resistances in series with the input

1/f series noise

$$A_{1/f} = \frac{A_f}{f}$$

1/f component in the drain current

White parallel noise

$$B_W = 2qI_{det} + 2qI_{G(B)} + \frac{4kT}{R}$$

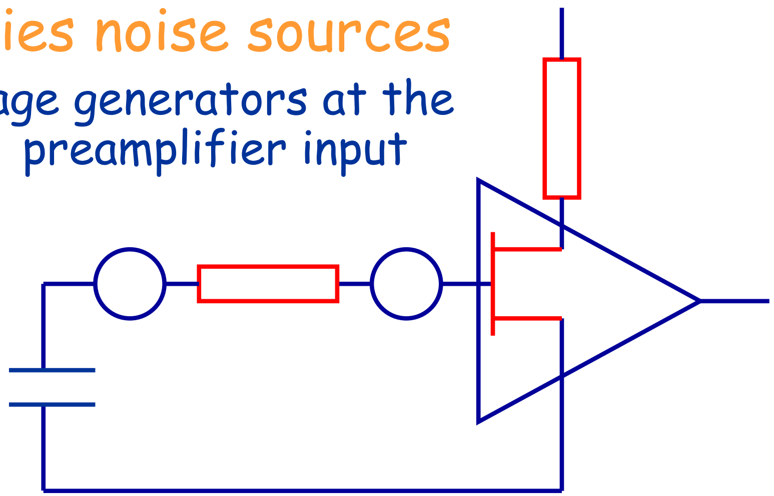
Shot noise in detector leakage current

shot noise in input device gate (base) current

thermal noise in feedback resistor

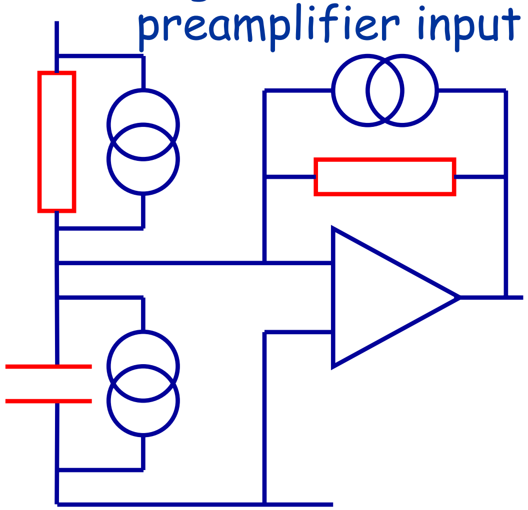
Series noise sources

Voltage generators at the preamplifier input



Parallel noise sources

Current generators at the preamplifier input



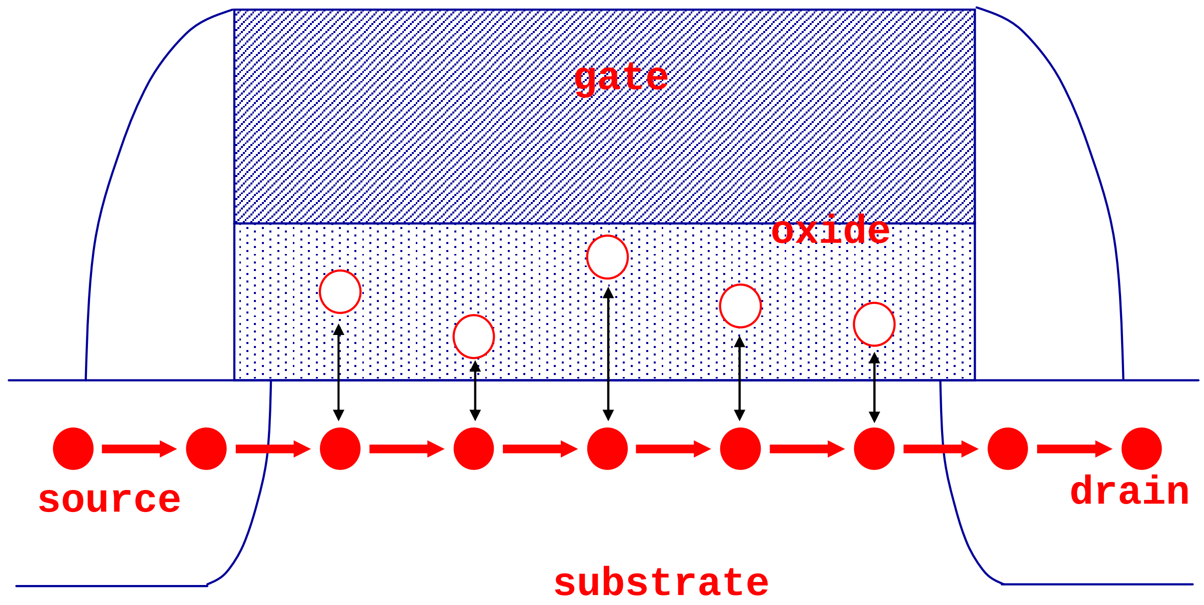
Shot noise

Shot noise is associated to device currents when charge carriers have to cross a potential barrier (P-N junctions in diodes and bipolar transistor)

$$S_I(\omega) = 2qI$$

In irradiated silicon detectors, leakage current and the associated shot noise may strongly increase

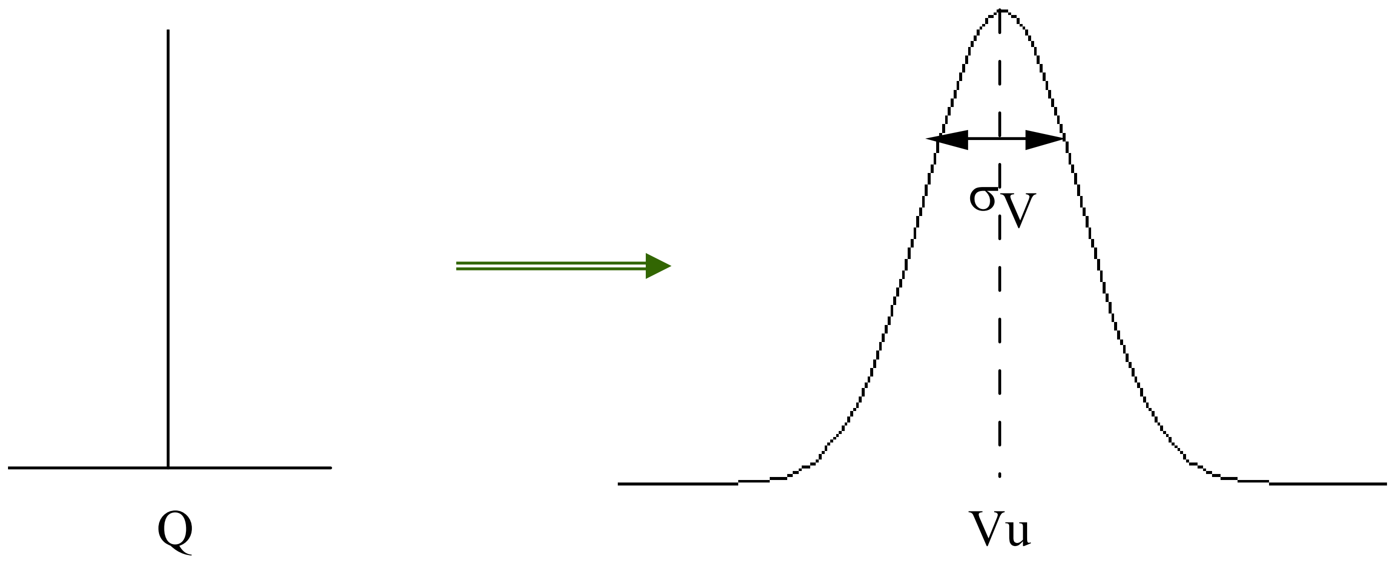
1/f noise



Interaction between charge carriers in the MOSFET channel and traps close to the Si-SiO_2 interface leads to fluctuations in the drain current.

This can be modeled with a noise voltage generator in series with the device gate, with a 1/f spectral density.

Effect of electronic noise on charge measurements

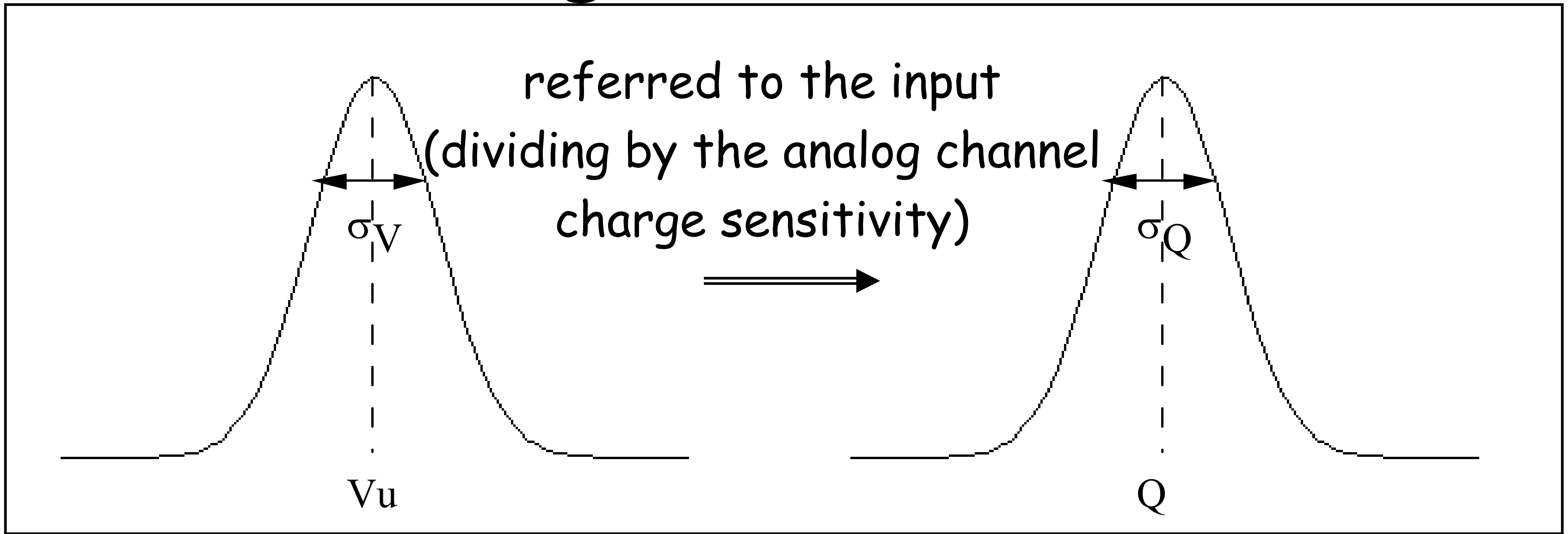


Ideally indefinitely narrow distribution of detector charge (neglecting statistics in energy deposition and charge creation)

Broadening of pulse amplitude distribution at the shaper output due to electronic noise

Because of electronic noise, the signal amplitude at the shaper output has a Gaussian probability density function

Effect of electronic noise on charge measurements



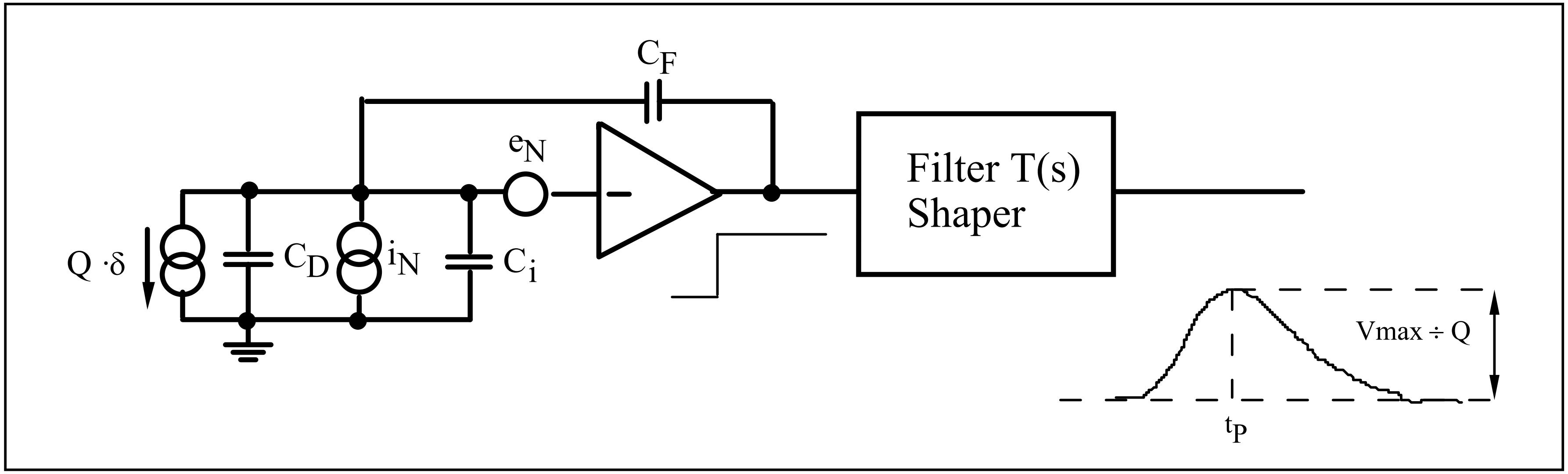
The signal amplitude at the output of the linear analog channel is characterized by a Gaussian probability density function

$$S/N = \frac{V_u}{\sigma_V} = \frac{Q}{\sigma_Q} = \frac{Q}{ENC} = \eta_Q$$

Equivalent Noise Charge = standard deviation in the charge measurement

charge injected at the input producing at the output of the linear processor a signal whose amplitude equals the root mean square output noise

Equivalent Noise Charge (ENC)



The mean square value of the noise voltage at the shaper output can be calculated as follows:

$$\overline{v_{u,N}^2} = \int_0^\infty S_u(\omega)df = \int_0^\infty \left[\left|T_{e_N}(j\omega)\right|^2 \cdot S_{e_N}(\omega) + \left|T_{I_N}(j\omega)\right|^2 \cdot S_{I_N}(\omega) \right] df$$

$$= \int_0^\infty \left[\left|T(j\omega)\right|^2 \cdot \frac{(C_D + C_i + C_F)^2}{C_F^2}\left(A_W + \frac{A_f}{f}\right) + \left|T(j\omega)\right|^2 \frac{1}{\omega^2 C_F^2} \cdot B_W \right] df =$$

Equivalent Noise Charge (ENC)

$$= A_W \frac{(C_D + C_i + C_F)^2}{C_F^2} \frac{1}{2\pi} \int_0^{\infty} |T(j\omega)|^2 d\omega +$$

$$+ A_f \frac{(C_D + C_i + C_F)^2}{C_F^2} \int_0^{\infty} \frac{|T(j\omega)|^2}{\omega} d\omega + B_W \frac{1}{C_F^2} \frac{1}{2\pi} \int_0^{\infty} \frac{|T(j\omega)|^2}{\omega^2} d\omega$$

$$\frac{1}{2\pi} \int_0^{\infty} |T(j\omega)|^2 d\omega = \frac{A_1}{t_P}$$

t_P = peaking time of the signal at the shaper output

$$\int_0^{\infty} \frac{|T(j\omega)|^2}{\omega} d\omega = A_2$$

A_1, A_2, A_3 = filter-dependent coefficients

$$\frac{1}{2\pi} \int_0^{\infty} \frac{|T(j\omega)|^2}{\omega^2} d\omega = A_3 t_P$$

Equivalent Noise Charge (ENC)

$$ENC = \frac{\sqrt{\overline{v_{u,N}^2}}}{Charge \quad sensitivity}$$

$$ENC^2 = \overline{v_{u,N}^2} \cdot C_F^2 = A_W (C_D + C_i + C_F)^2 \frac{A_1}{t_P} + A_f (C_D + C_i + C_F)^2 A_2 + B_W A_3 t_P$$

$C_T = C_D + C_i + C_F$
= total capacitance at the preamplifier input

In a well designed preamplifier, the noise is determined by the input device.

Equivalent Noise Charge (ENC)

$$ENC^2 = A_W C_T^2 \frac{A_1}{t_P} + A_f C_T^2 A_2 + B_W A_3 t_P$$

White series noise:

Neglecting noise in parasitic resistors:

$$A_W = 4kT \frac{\Gamma}{g_m}$$

$\Gamma = 0.5$ (BJT)

$\Gamma = 2/3$ (Long channel FETs)

$\Gamma \approx 1$ (Short-channel FETs)

White parallel noise:

$$B_W = 2qI$$

$I = I_B$ (BJT)

$I = I_G$ (gate tunneling current in nanoscale CMOS)

$I = I_{leak}$ Detector leakage current

Equivalent Noise Charge (ENC)

$$ENC^2 = A_W C_T^2 \frac{A_1}{t_P} + A_f C_T^2 A_2 + B_W A_3 t_P$$

Series 1/f noise (MOSFET):

$$A_f = \frac{K_f}{C_{ox} WL}$$

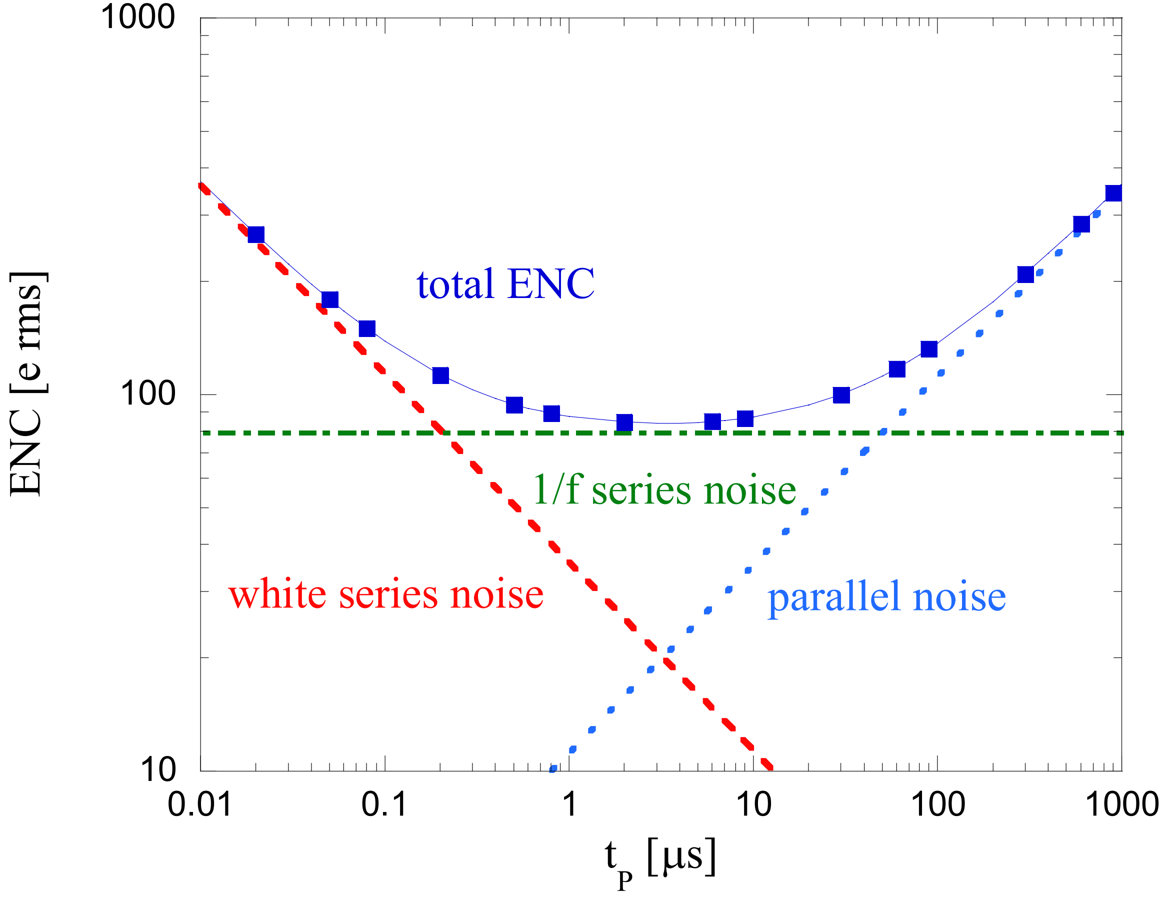
K_f: 1/f noise parameter; depends on the gate oxide quality

C_{ox}: Oxide capacitance per unit gate area

WL: Transistor geometry (gate Width and Length)

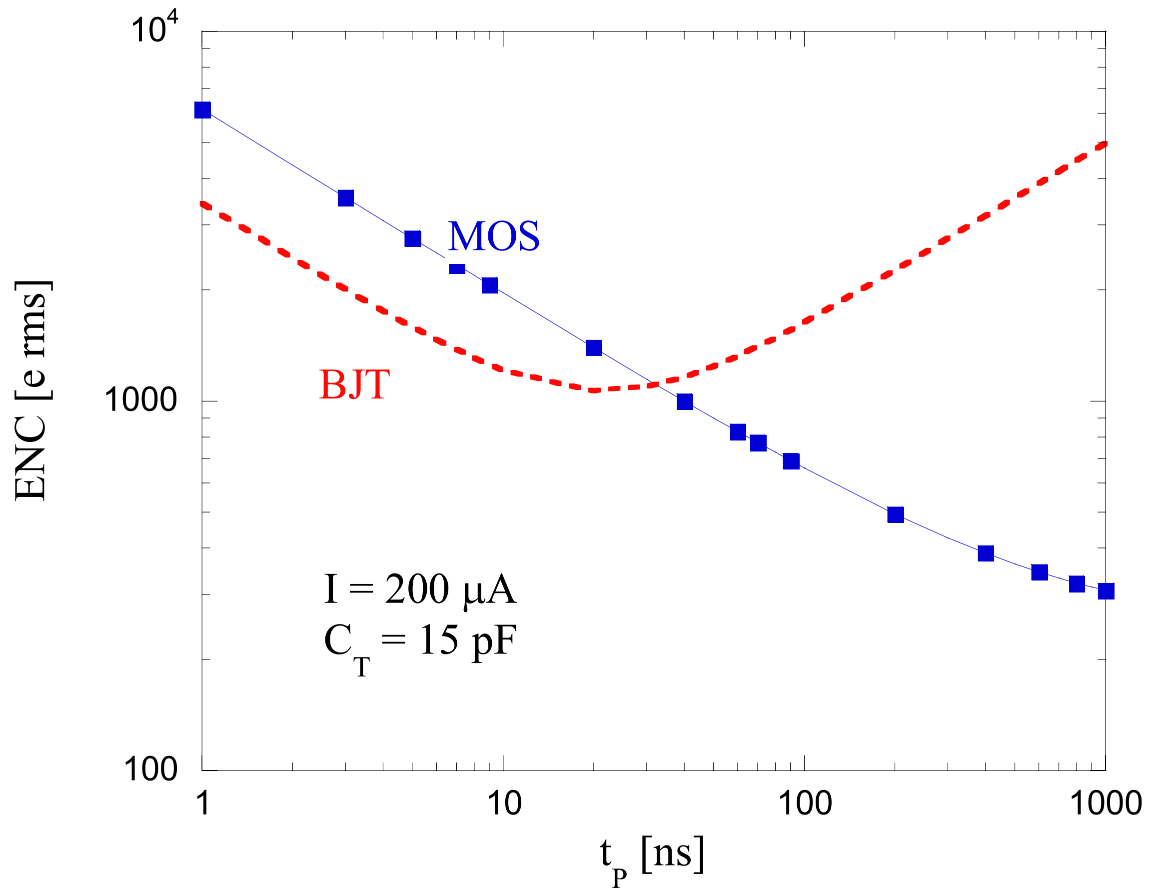
The ENC contribution from 1/f noise is independent of the peaking time of the signal at the shaper output; it is weakly dependent on the shape of the transfer function of the shaper.

- In trackers for high luminosity colliders, event rate is very high, and the peaking time has to be short (< 100 ns).
- White series noise is usually dominant here, except with irradiated sensors, where leakage current (and the associated shot noise) may increase to a very large extent.

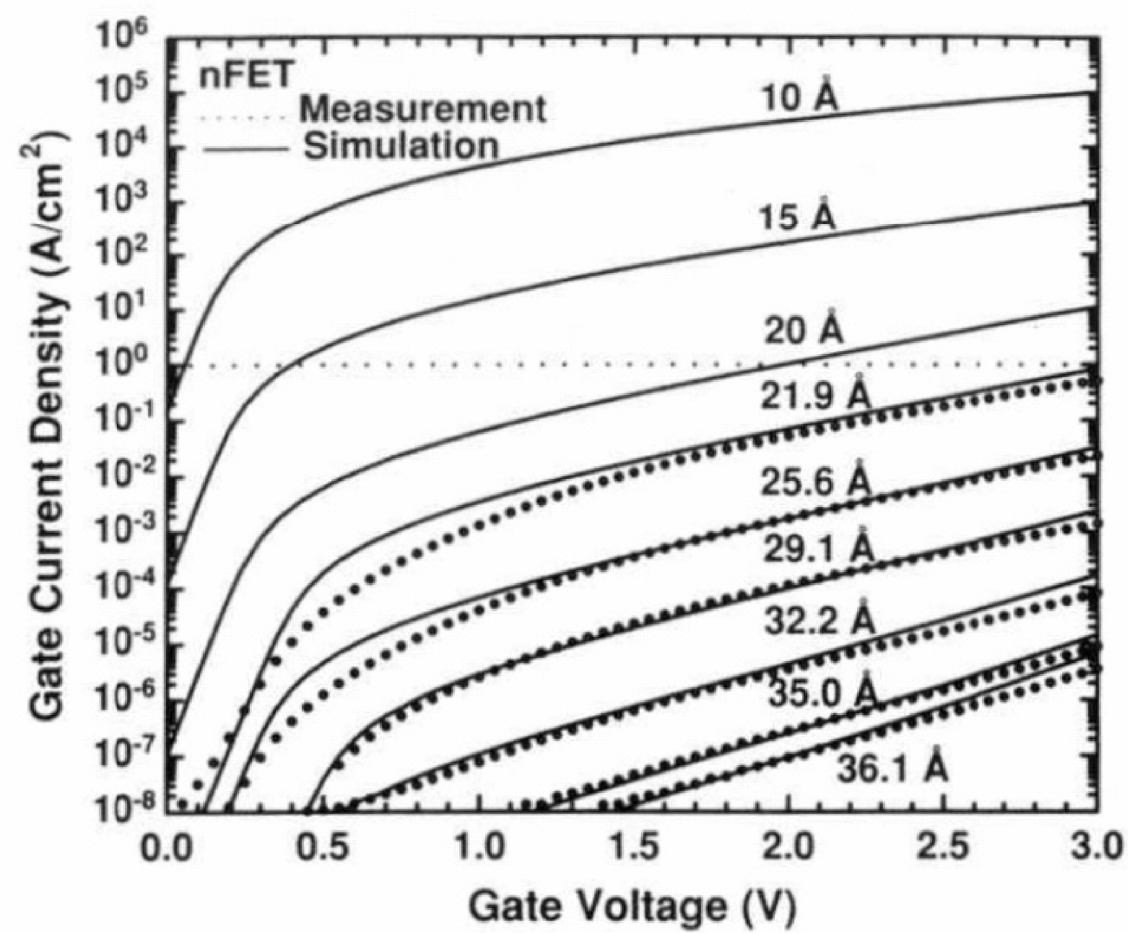


ENC: BJT vs MOSFET

- Bipolar transistors have a larger g_m/I ratio with respect to MOSFET, which means a lower series white noise for a same current
- BiCMOS (SiGe) technology are an appealing alternative for fast readout systems; since they are less dense than CMOS, their use is limited to strip front-end chips



Gate leakage current shot-noise in nanoscale CMOS



$$S_{IG}(f) = 2qI_G$$

90 nm CMOS process:

- Current density = 1 A/cm^2
- W = 1000 μm
- L = 0.1 μm

$\Rightarrow I_G = 1\mu A$

$\Rightarrow S_{IG} = 2qI_G = 0.56\ pA/\sqrt{Hz}$

Non negligible noise contribution

Rad-hard, low-noise charge preamplifier design: short strip readout with 90 nm electronics, NMOS input

$$ENC^2 = \left(A_W \frac{A_1}{t_P} + \frac{K_f}{C_{OX} WL} A_2 \right) C_T^2 + 2qI_G \cdot A_3 \cdot t_P$$

White noise — 1 / f noise — Parallel noise

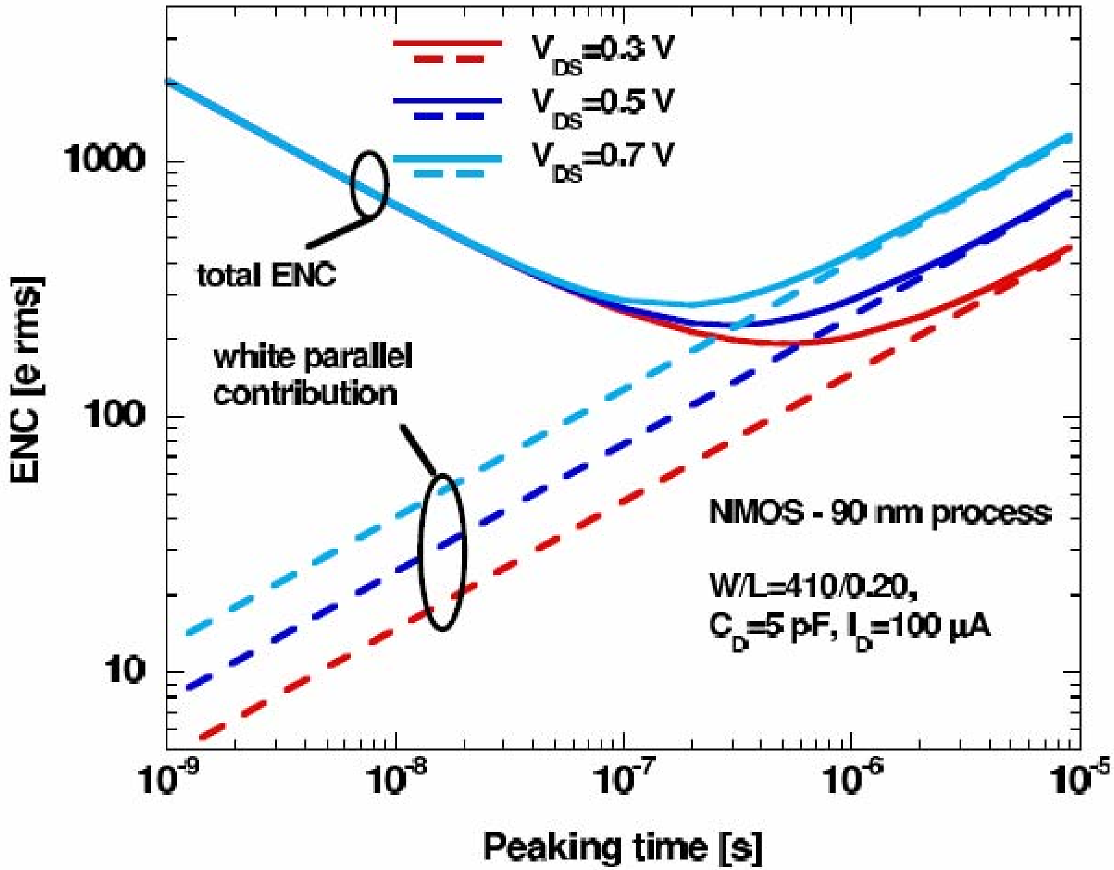
- CMOS looks not too different from bipolar transistors
- Weak inversion region: $g_m = \frac{I_D}{nV_T}$

  (n =1.2 in 100-nm scale CMOS, n=1 in bipolar transistors)

  $\Rightarrow$ Expect ~ 20% higher ENC contribution from white series noise for the same device current

$$A_W = n\frac{2kT}{g_m} = n^2 2kT\frac{V_T}{I_D}$$

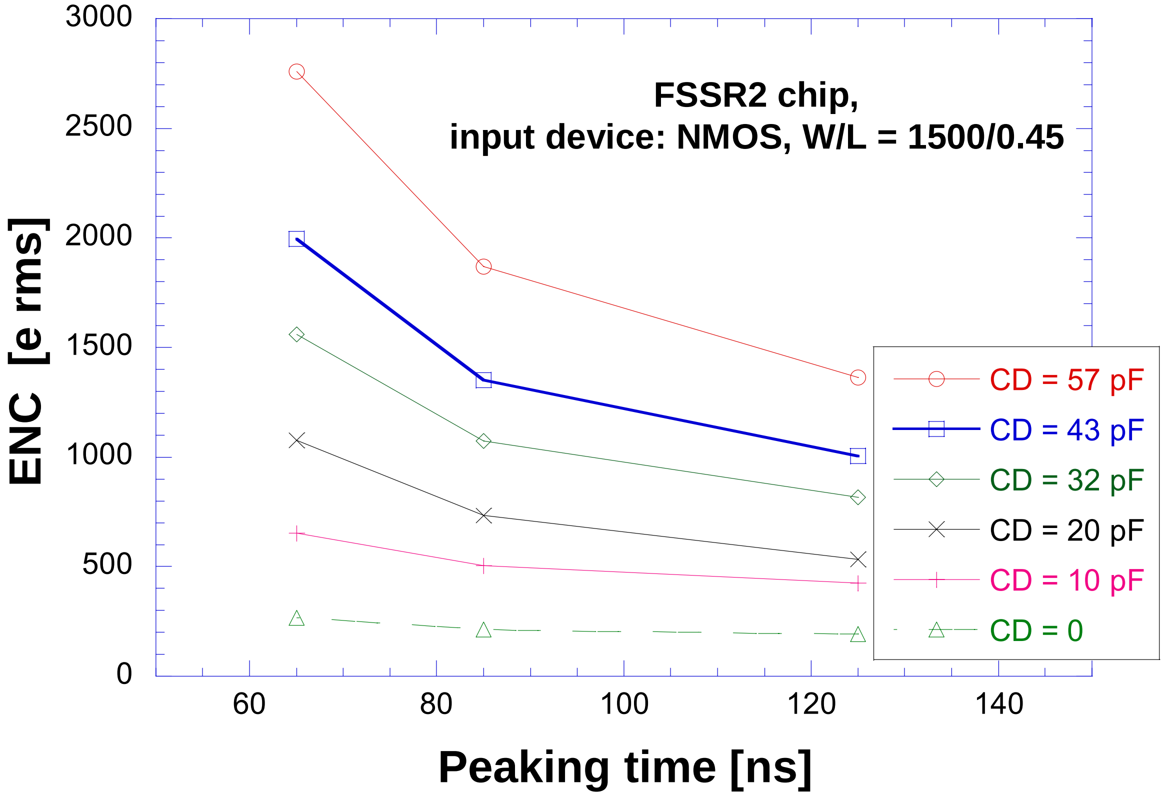
- Series white noise is dominant at $t_P < 100$ ns

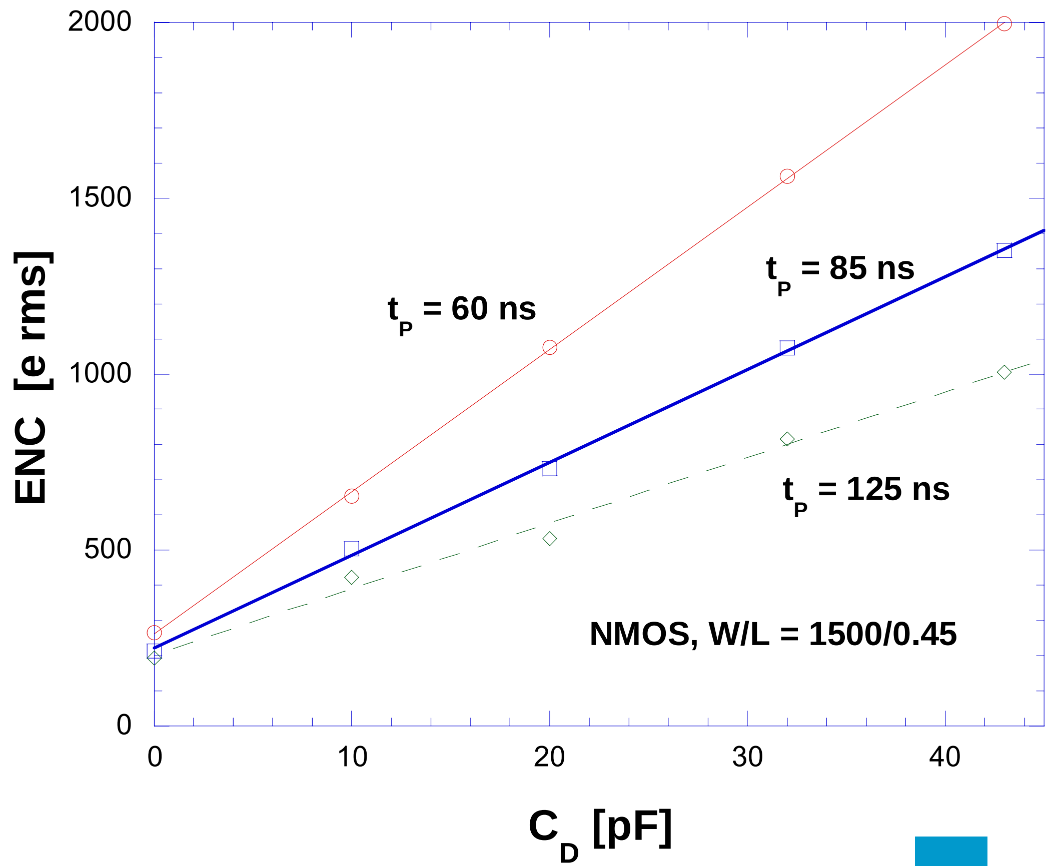


Noise and detector capacitance

- White and 1/f series noise terms (dominant in CMOS) give a contribution to ENC linearly increasing with the detector capacitance ($C_T = C_D + C_{IN} + C_F$).

$$ENC^2 = \left(A_W \frac{A_1}{t_P} + \frac{K_f}{C_{OX} W L} A_2 \right) C_T^2$$





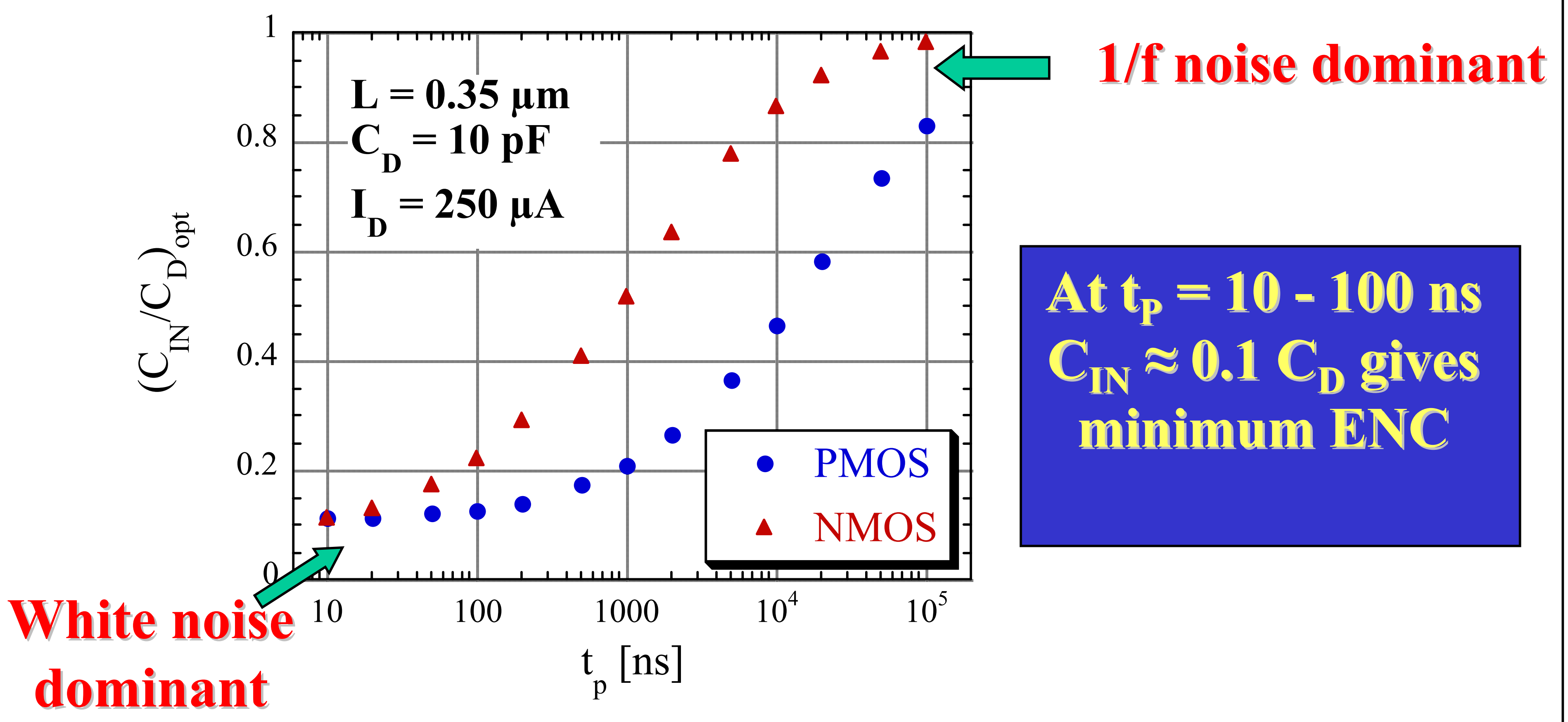
Capacitive matching

- It is possible to minimize ENC by a correct choice of the dimensions of the preamplifier input device (gate width W and length L)

- Conditions for optimum matching between the preamplifier input capacitance ($C_{IN} = C_{OX}WL$) and the detector capacitance C_D depend on the input device operating region (most often, weak or moderate inversion) and on which series noise contribution is dominant (white or 1/f)

- This optimization has to comply with constraints on the power dissipation, which limit the drain current in the input device (in weak inversion, $A_W \div 1/g_m \div 1/I_D$)

Capacitive matching in a deep submicron technology

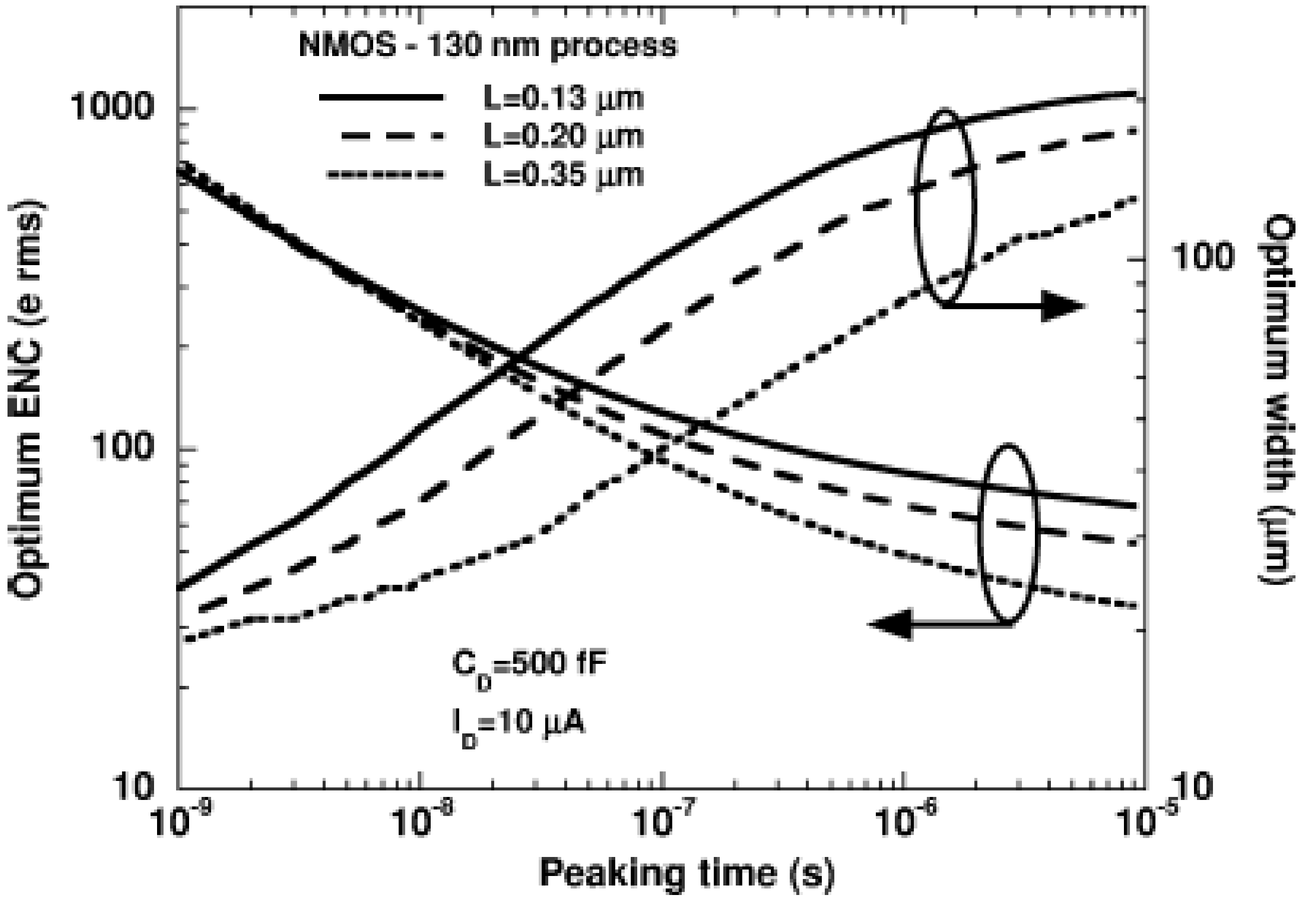


At t_P = 10 - 100 ns $C_{IN} \approx 0.1\ C_D$ gives minimum ENC

0.18 µm technology

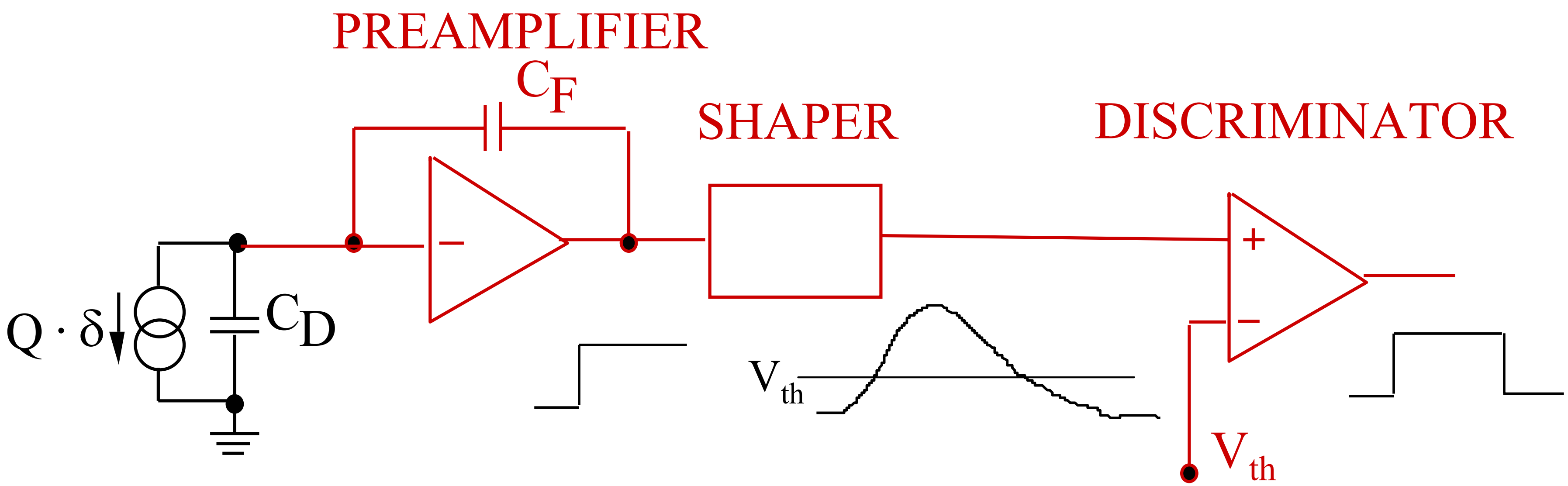
Capacitive matching in a deep submicron technology

- Optimum ENC and input NMOS gate width in the C_D region of pixel detectors



Extracting a hit information from the sensor signal: the discriminator

- Binary readout: hit/no hit information from a discriminator
- This can also be associated to an ADC system, providing an information about the charge delivered by the detector



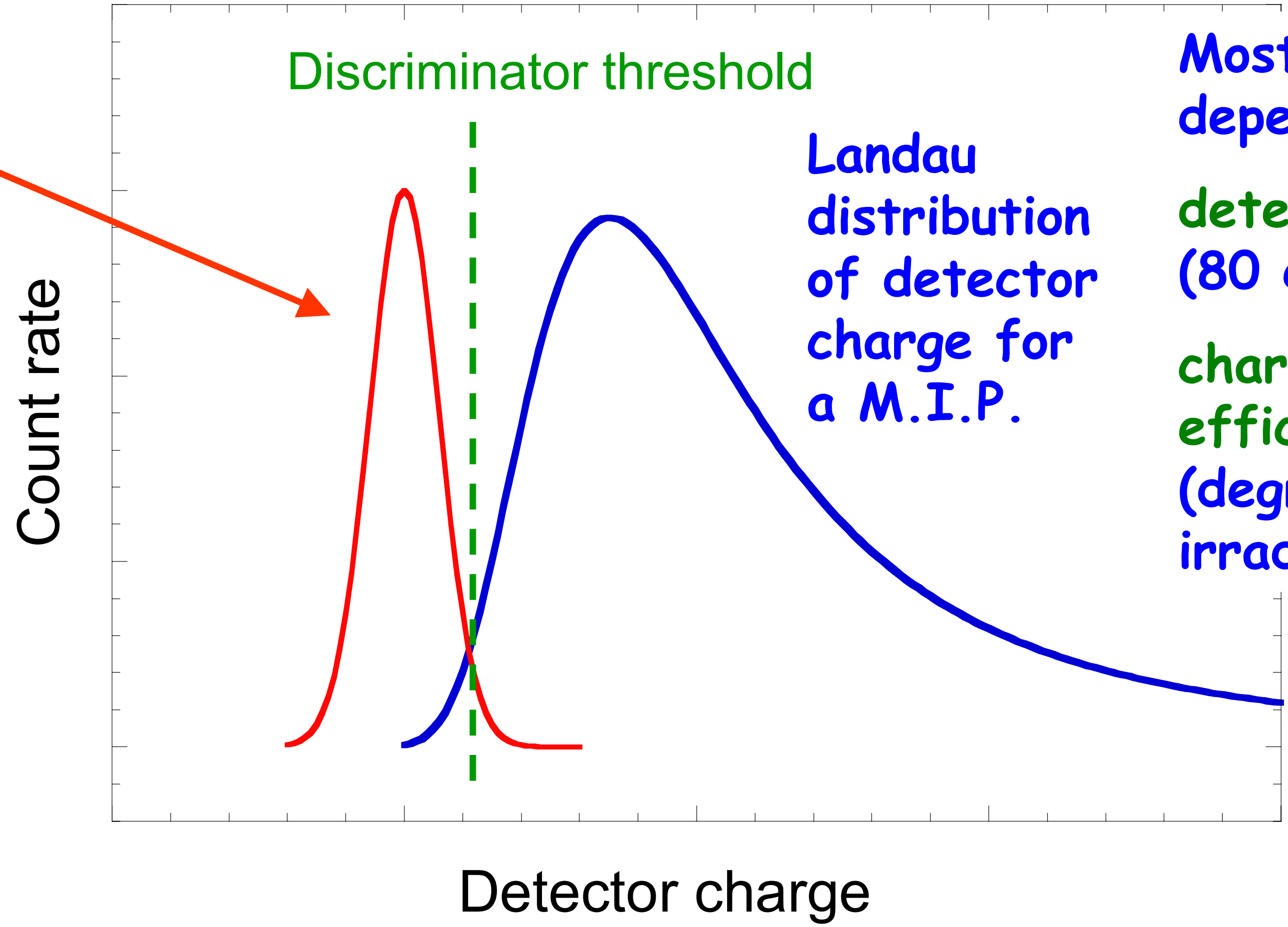
- In a multichannel readout chip, channel-to-channel threshold variations due to device mismatch may degrade detection efficiency and spurious hit rate

Efficiency and noise occupancy

- An excessive threshold dispersion can lead to channels with high noise hit rate or reduced efficiency in signal detection.

Noise gaussian distribution

(σ = ENC)



Most probable value depends on:

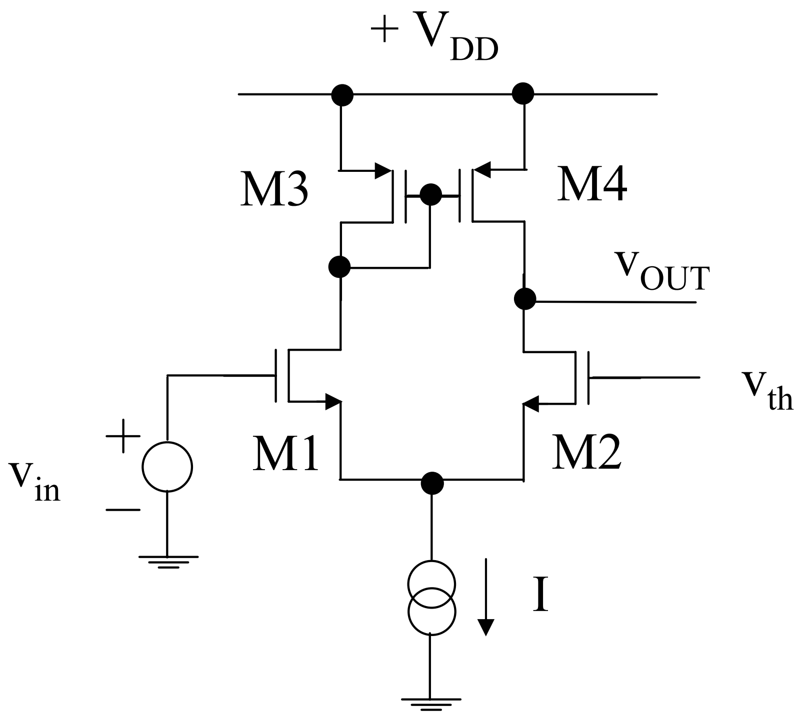
detector thickness (80 e-h pairs/μm)

charge collection efficiency (degraded in irradiated silicon)

Threshold dispersion

- Discriminator threshold dispersion is given by statistical variations of the threshold voltage of MOSFETs in the differential pairs used in the discriminator input stage:

$$\sigma^2(\Delta V_{th}) = \frac{A_{vth}^2}{WL}$$



Large area transistors help reduce the effect of threshold mismatch

- As for the noise, the discriminator threshold and its dispersion (divided by the analog channel charge sensitivity) can be treated in term of input-referred charges, Q_{th} and σ_{qth} respectively.

- For a second-order semigaussian shaper, and series white noise as the dominant contribution to ENC, the frequency of noise hits can be calculated as:

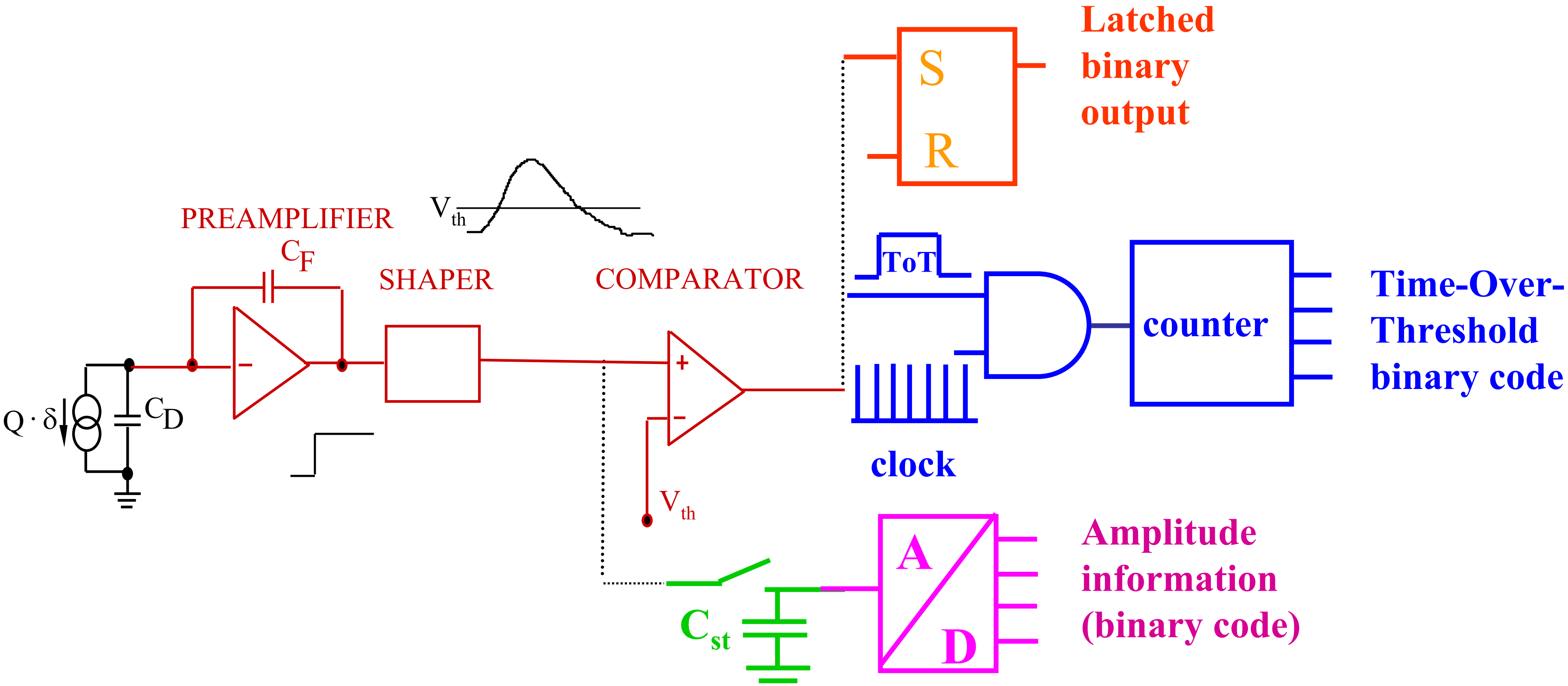
$$f_n = \frac{\sqrt{3}}{\pi t_p} e^{-\frac{Q_{th}^2}{2ENC^2}}$$

- In practical conditions, the number of noise hits can be kept at acceptably low values by satisfying this condition:

$$Q_{th}^{sig} > 4\left(ENC + \sigma_{qth}\right)$$

- To maintain an adequate efficiency, a channel-by-channel threshold adjustment may be necessary (threshold DAC in the pixel cell)

Analog-to-digital conversion

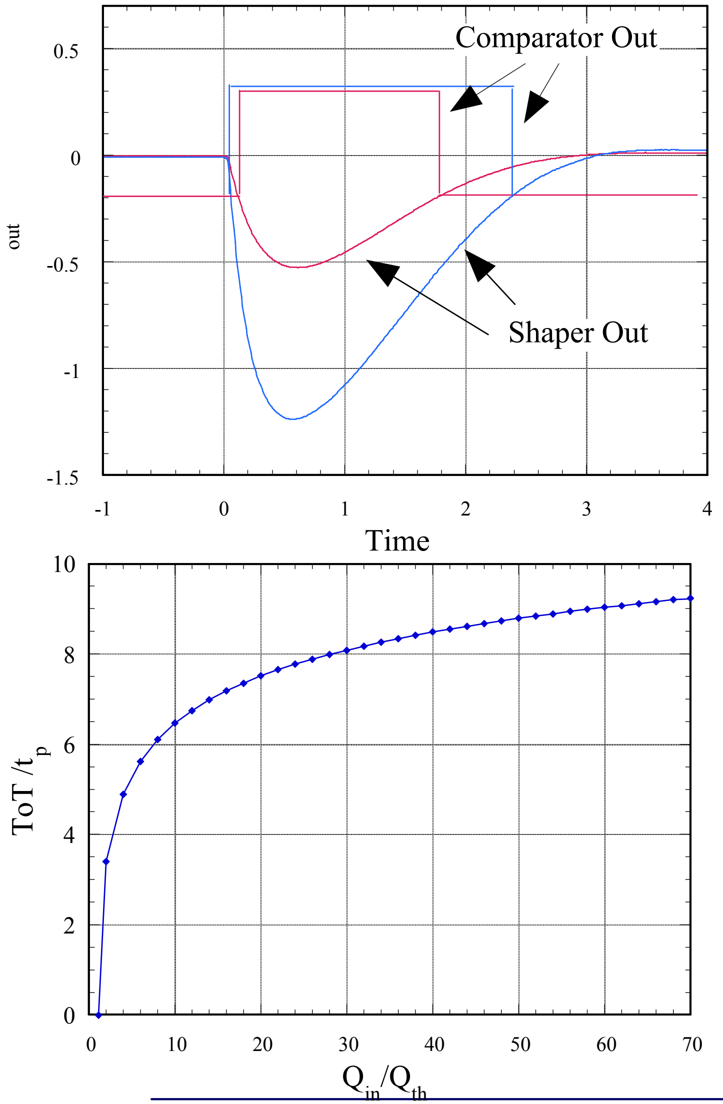


Flash, ramp, SAR,……

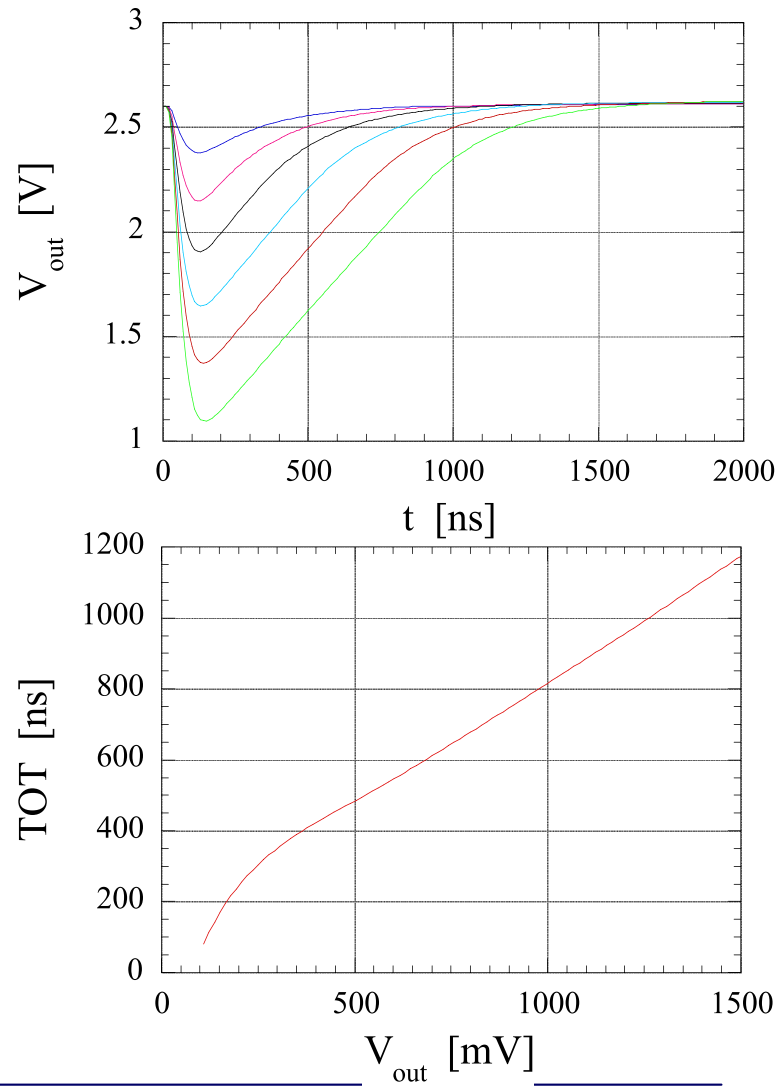
Time-Over-Threshold (ToT) analog-to-digital conversion

The ADC conversion of ToT is straightforward, avoiding circuit complexity in a chip with a very high functional density.

Compression type characteristic



Pseudo-linear characteristic



Readout architecture

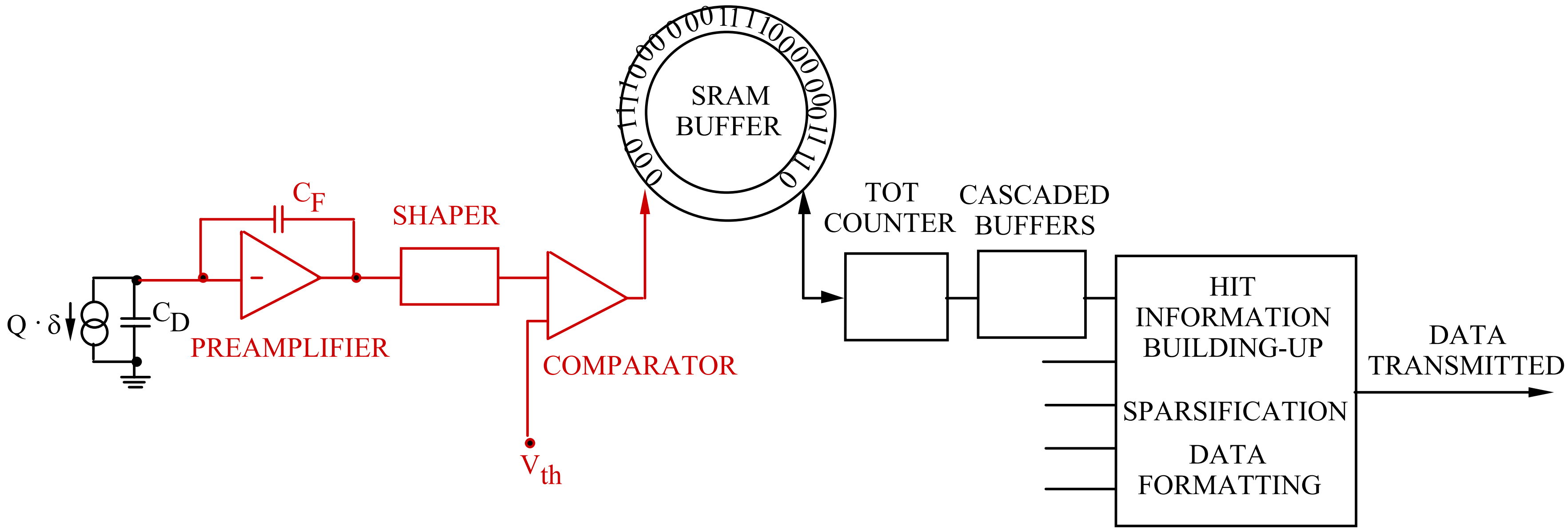
- Digital information of hit signals is further processed by circuitry associated to each pixel (strip) and at the chip periphery. Position (pixel or strip address), timing (time stamp) and possibly pulse amplitude (from ADC) information must be provided.

- All architectures perform data sparsification, processing only data from channels where the signal exceeds the discriminator threshold

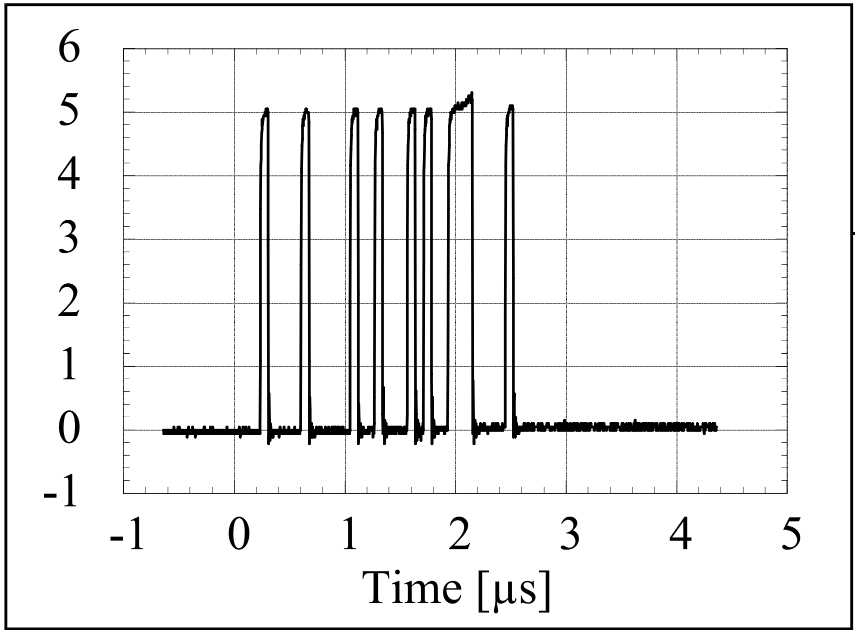
- Often, a trigger system selects only a fraction of the events for readout, reducing the data volume sent to the DAQ. In this case, information for all hits must be buffered for some time, waiting for a trigger signal (delay of a few μs).

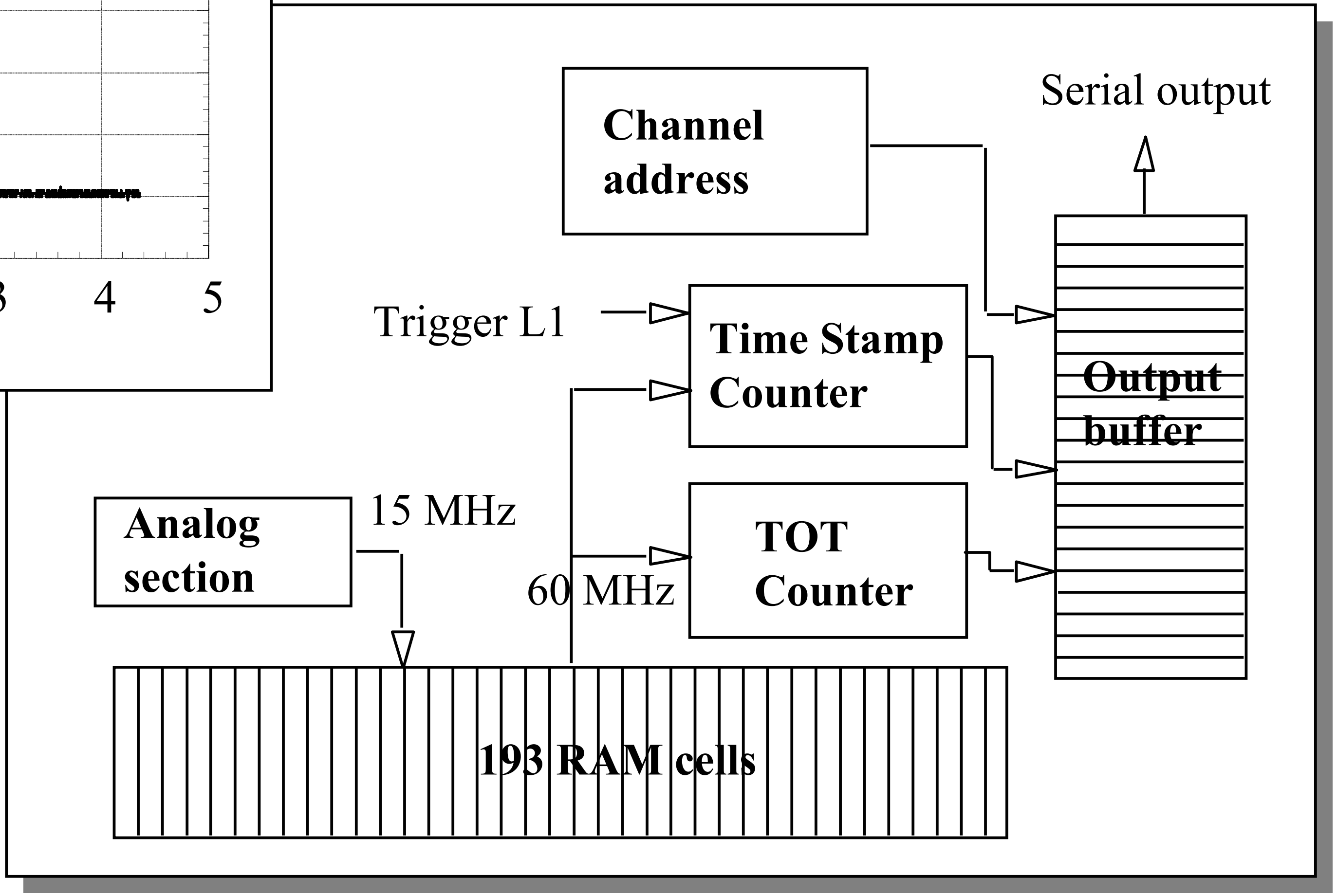
- Triggerless (data push architectures) are also available. All hits are read out immediately (as long as the rate is not too high). This allows the tracker information to be used for Level 1 Trigger (BTeV, SLHC)

Block diagram of the front-end chip AToM for signal processing in the BaBar Silicon Vertex Tracker



AToM digital section





1 start bit
4 chip address
1 read event/register
5 trigger tag
5 trigger time

7 channel number
5 time stamp
4 ToT

Time stamp readout in pixel readout chips

- A time stamp counter generates a time reference.

  The time stamp code:

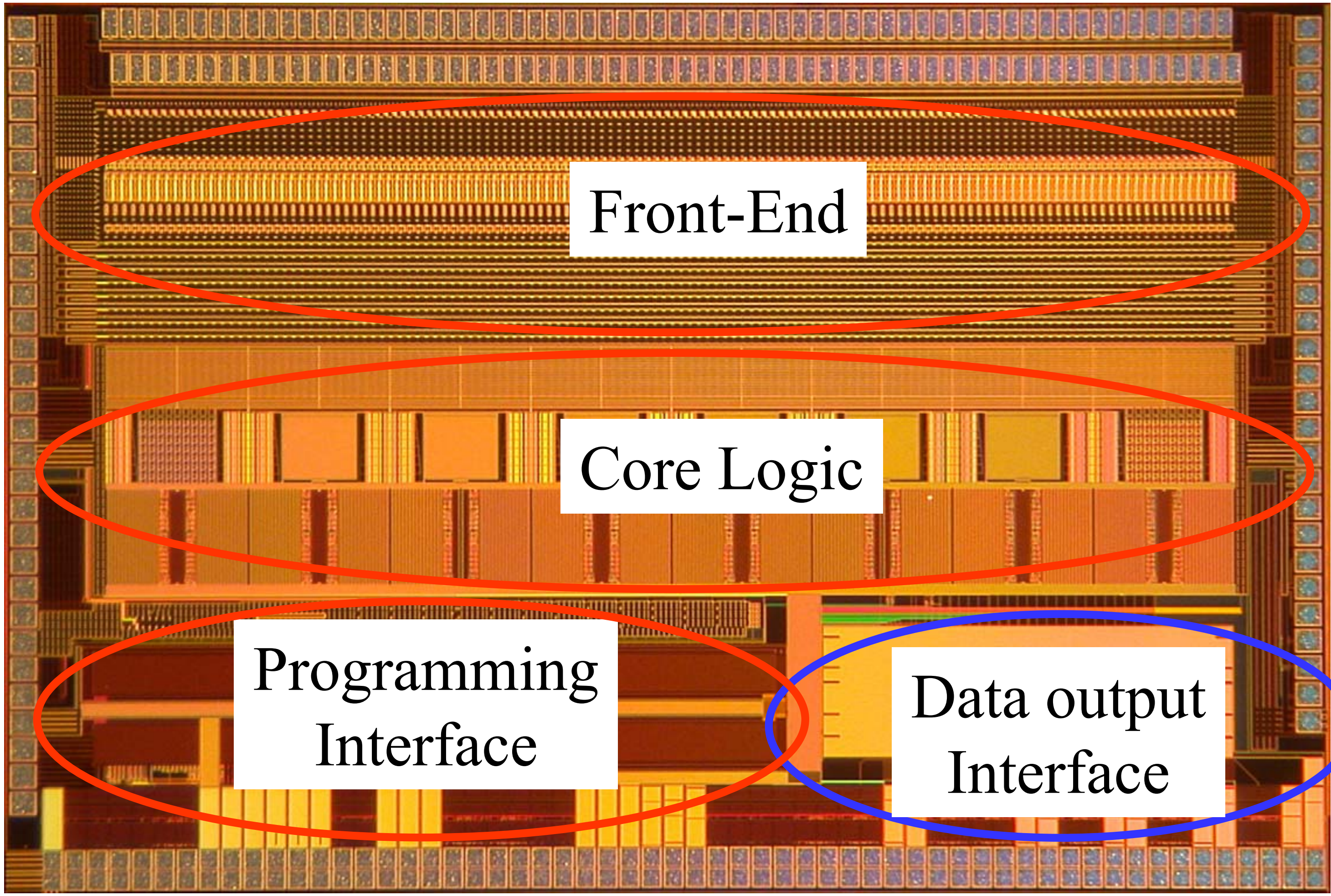
  1) can be distributed to all pixels

  The content of an in-pixel time stamp register is frozen when the pixel detects a hit and is then transmitted to the periphery.

  2) can stay in the chip periphery or in the "end-of-column" control logic block.

  When a pixel is hit, the end-of-column or periphery logic is informed that one or more hits have occurred and stores the relevant time stamp in a register.

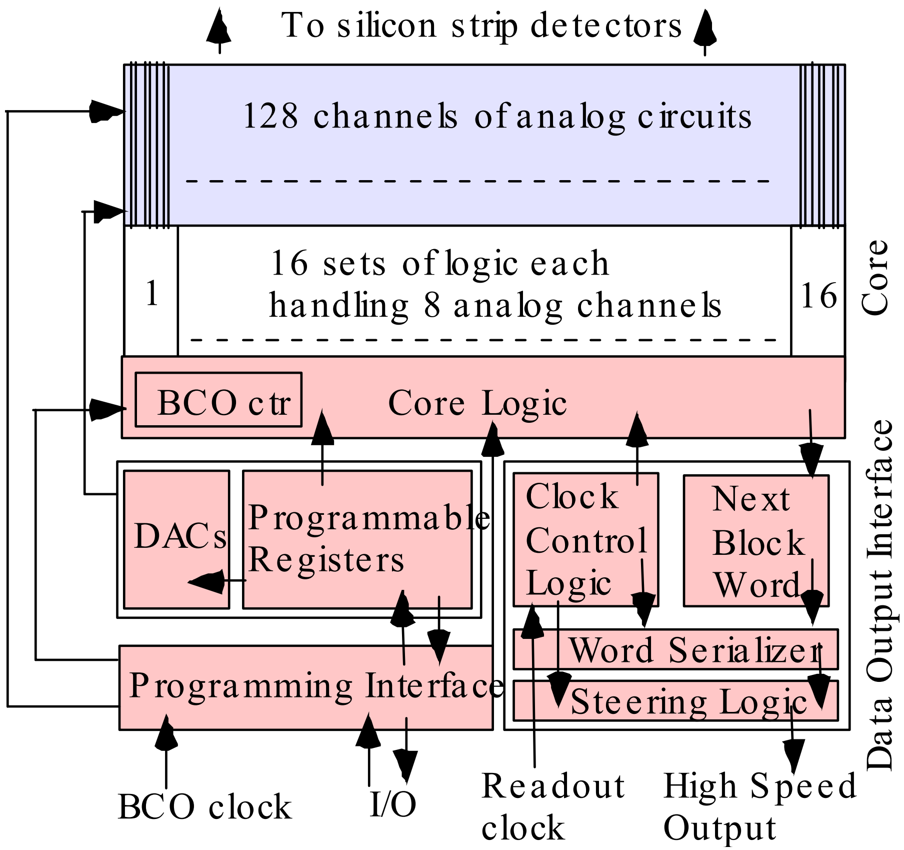
FSSR2 chip
(triggerless strip detector readout)



7.5 mm x 5 mm, input pads with 50 μm pitch

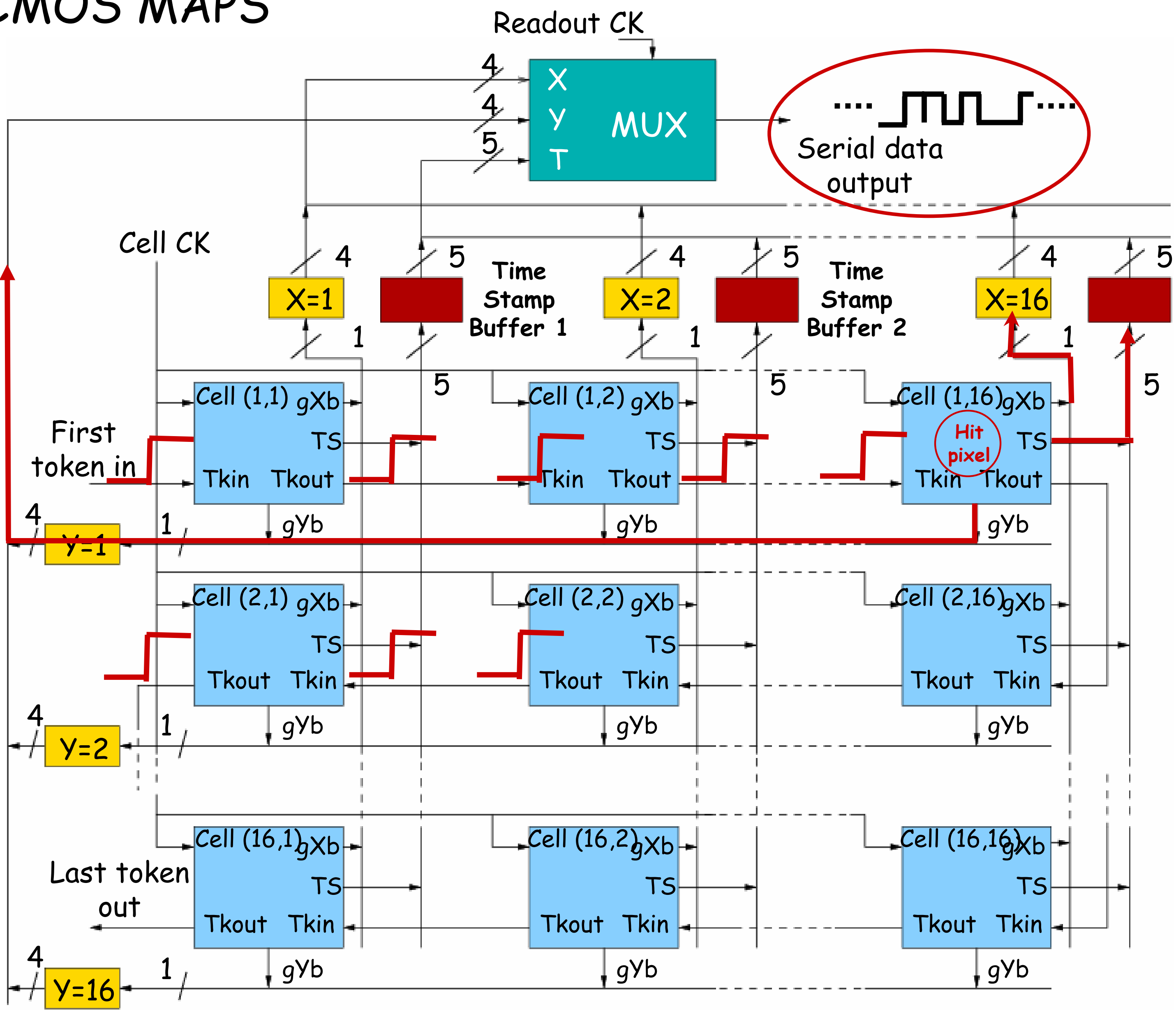
FSSR2 block diagram

- FSSR2 Core
  - 128 analog channels
  - 16 sets of logic, each handling 8 channels
  - Core logic with BCO counter (time stamp)
- Programming Interface (slow control)
  - Programmable registers
  - DACs
- Data Output Interface
  - Communicates with core logic
  - Formats data output



FNAL idea, implemented by INFN in a 130nm CMOS MAPS

ILC VTX pixel readout architecture



Readout phase:

- token is sent
- token scans the matrix and
- gets caught by the first hit pixel
- the pixel points to the X and Y registers at the periphery and
- sends off the time stamp register content
- data are serialized and token scans ahead

The number of elements may be increased without changing the pixel logic (just larger X- and Y- registers and serializer will be required)

CMOS and LHC upgrades: from deep submicron to ultra-deep submicron

- New generation of mixed-signal integrated circuits for the readout of pixel and strip detectors for HEP and imaging experiments are being designed in CMOS technologies in the 100 nm range

- In future collider experiments, pixel sensors and front-end electronics will be very close to the beam interaction region, and radiation tolerance will be an essential requirement

- For analog front-end circuits, noise performance under irradiation is critical, since thin and/or heavily irradiated silicon detectors will deliver a considerably smaller signal than standard, 300 μm-thick sensors

- 130 nm and 90 nm CMOS technologies have the potential of a high degree of radiation tolerance because of the thin gate oxide, but peculiar effects may pose threat (thick isolation oxides, gate tunneling current)

Ionizing radiation levels for front-end electronics in SLHC

- Pixel layers : 100 Mrad – 350 Mrad

  (several years lifetime, not including safety factors)

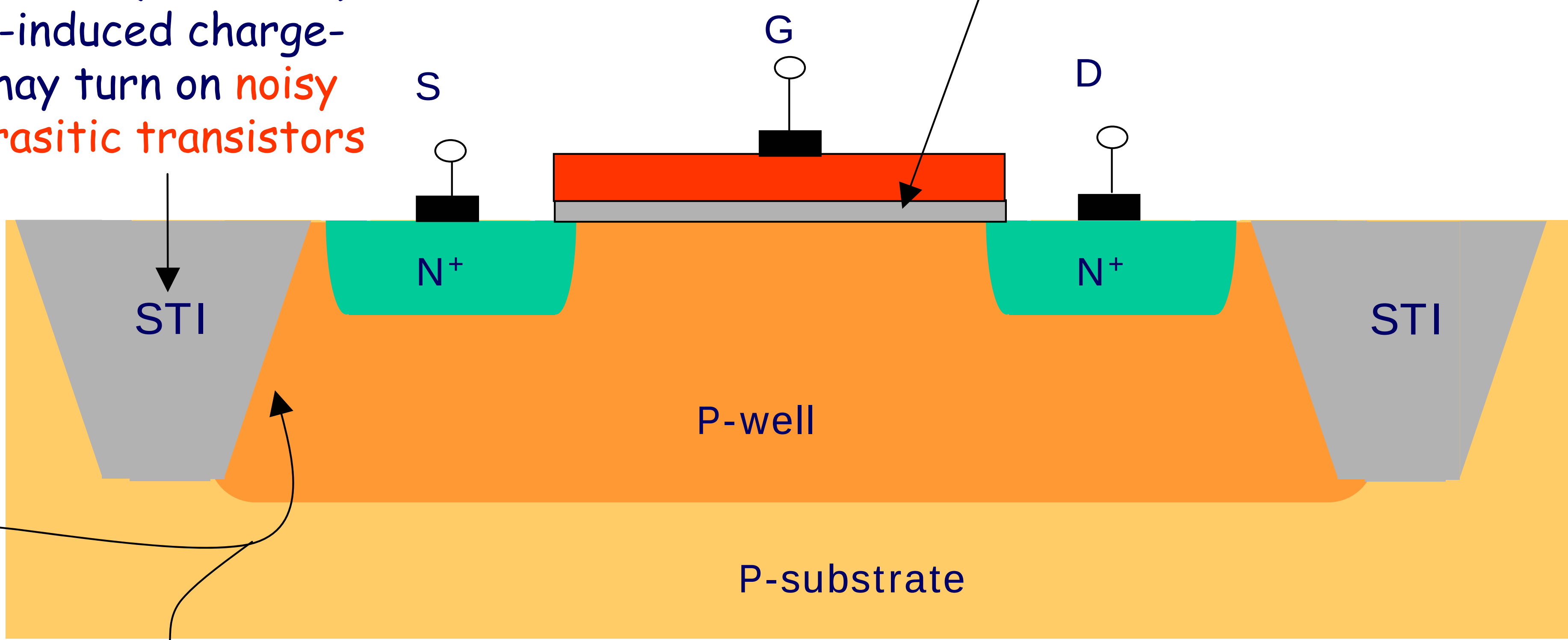
- Short strips (C_D = 5 pF): 10 – 15 Mrad

- Long strips (C_D = 15 pF): 4 – 5 Mrad

Ionizing radiation effects in MOSFETs

Thick Shallow Trench Isolation Oxide (~ 300 nm): radiation-induced charge-buildup may turn on noisy lateral parasitic transistors

Thin gate oxide for core devices, radiation-induced positive charge is removed by tunneling, when thickness ~ 2 nm, as in CMOS technologies in the 100 nm regime

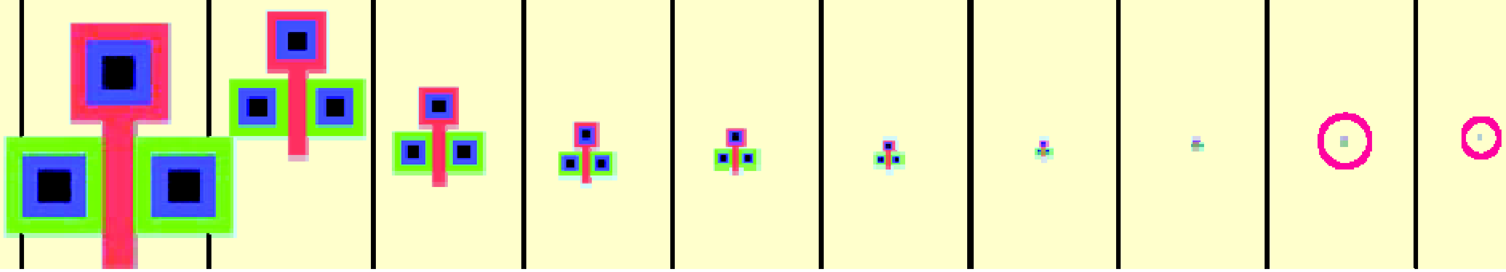


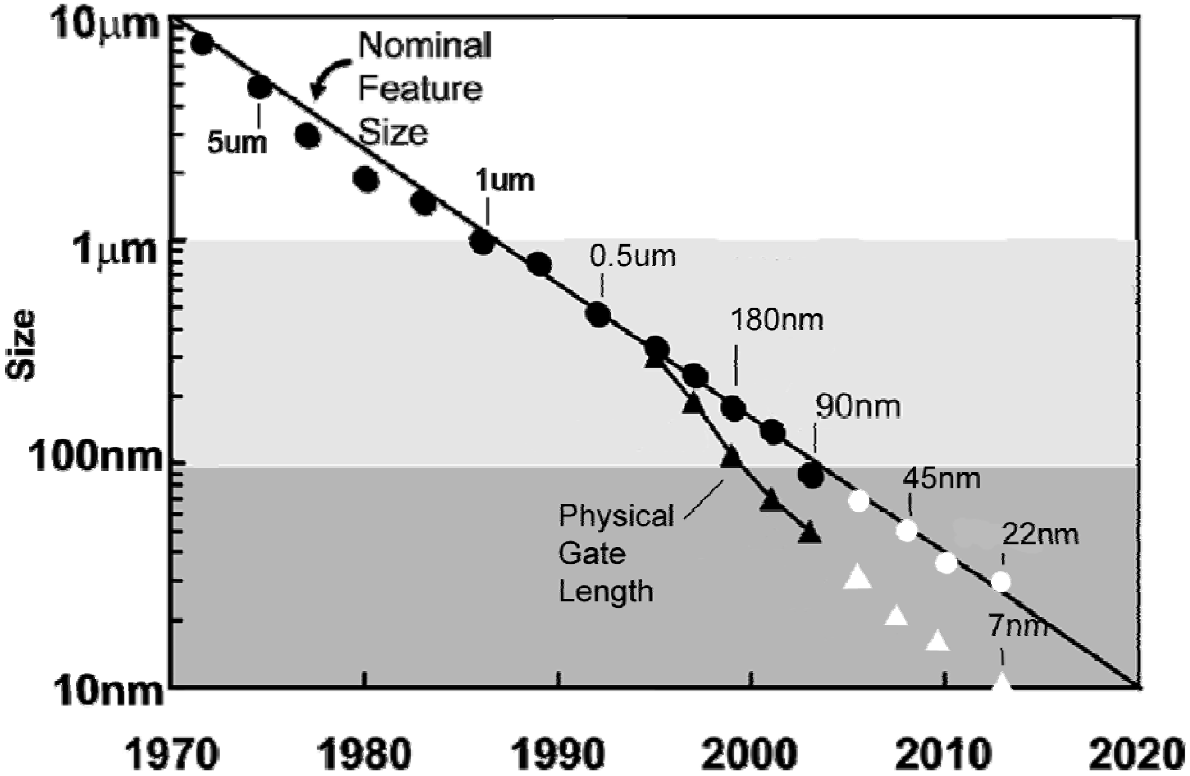
Doping profile along STI sidewall is critical; doping increases with CMOS scaling, decreases in I/O devices

Increasing sidewall doping makes a device less sensitive to radiation (more difficult to form parasitic leakage paths)

Industry Scaling Roadmap

Feature Size [nm]	2000	1200	800	500	350	250	130	65	35	20
Minimum NMOS										



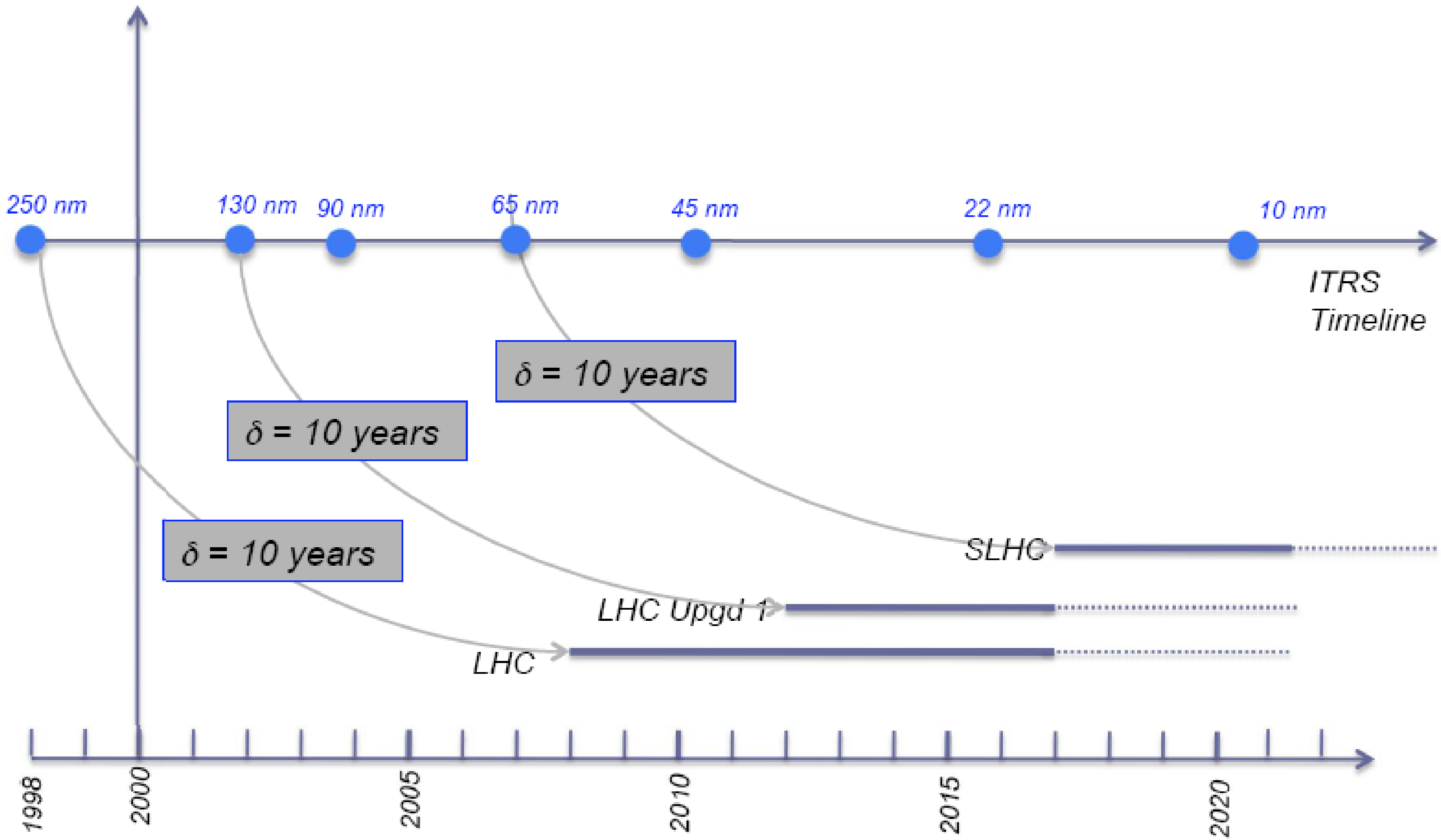


CMOS generations: beyond 100 nm, towards 65 nm

- Industrial CMOS scaling is entirely driven by commercial digital electronics. Front-end electronics may benefit from scaling in terms of functional density (small pitch pixels) and digital performance. Analog design is a challenge (reduced supply voltage and dynamic range, statistical doping effects, ………)

- CMOS scaling is going towards sub-100 nm processes. 65 nm CMOS is today a well-established industrial process. Gate material is changing (SiON), V_{DD} = 1.2 V as in 130 nm CMOS. Preliminary data show a comparable noise performance as less scaled technologies; what about radiation hardness (and, obviously, cost)?

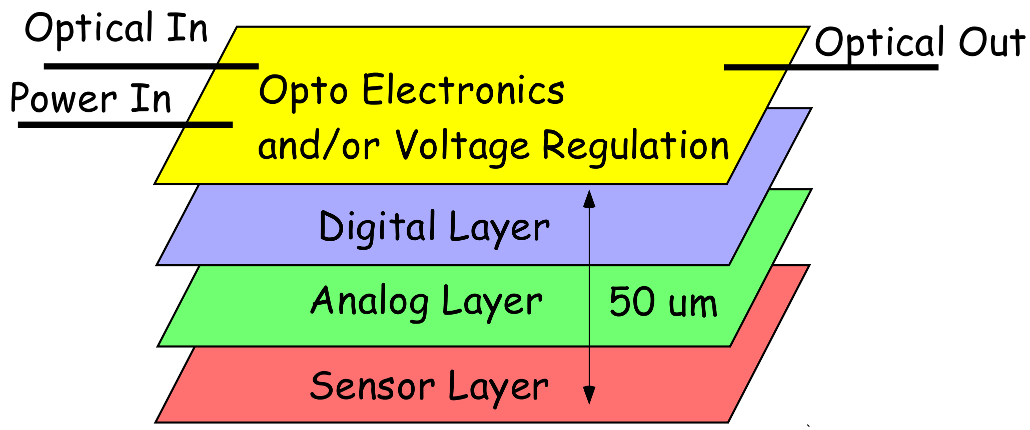
Perspectives



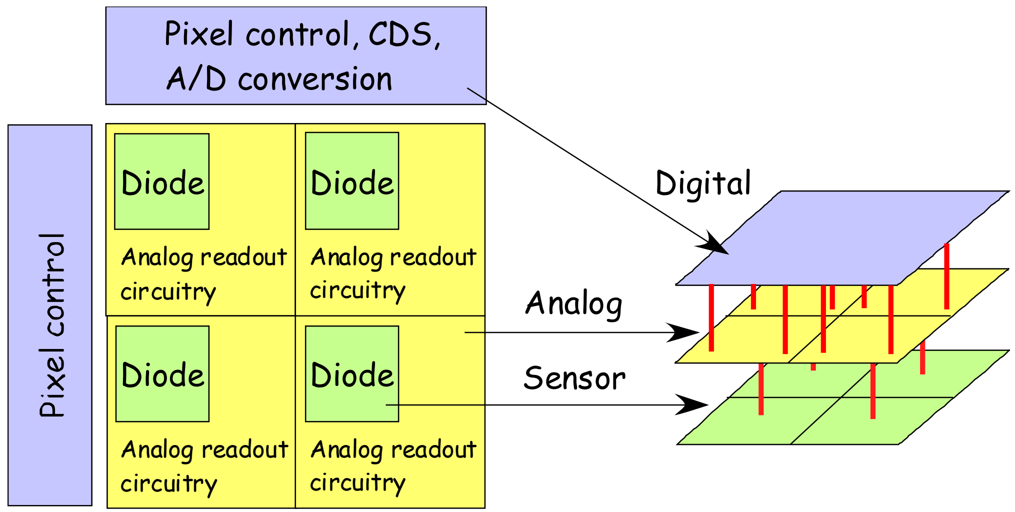
A. Marchioro / CERN

A different approach: vertical integration

- A "3D" chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward Vertical Integration to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk
- This is a major direction for the semiconductor industry.



Physicist's Dream



Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

3D Consortium (FNAL, IN2P3, INFN) 3dic.fnal.gov

VIPIX INFN project: eil.unipv.it/vipix

Conclusions

- Front-end electronics for silicon trackers in future experiments is an exciting challenge for integrated circuit designers

- Classical analog problems (signal amplification and shaping, noise, threshold dispersion) will require clever solutions

- New industrial technologies (nanoscale CMOS, vertical integration, …) will be exploited to achieve increasingly demanding specifications

References

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- V. Radeka: “Low-noise techniques in detectors”, Ann. Rev. Nucl. Part. Sci., 1988
- G. Lutz: “Semiconductor radiation detectors”
- L. Rossi, P. Fischer, T. Rohe, N. Wermes: “Pixel Detectors. From Fundamentals to Applications”
- H. Spieler: “Semiconductor detector systems”

Spare slides

Pixel detectors in future HEP experiments

- Physics goals set severe requirements:
  - High granularity ⇒ small pixel pitch
  - Low material budget ⇒ low mass cooling, thin silicon wafers, small amount of material for support and interconnections
  - Small distance to interaction point ⇒ large background

⇙ High data rate, Level 1 trigger

⇘ radiation hardness (deep submicron CMOS intrinsically rad-hard)

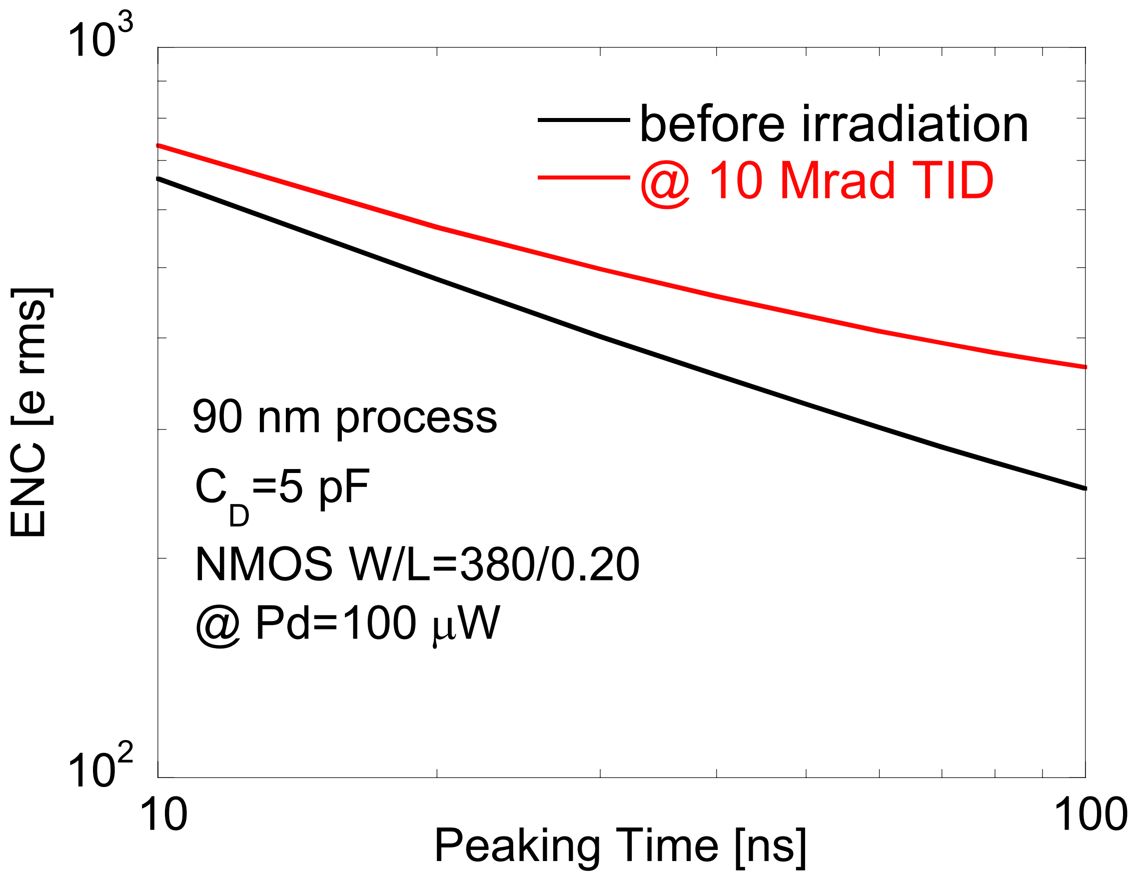
⇓ Data sparsification

⇙ Full CMOS ⇖ In MAPS, loss of efficiency due to in-pixel PMOS

⇘ Mixed-signal chips ⇗ Digital-to-analog interferences

Rad-hard, low-noise charge preamplifier design: strip readout with 90 nm electronics, NMOS input

- The parallel noise contribution from the detector leakage current is neglected here.
- The device width W is optimized as a function of the detector capacitance for the peaking time region around 50 ns under typical power dissipation constraints.
- At 10 Mrad, at the low current density dictated by power dissipation constraints, the 1/f noise increase affects ENC also in 25 – 50 ns peaking time region.

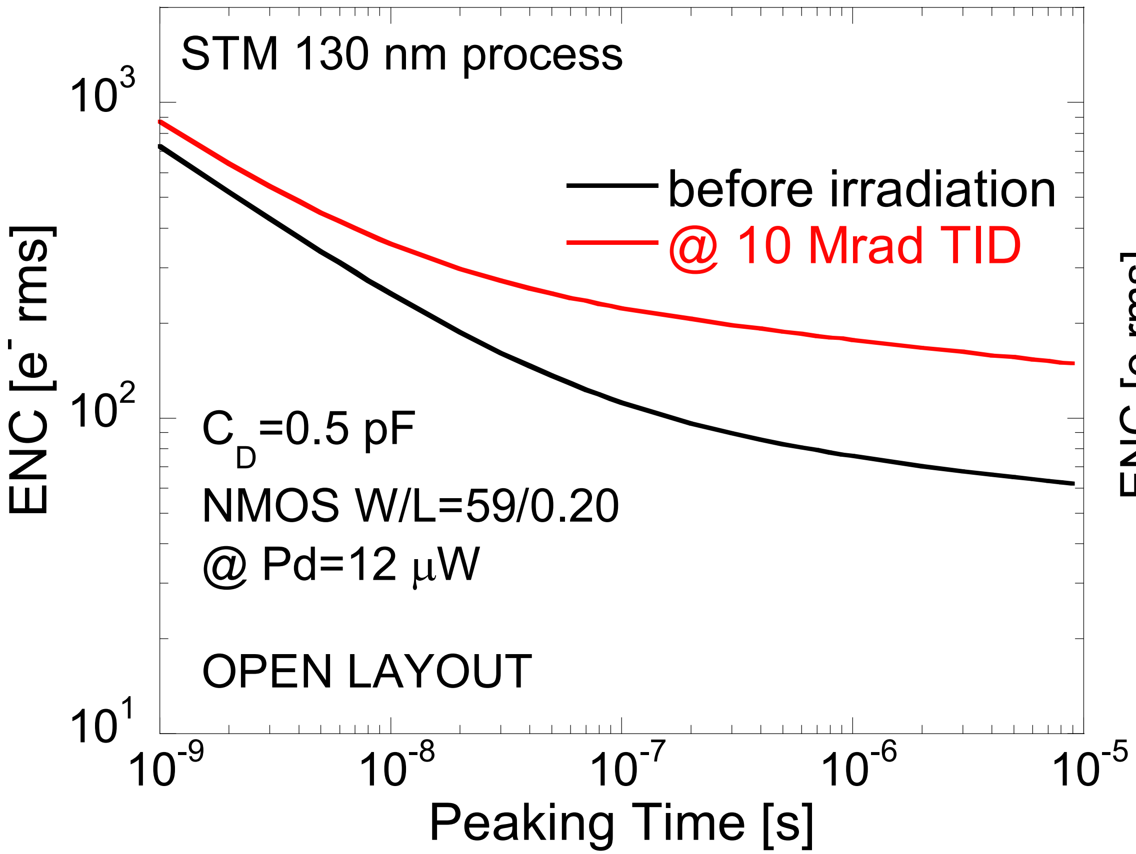


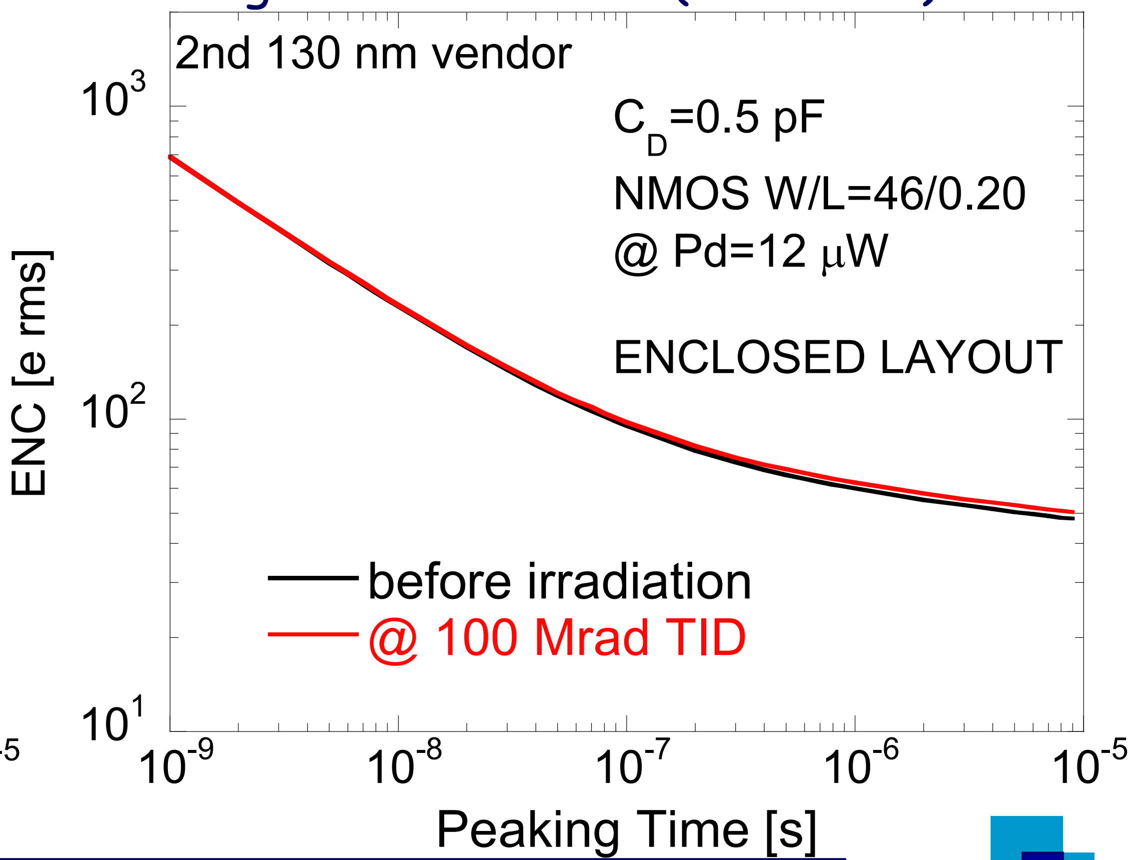
- ENC estimates based on measured noise parameters show that ENC increases by about 20% at t_p = 25 ns (430 e → 520 e) and by about 30 % at t_p = 50 ns (325 e → 430 e) (the noise contribution from the gate leakage current can be neglected in this range)

Ionizing radiation effects on signal-to-noise ratio: pixel readout with 130 nm electronics

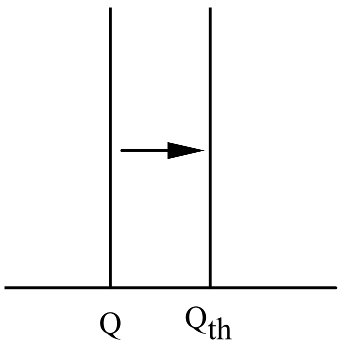
- Even at 10 Mrad, in open layout devices the white and 1/f noise degradation increase ENC by 80% - 100% in the 25 – 50 ns peaking time region.

- In enclosed NMOSFETs, since there are no lateral parasitic devices turning on and contributing to noise, on the basis of irradiation tests we can predict that ENC is not affected by the absorption of high ionizing radiation doses (100 Mrad).

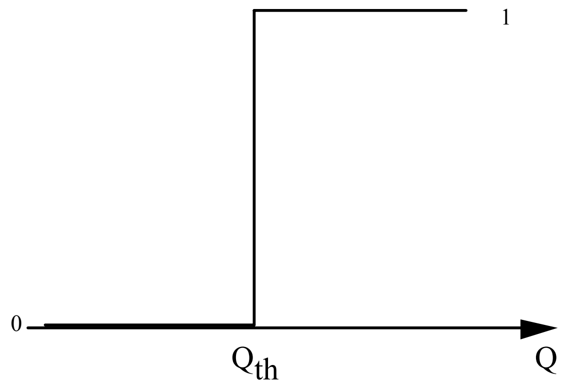


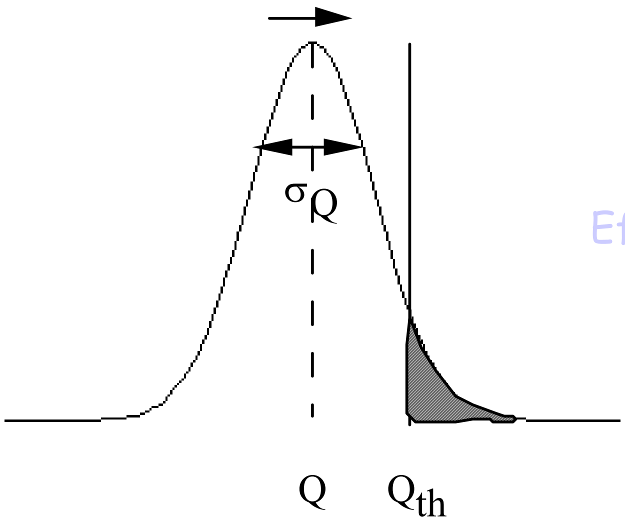


Effect of noise on discriminator firing efficiency

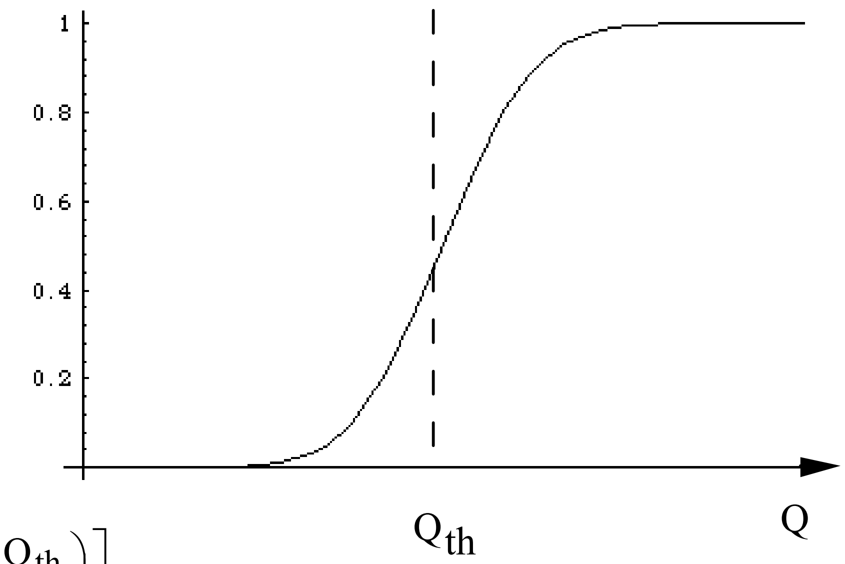


Noiseless system



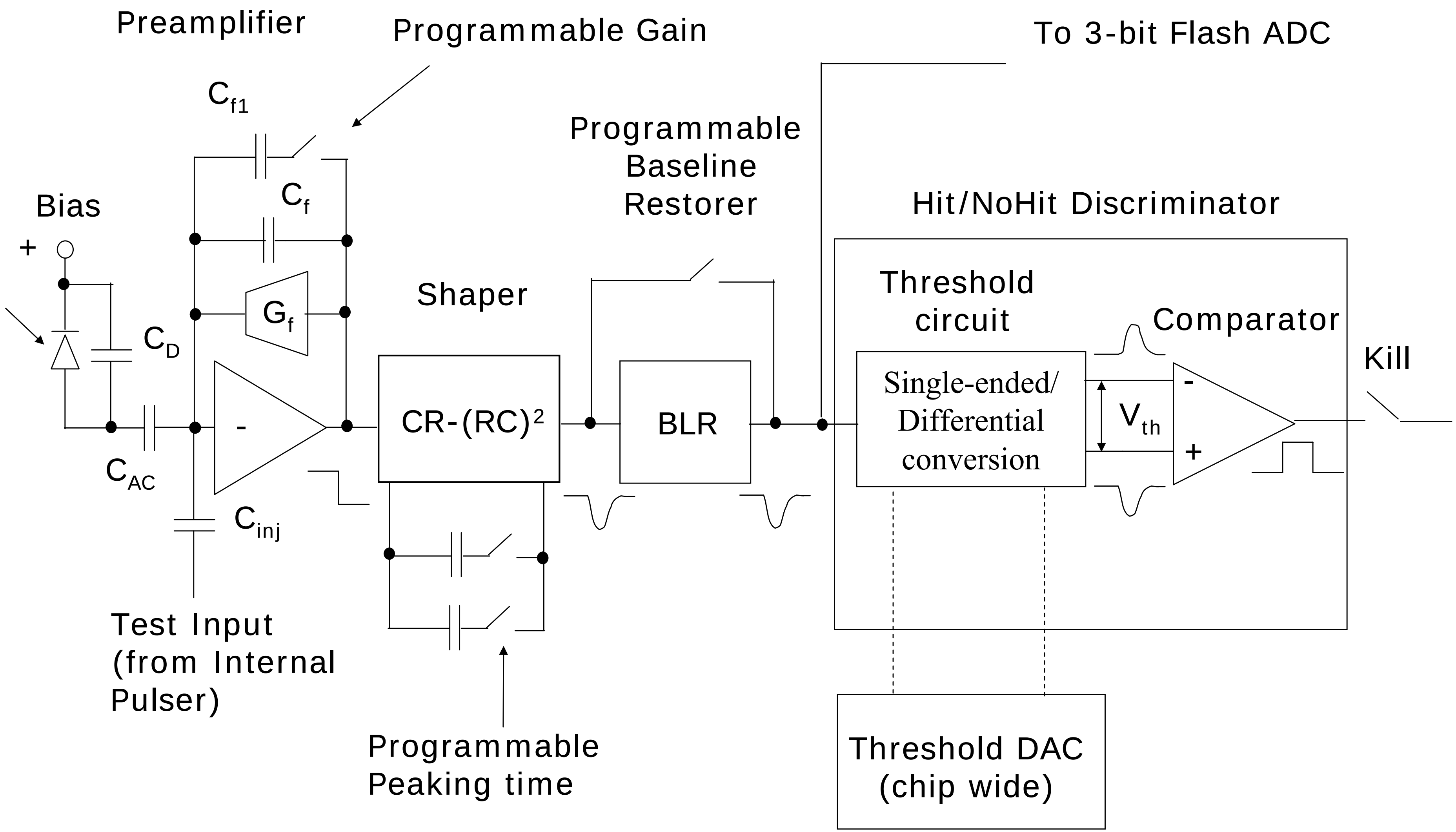


Effect of noise



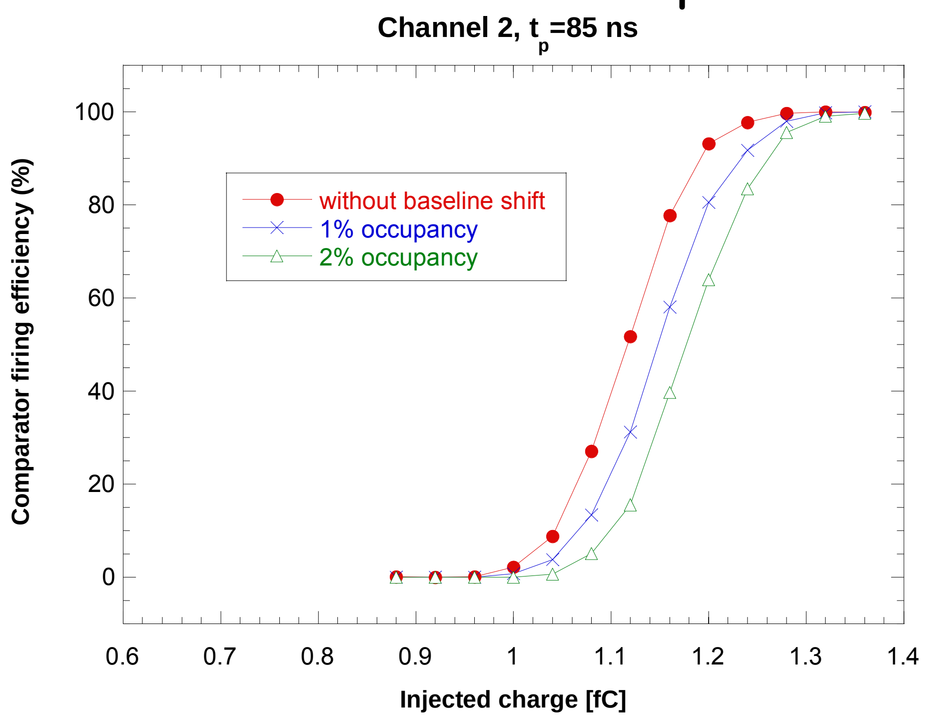
$$P(Q_{th}) = \int_{Q_{th}}^{+\infty} \frac{1}{\sqrt{2\pi}\sigma_Q} \exp\left[-\frac{(q-Q)^2}{2\sigma_Q^2}\right] dq = \frac{1}{2}\left[1 + \mathrm{Erf}\left(\frac{Q-Q_{th}}{\sqrt{2}\sigma}\right)\right]$$

Analog channels (FSSR2 chip)

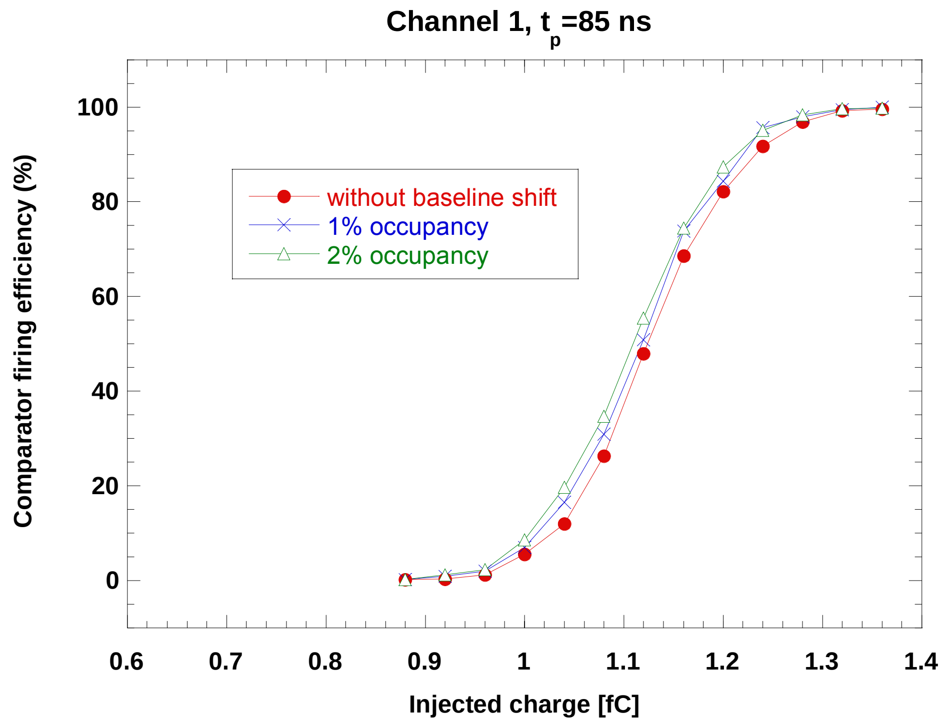


Processing the signal from the sensor: the baseline restorer

- Since the signal at the preamplifier output is not an ideal voltage step, but returns to baseline with a long time constant, the signal at the shaper output has a long tail. This results in a baseline shift at the discriminator input, with related statistical fluctuations, adding to the threshold dispersion.



Input signal discriminator scan without BLR



Input signal discriminator scan with BLR

Shift and fluctuations of the baseline at the discriminator input can be removed by a baseline restorer.