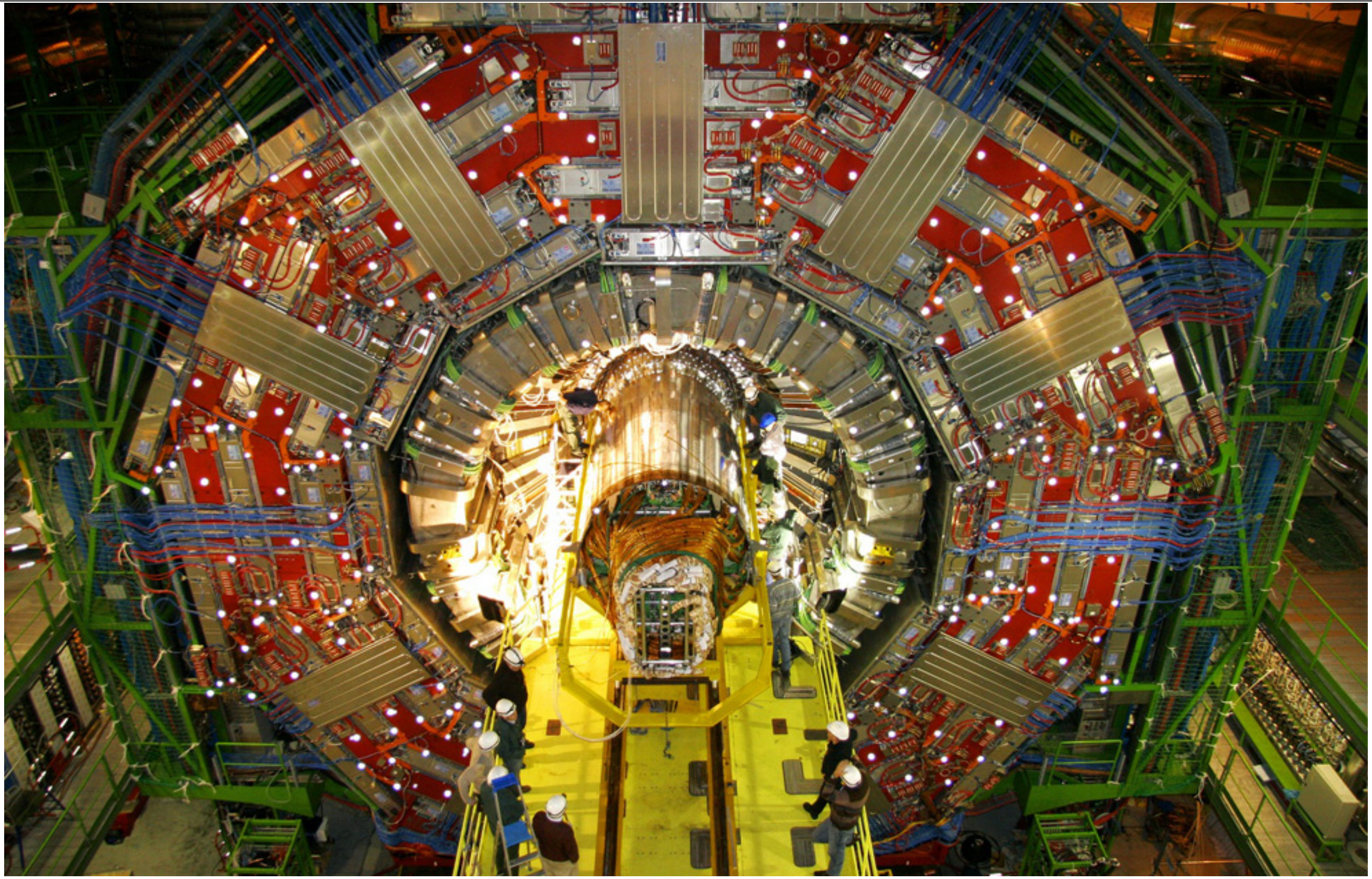


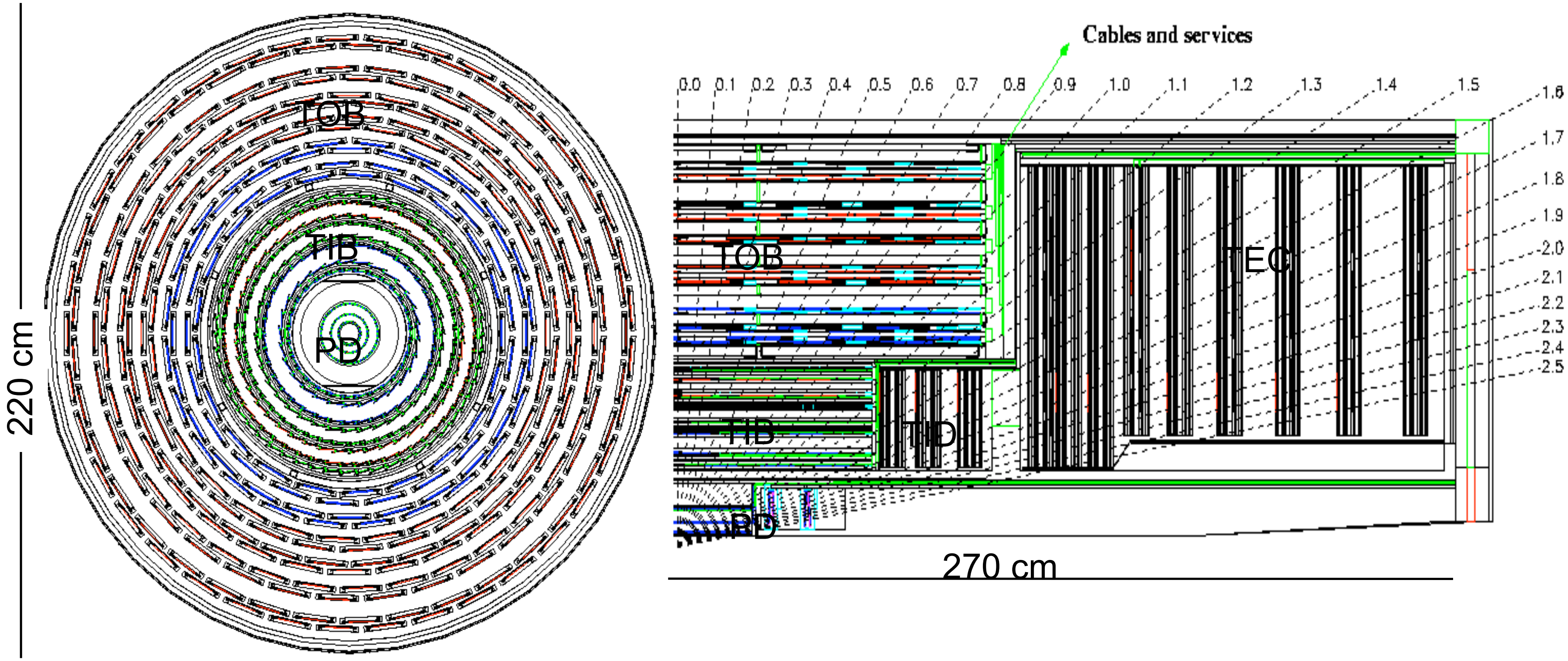
Le sfide per i tracciatori a Super LHC

Fabrizio Palla
INFN Pisa

Outline

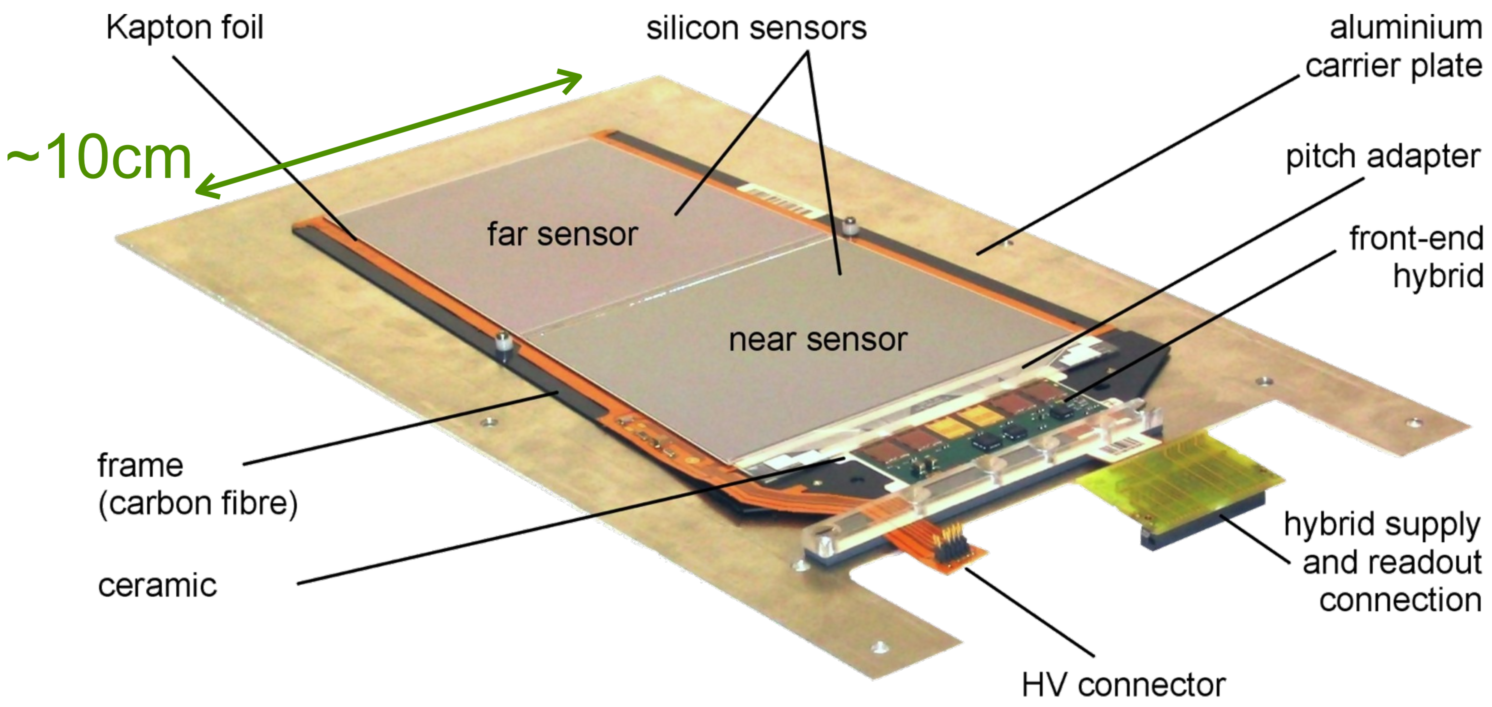
- Why (and when) SLHC
- General concepts for a Tracker upgrade
  - Sensors R&D (much details in the talks from previous speakers)
  - Power issues
  - Cooling
- Phase I - pixel replacement
- Phase II - Tracker Trigger problems
- Fast links
- Conclusions

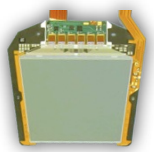
The CMS Silicon Tracker



210m2 micro-strip silicon detectors 15.232 modules
6136 320µm thick and 18.192 500µm thick sensors (all from 6” wafers).
7.136 APV chips
9.648.128 analog strip channels.
About 25M wire bonding.

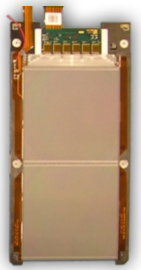
The Si-strip module





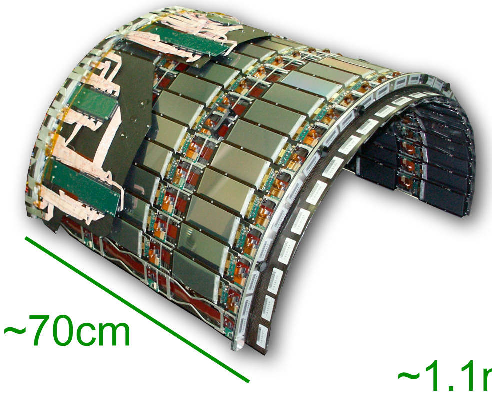

15148 modules
of 27 different sizes and shapes.

Modules are robust, easy to handle
and of excellent quality.

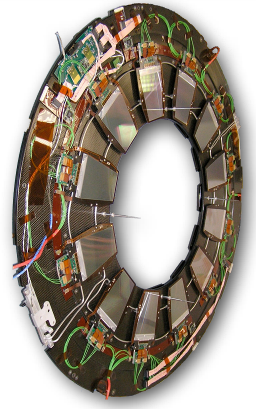
Substructures

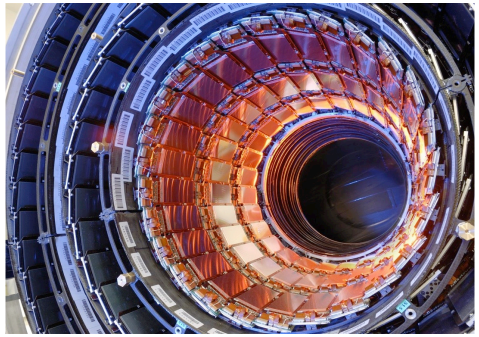
TIB: 16 half cylinder *shells*, 135 to 216 modules
TID: 18 *rings*, 40 to 48 modules



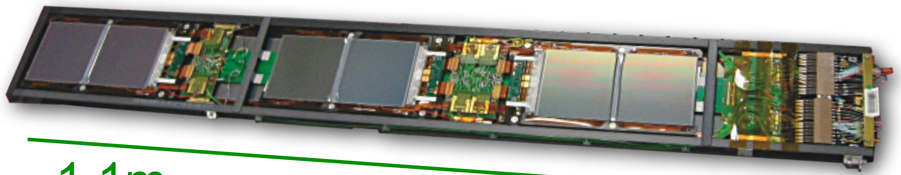
~70cm

~1.1m

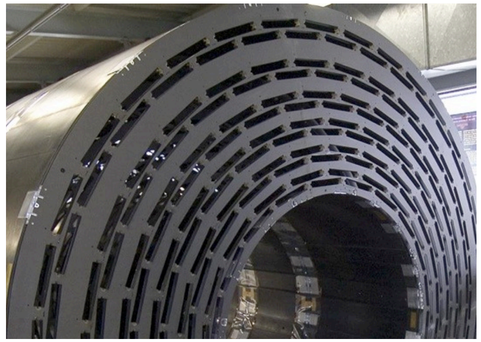




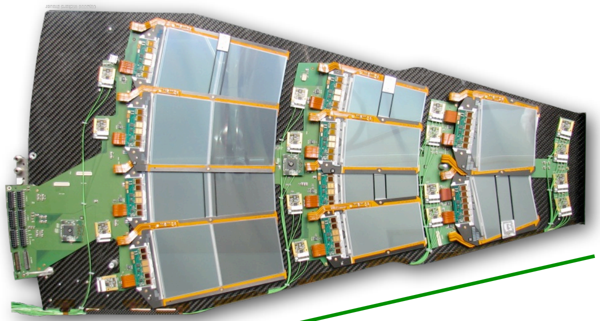
TOB: 688 *rods*, 6 or 12 modules



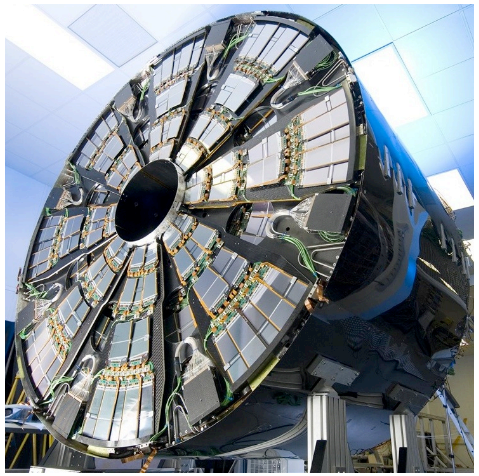
~1.1m



TEC: 2x144 *petals*, 17 to 28 modules.



~80cm

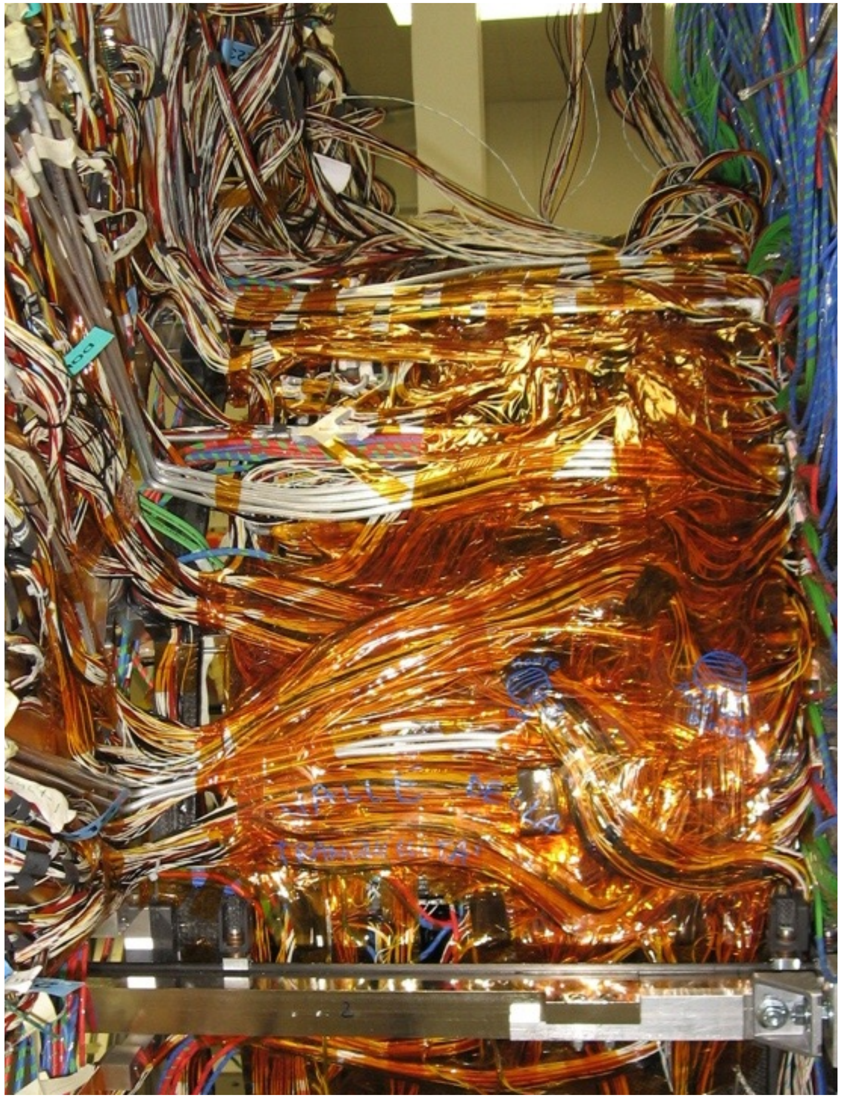


TIB/TID services

TIB/TID is challenging in terms of number of channels over volume density.

	#channels	Volume $[m^3]$	Density $[\times 10^6 ch/m^3]$
TIB	1 787 904	0.82	2.2
TID	565 248	0.5	1.1
TOB	3 096 576	5.9	0.52
TEC	3 866 624	11	0.35

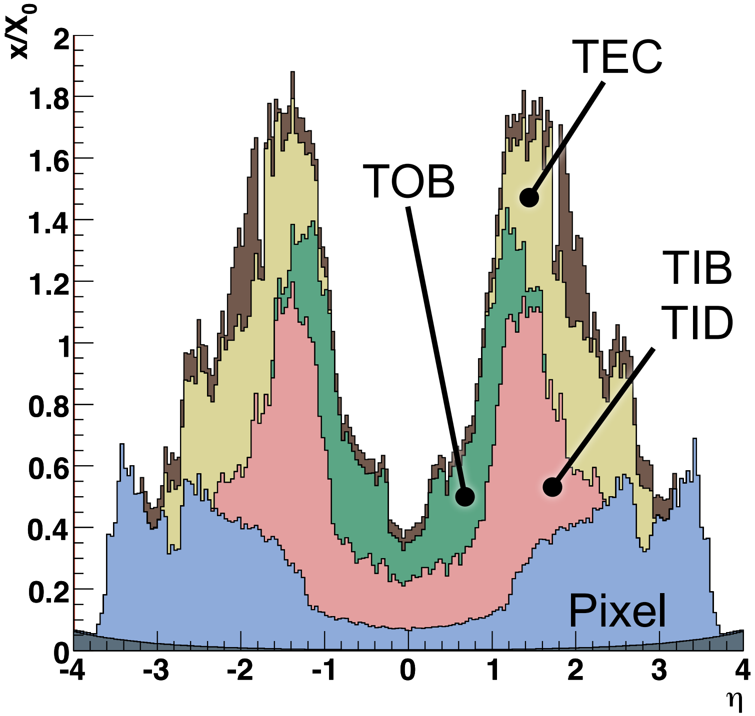
A very large number of service connections to be constrained in a very tight room:
- ordered layout difficult;
- tough handworked job.



Material Budget

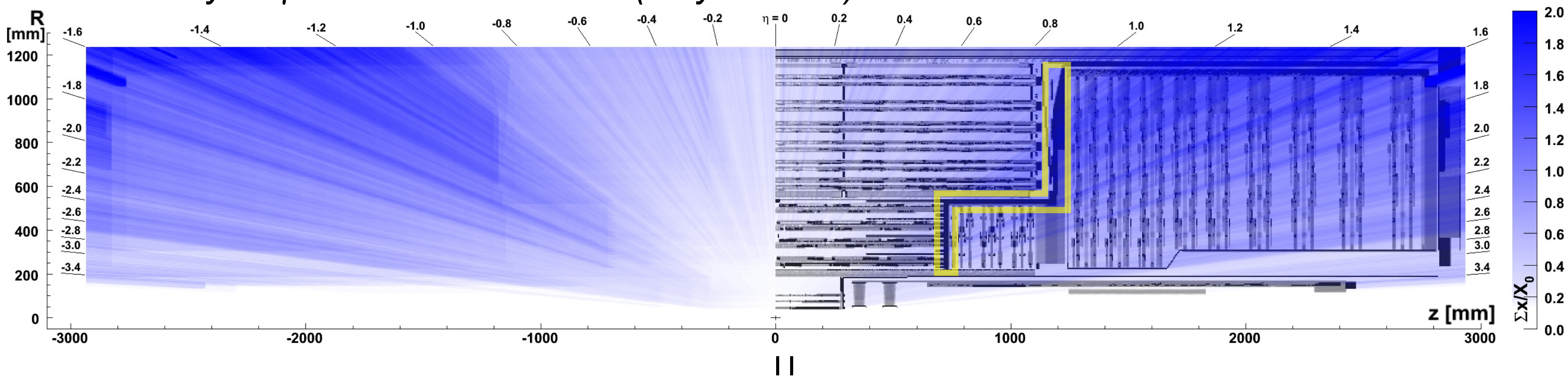
The completion of the tracker allowed for a realistic MB estimation to be done, all details included!

Large contribution comes from service volumes, especially at smaller radii (TIB and TID)



$\sum x^{*}X_0^{-1}[cm^{-1}]$ ~density of γ conversion tracks

X_0^{-1} ~density of γ conversion vertices (only z+ side)



SST: DAQ system

Read-out system

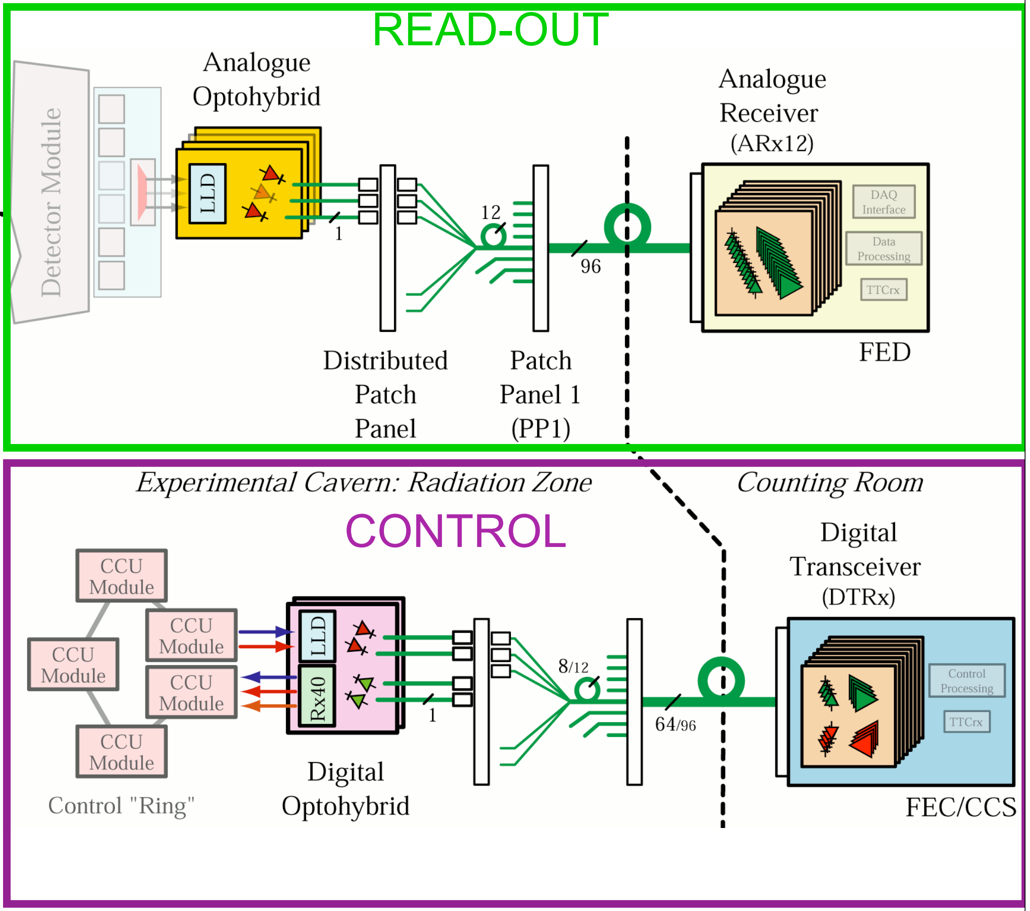
based on the FE chip APV25 and Front-End Driver (FED)

- APV25: analogue signal amplified, shaped and buffered
- data sent to FED via optical link
- FED: signal processing (reordering, pedestal and noise subtraction, cluster finding)

Control system

based on Front-End Controller (FEC) and organized in token ring

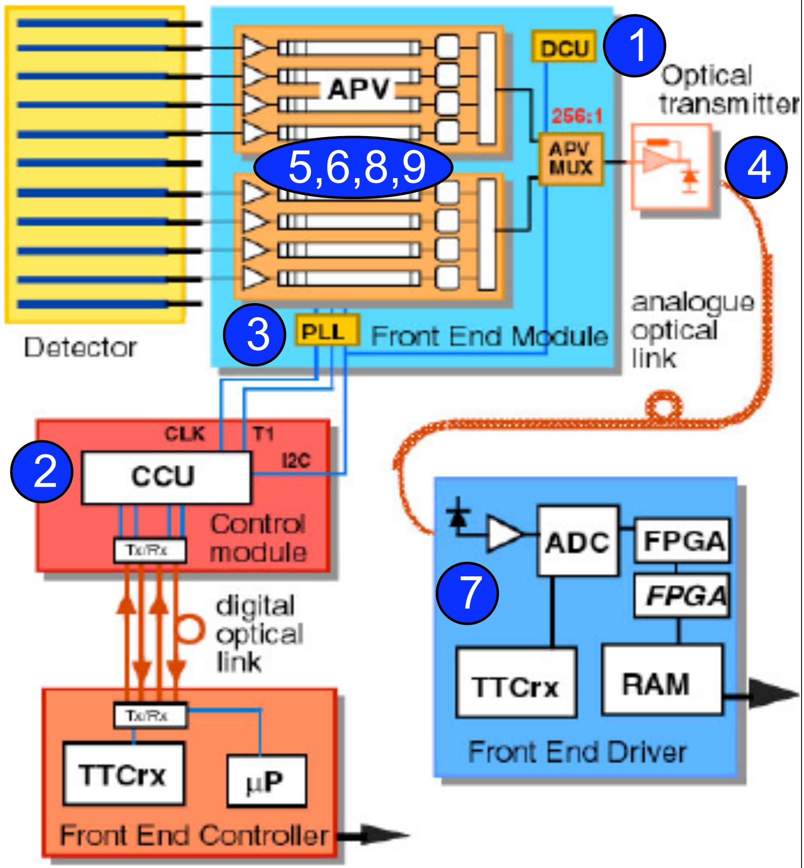
bidirectional digital flow (via optical link) to distribute slow control commands, clock and trigger signal and also to monitor the front-end electronics



SST: Commissioning

The commissioning procedure is required to configure, synchronize and calibrate the various components of the readout system. It consists of several independent steps performed on four partitions (TIB/TID, TOB, TEC-, TEC+)

- **Check of connection**
  - Electrical cabling (1)
  - Optical cabling (2)
- **Internal timing**
  - Synchronization of all channels to include different fiber length (3)
- **Chip parameter optimization**
  - Optical Gain (4)
  - Analog baseline tune (5)
  - Pulse shape tuning (6)
- **Pedestal run**
  - Pedestal and noise value for DB upload (7)
- **APV latency scan**
  - Synchronize tracker with LHC clock (8)
- **Fine tuning of pulse shape sampling**
  - Tune to 1ns level (9)



After this procedure, detector is ready for data taking

SST: hardware performance

Each test of the commissioning procedure is used also to identify the fraction of working hardware components:

- Electrical cabling: non answering I2C channels due to Power Supply Unit (PSU) problems
- Optical cabling: broken fibers
- Timing run: faulty PLL's related to PSU problems
- Pedestal run: high noise related to HV problems

Fraction of SST working hardware

TIB/TID	TOB	TEC+	TEC-
97%	98.0%	99.2%	98.3%

Some modules have been recovered after intervention in the service cavern but they were not included in DAQ since they needed to be re-commissioned

During the shutdown work is already planned (and partially done) to recover a significant fraction of faulty hardware components

Cosmic data taking

SST included in CMS for cosmic data taking since July 2008

- Conditions: magnetic field on/off, different trigger condition and rates
- Purpose: optimize full CMS detector performance
- Debug any existing problem

Results from cosmic events with magnetic field at 3.8T

- Continuous data taking for about four weeks with CMS magnet on
- About 280 M events collected
- Average trigger rate ~550Hz
- ~ 7.5 M tracks in SST

Tracker operation

- Silicon Strip Tracker in ~95% of the data taking time
- Temperature: sensors at 20-30 ºC
- Few inefficiencies due to
  - Cooling plant problems (trips or time needed for coolant fluid refilling)
  - Power Supply system temporary failure

SST: Control & Safety Systems

The Detector Control System (DCS) handles control, low and high voltages, as well as fast ramp-down in case of unsafe conditions detected in the experiment cavern

- Power on/off tracker
- Monitor environmental conditions
- Show all problems related to power supply
- Shutdown properly SST in case of problems

The Tracker Safety System (TSS) is designed to guarantee protection of the detector.

- takes action depending on the monitored values (temperatures, humidity and CMS cavern information)
- Provide interlocks in case of problems (temperatures, cooling, trips etc.)

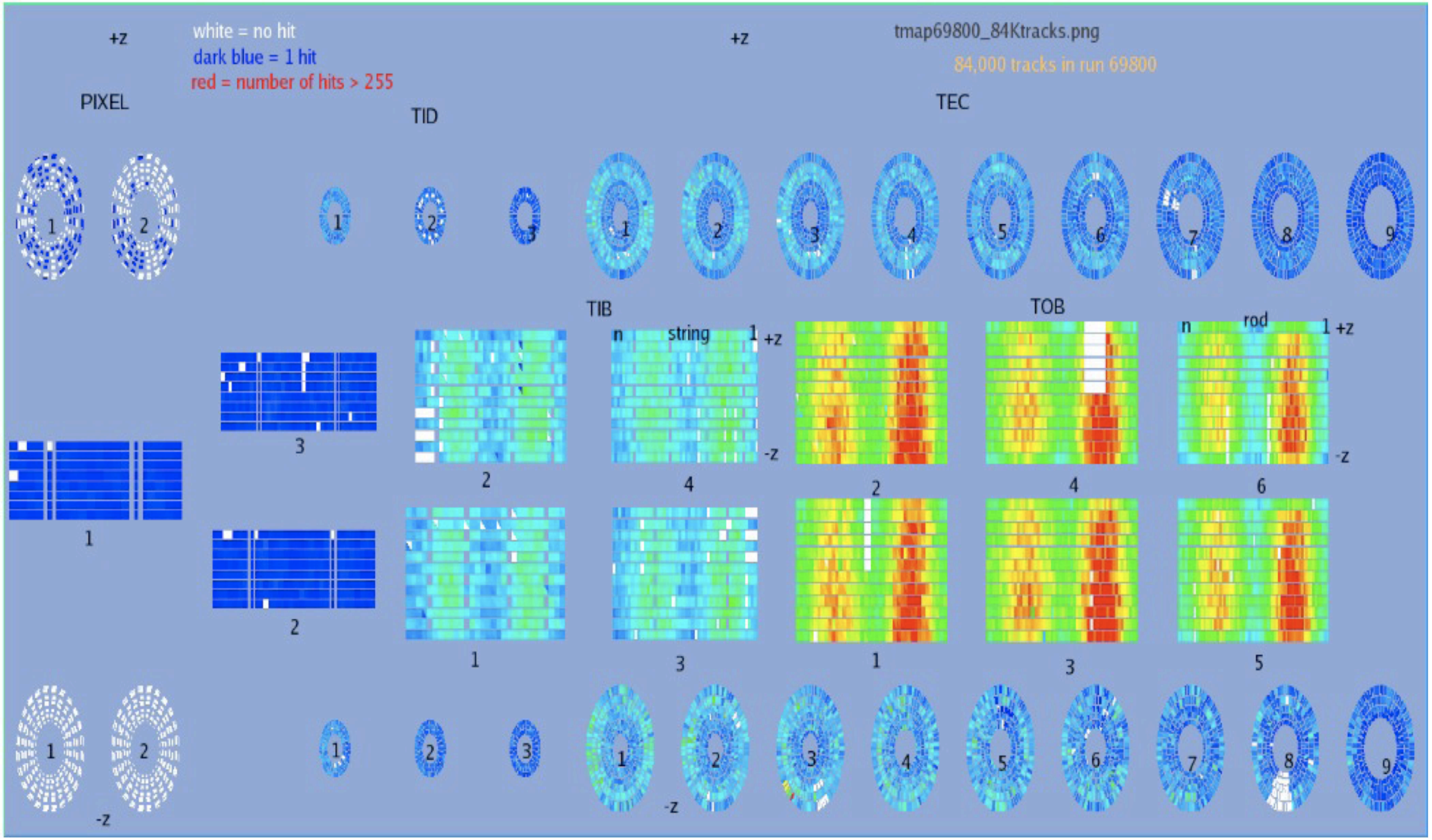
The system worked fine for the full period of data taking

Tool for DQM: Tracker Map

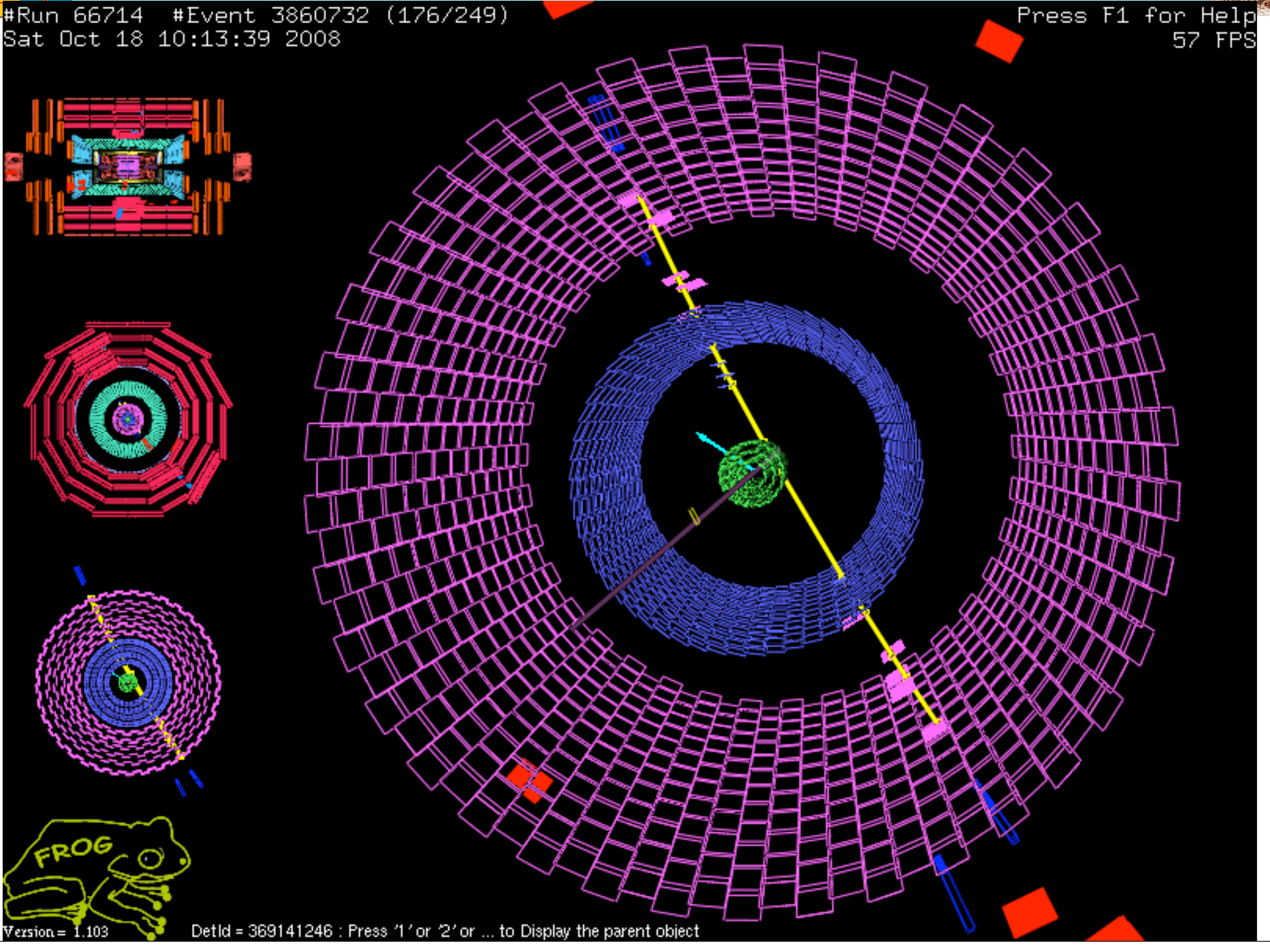
Useful tool to check the status of the full SST for each monitored quantity

White corresponds to “no hit”

It allows to easily identify problems in some geometrical region



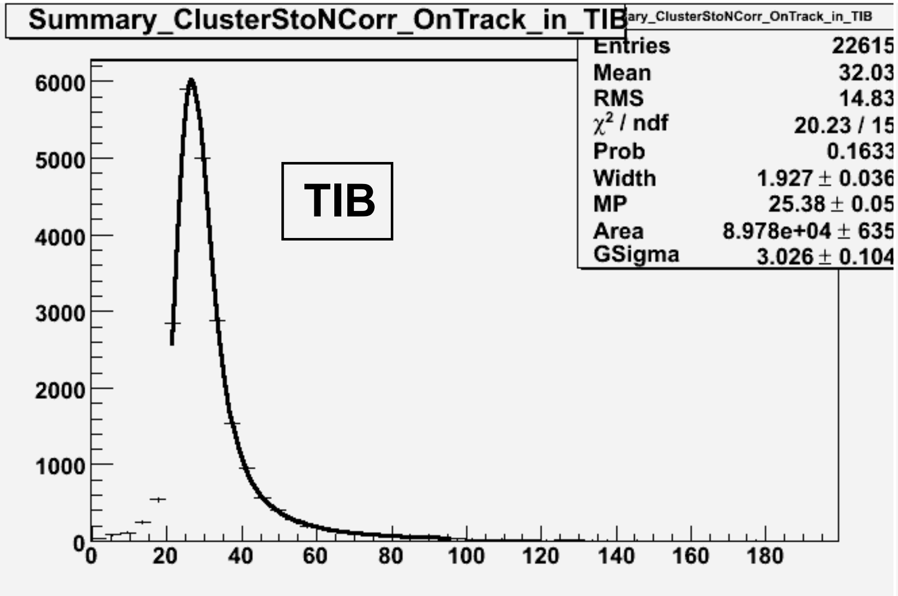
Event Display

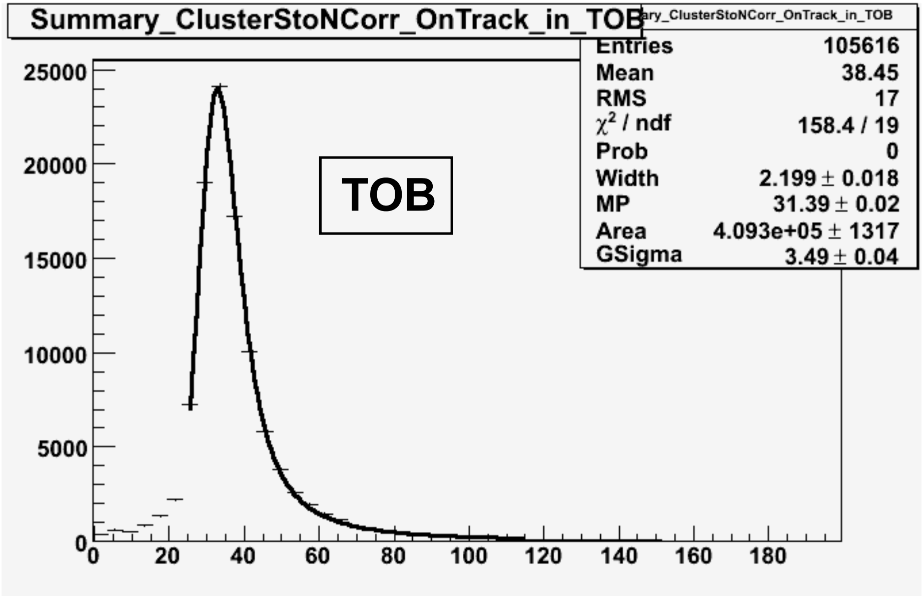


Tracker performance: Clusters

Signal-to-Noise ratio (S/N) for clusters associated to tracks. The track direction is used to correct the signal for the path length with respect to normal incidence

S/N value for TIB (320 um) and TOB (500 um): similar performance for thin and thick modules due to a different strip length: ~ 11 (~19) cm for TIB/TOB

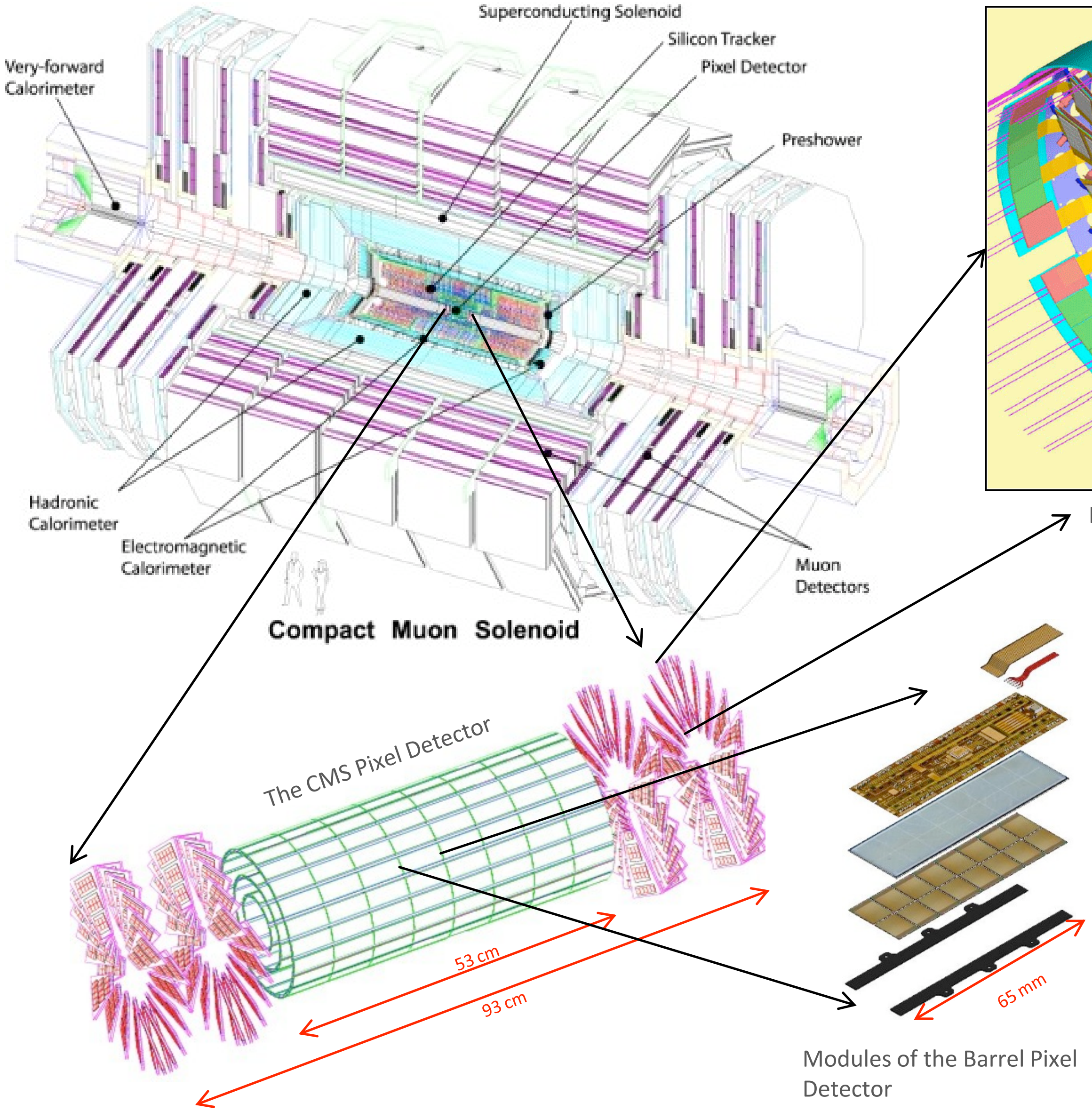




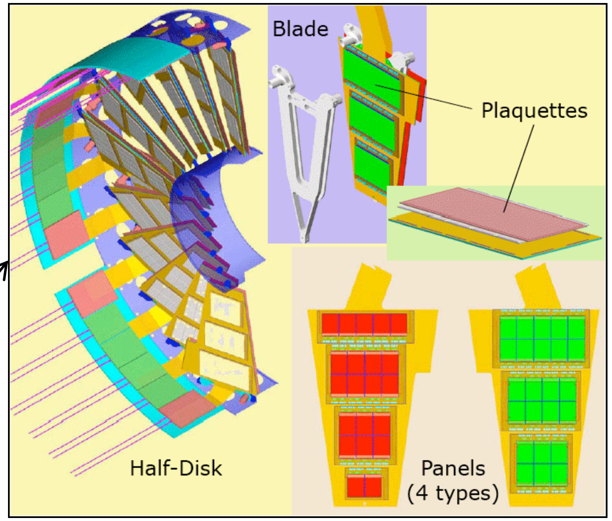
Most Probable Value (MPV) for each subsystem from the fit with a Landau function convoluted with a Gaussian
Value in agreement with expectation

	TIB	TOB	TID	TEC
S/N	25.4	31.4	27.5	30.4

The Pixel Detector in the Compact Muon Solenoid



Modules of the Barrel Pixel Detector



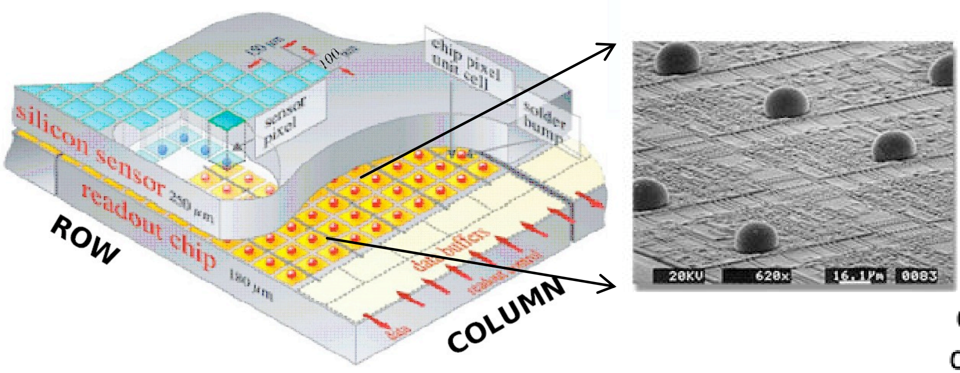
Panels of the Forward Pixel Detector

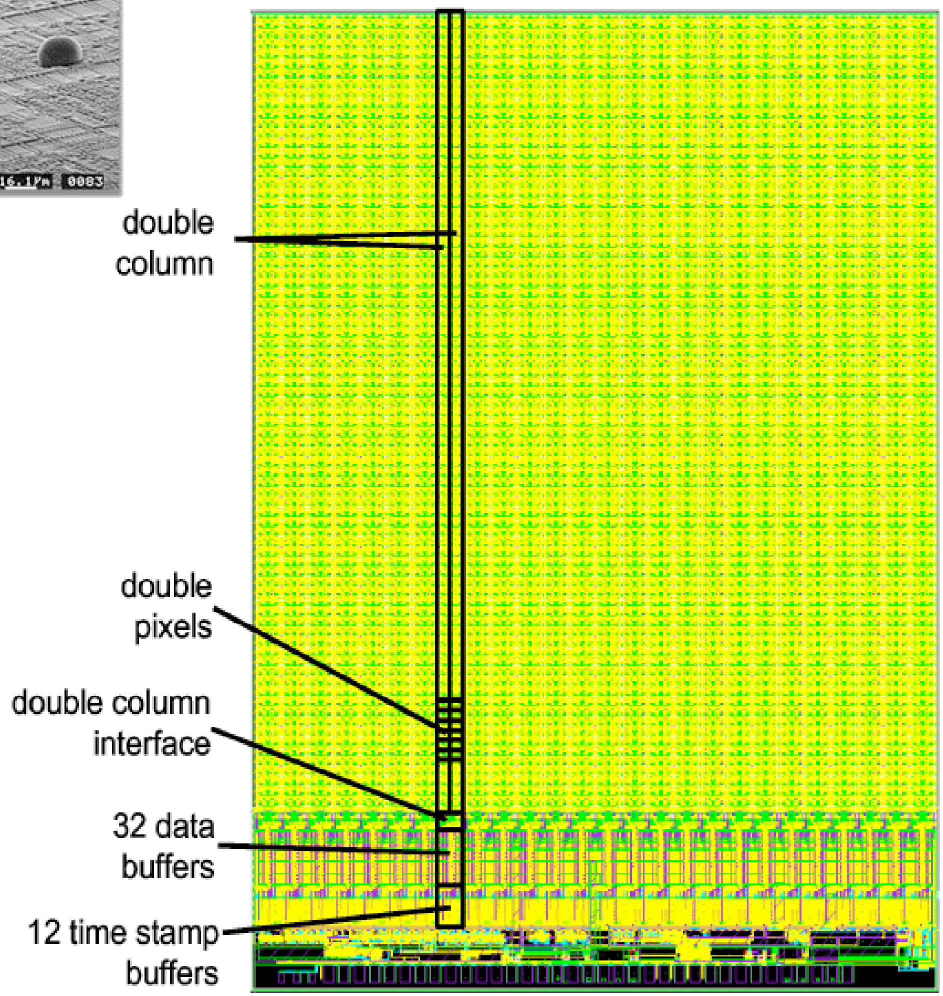
- Forward Pixel Detector (**FPix**) has two disks on each side at 34.5 cm and 46.5 cm
- FPix has 672 modules

- Barrel Pixel Detector (**BPix**) has 3 layers of radii 4.3 cm, 7.2 cm and 11.0 cm
- BPix has 768 modules

- Total of **~15,840 Readout Chips**

The Pixel Sensor and the Read Out Chip





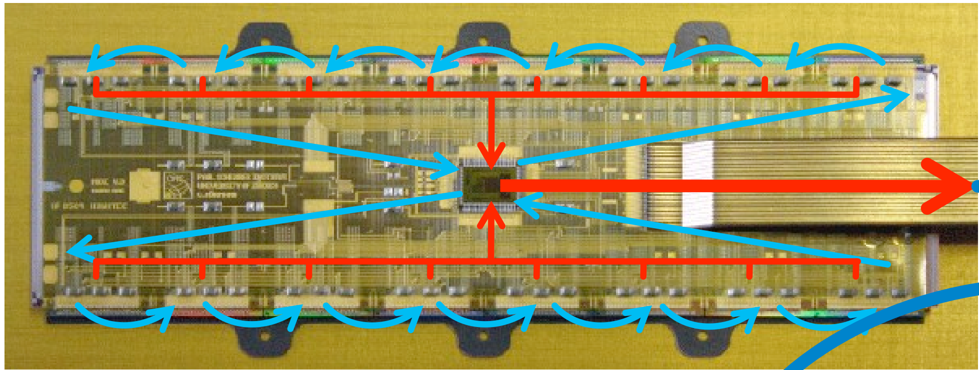
•ReadOut Chip (ROC) bump bonded sensor pixels.

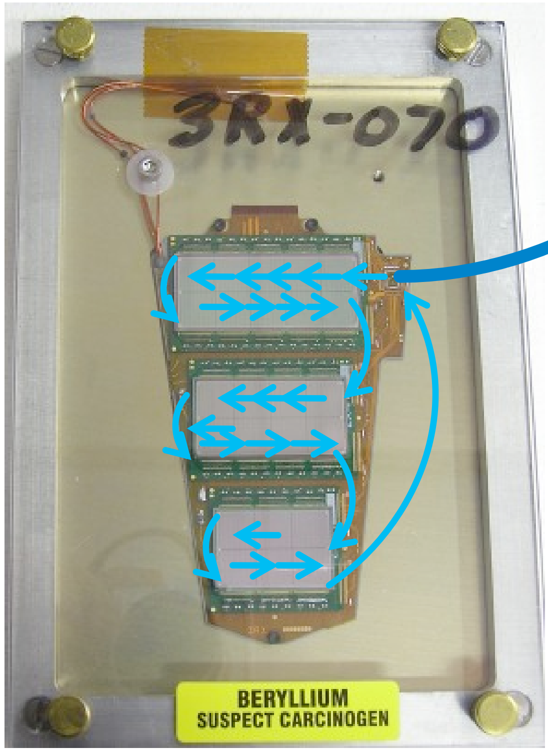
•52   80 = 4160 pixels per ROC
•15,840 ROCs
•66 million pixels

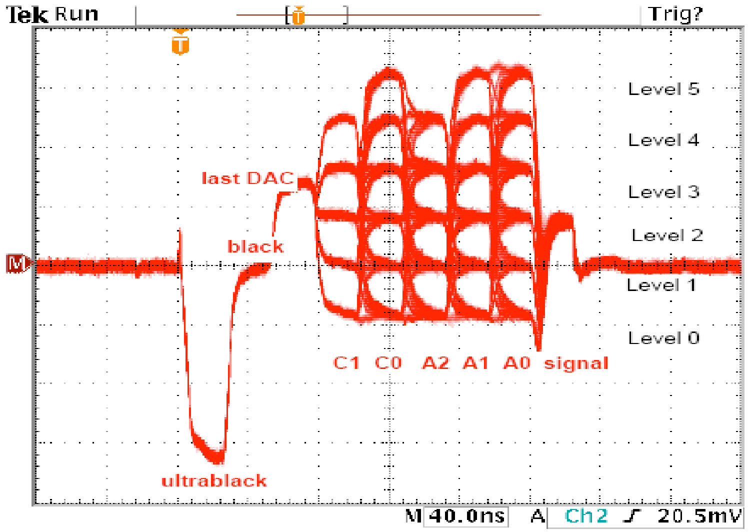
•Automatic zero-suppression

•Each pixel has a programmable threshold (adjusting this is called *trimming*)

Forward and Barrel Pixel Analog Readout







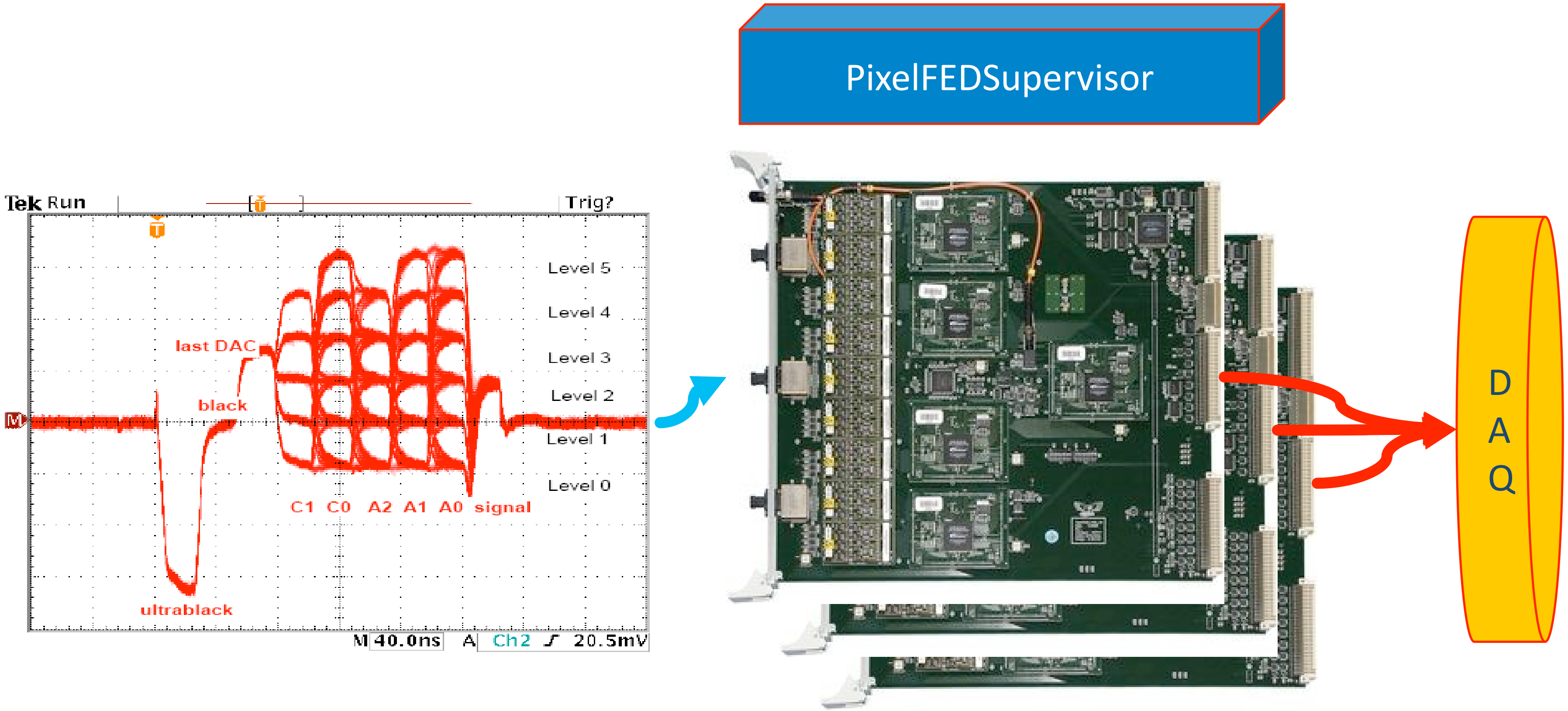
•On receiving a L1 trigger, the Token Bit Manager (TBM) initiates a Chinese-whisper of "token bits" that instruct each ROC to send its hit data to the TBM

•The signal from the TBM is electrical and analog. It encodes the ROC #, row and column and charge deposit of each pixel hit

•The electrical signal from the TBM is converted to optical by the Analog-Optical Hybrid (AOH)

Poster of J. C. Yun "Readout System of the CMS Pixel Detector" for details.

Digitization of Analog Readout with the Front End Driver



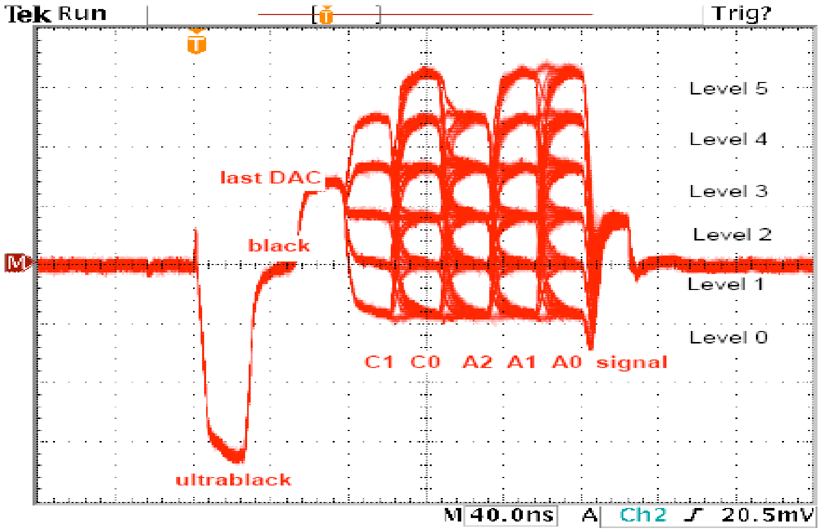
•Pixel Front End Driver (FED) digitizes analog signals given the level thresholds for decoding.

•One crate of FED boards is controlled by one PixelFEDSupervisor application. 40 FEDs in Pixels.

•FEDs send digitized data down S-Link cables to the Data Acquisition System (DAQ).

•FED data may also be read out via VME by the PixelFEDSupervisor.

Address Levels Calibration during Second Commissioning Phase



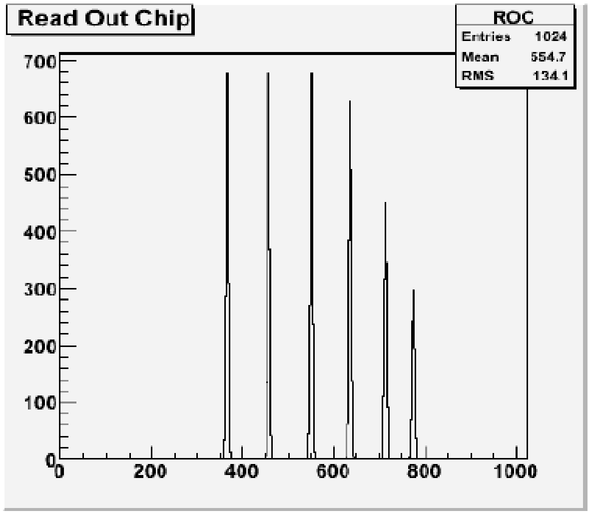
The analog signal from the TBM

Address Levels Calibration

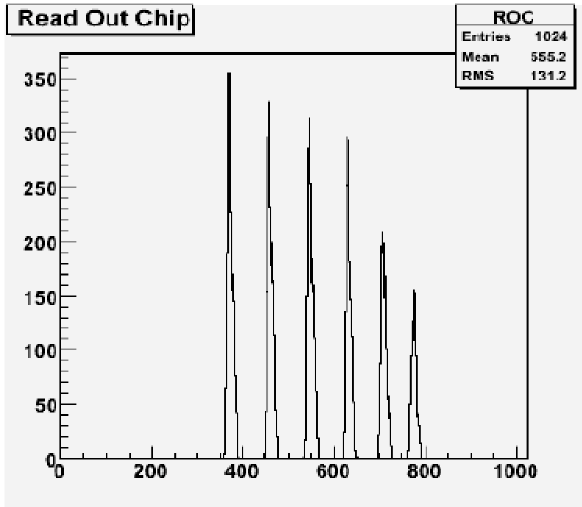
For the FED to decode the analog output of the TBM, it must know the address level thresholds.

Address level peaks may get smeared out when:
•The FED samples the signal at the wrong time
•The baseline is jittery due to unclean optical fibers

Good separation: rms is ~2.5 ADC



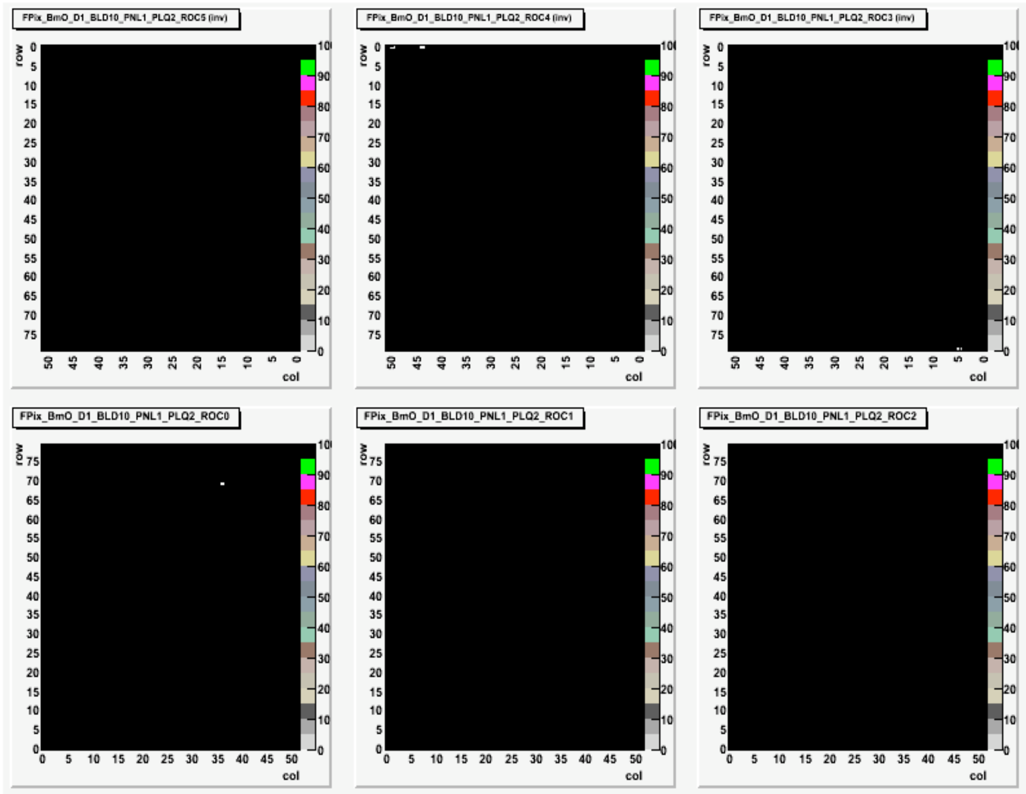
Poor separation: rms is >5 ADC



Pixel Alive Scan during Second Commissioning Phase

Pixel Alive

Inject charge repeatedly into each pixel and see how often they respond.
Build up an efficiency map and identify defective pixels.



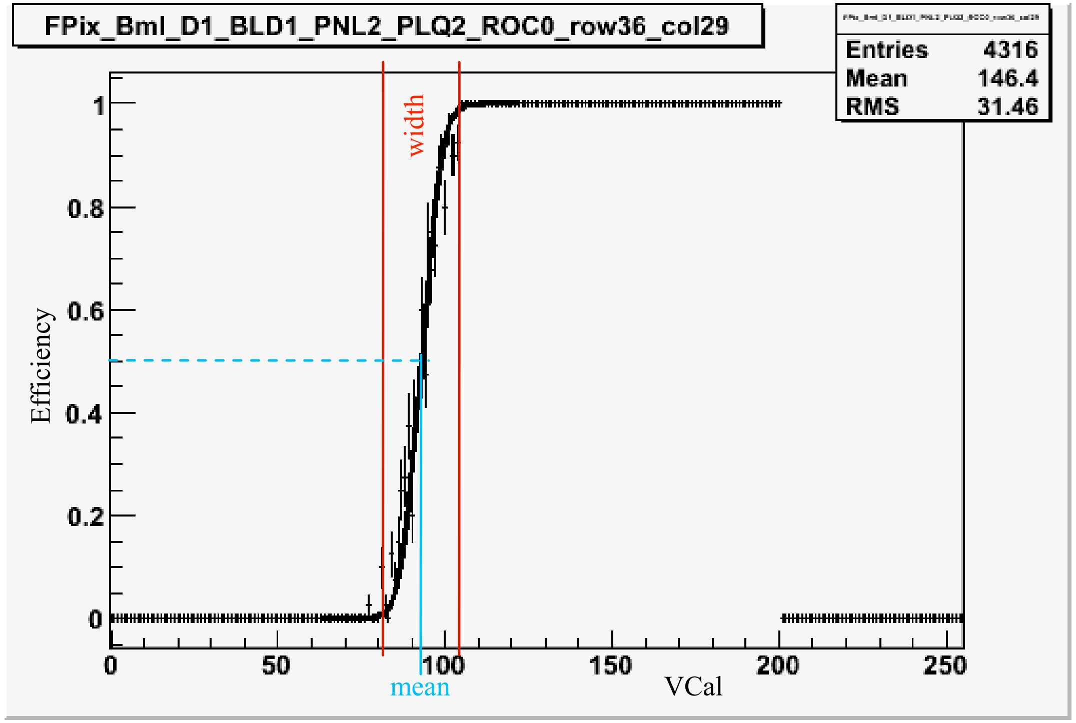
Dead Pixels

0.010% of BPix
0.015% of FPix

S-Curve Calibration during Second Commissioning Phase

S-Curve Calibration

The charge injected into each pixel for calibration, governed by *VCal*, is varied.
The efficiency of pixel response against the change in *VCal* gives us an S-Curve

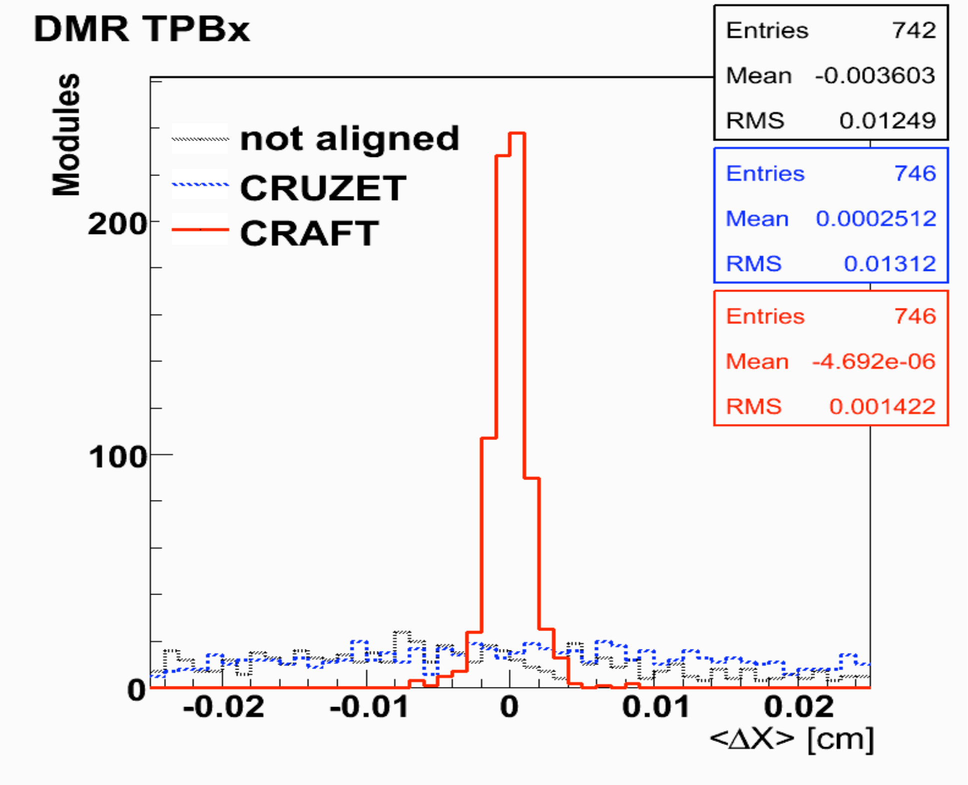


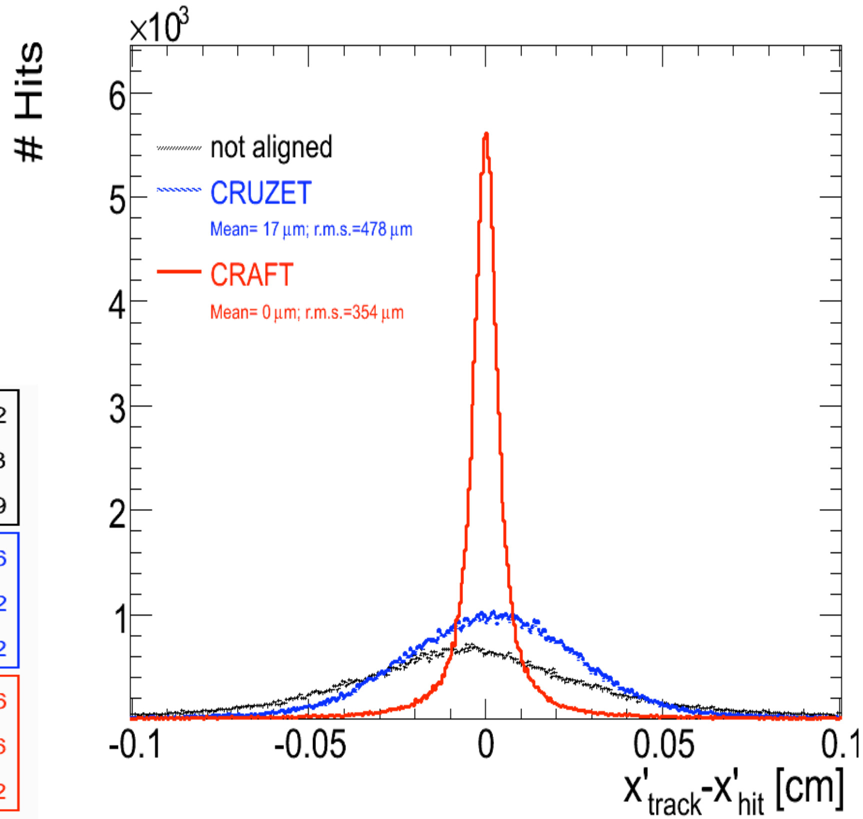
•The *VCal* corresponding to 50% efficiency is the **threshold** of response.
•The width of the turn-on region is a measure of the pixel's **noise**.

•One unit of *VCal* is roughly **65 electrons**.

Track Quality after Alignment with Cosmic Muons

- **CRUZET** = Alignment with Cosmic Run at Zero Tesla
- **CRAFT** = Alignment with Cosmic Runs at Four (3.8) Tesla
- **Residual** = Distance between expected hit and reconstructed hit
- **DMR** = Distribution of Median of Residuals





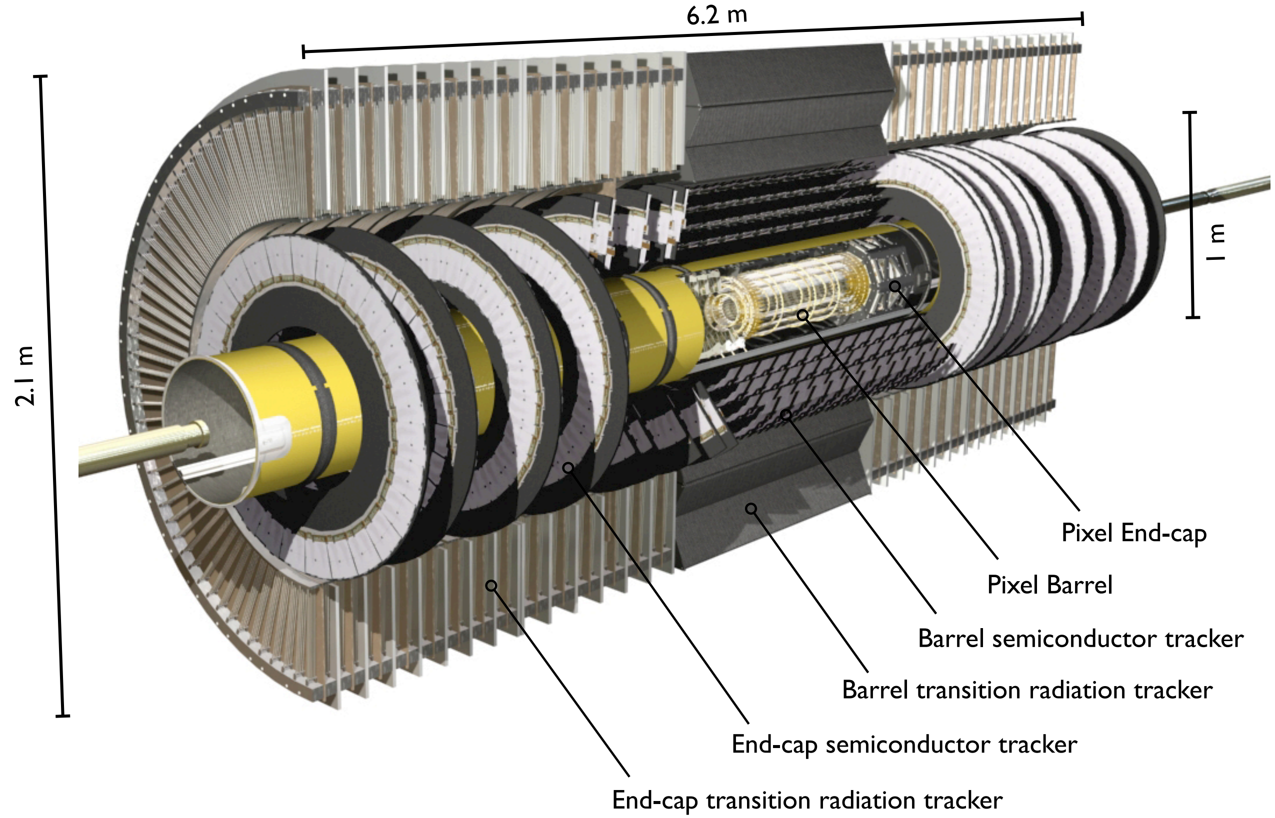
Barrel Pixels x-residuals

Design Resolution of **10 µm**
DMR RMS is **14 µm**

ATLAS Tracker

ATLAS Inner Detector tracking system

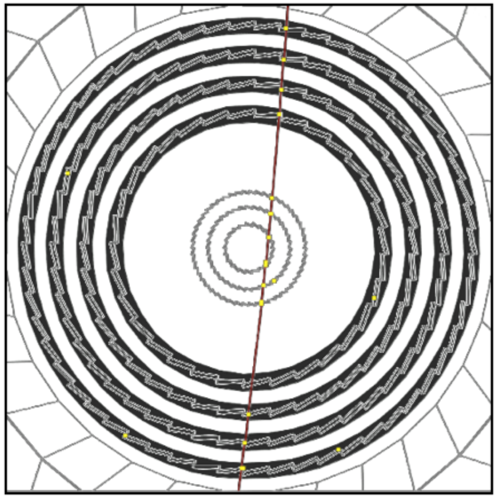
- Hermetic and robust pattern recognition
- Excellent momentum resolution
- Primary and secondary vertex measurements for charged tracks

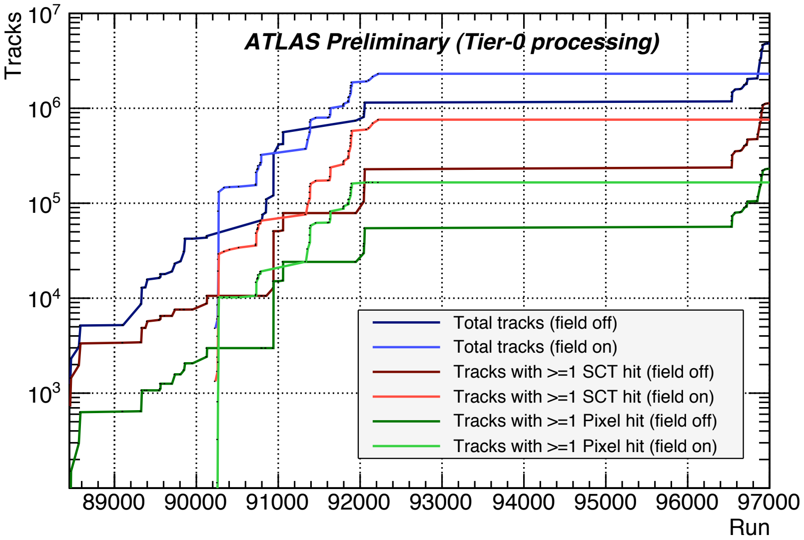


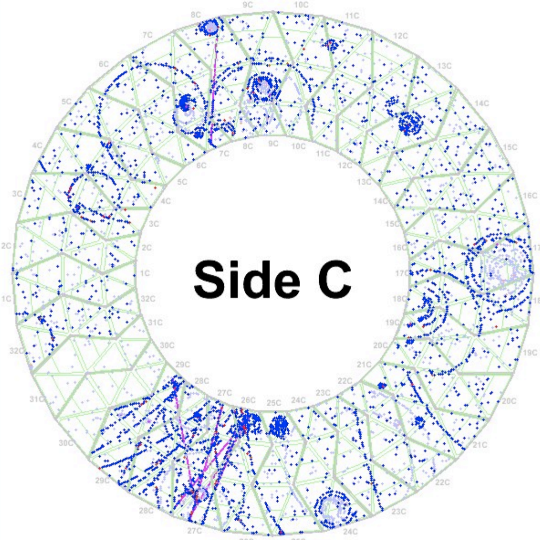
Commissioning Cosmic rays

- Global cosmic ray data taken in fall 2008
- Cosmic data with magnetic field :
  - 2.6 Million tracks
  - 880k ID tracks with SCT hits
  - 190k ID tracks with Pixel hit
- Cosmic data without magnetic field:
  - 5 Million tracks
  - 1.15 Million tracks with SCT hits
  - 230k tracks with Pixel hits

October 18th 2008 cosmic ray in the Inner Detector



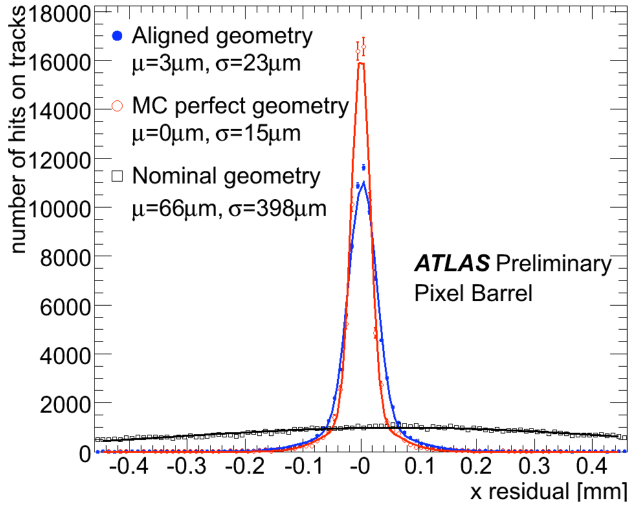


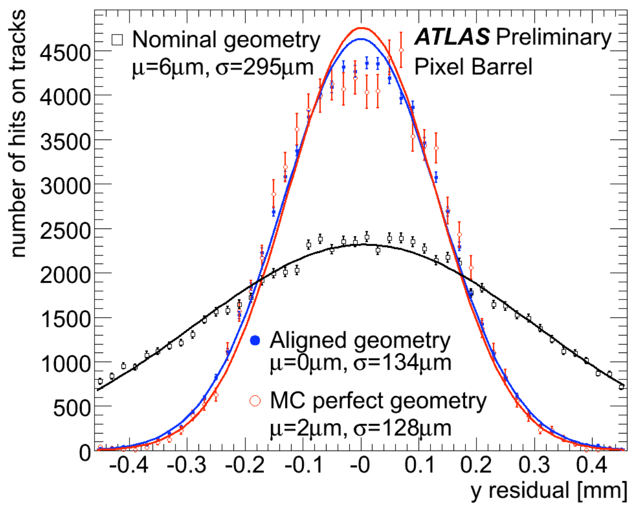


Event with tracks from cosmic particles observed in the ATLAS TRT Barrel (Aug 2008)

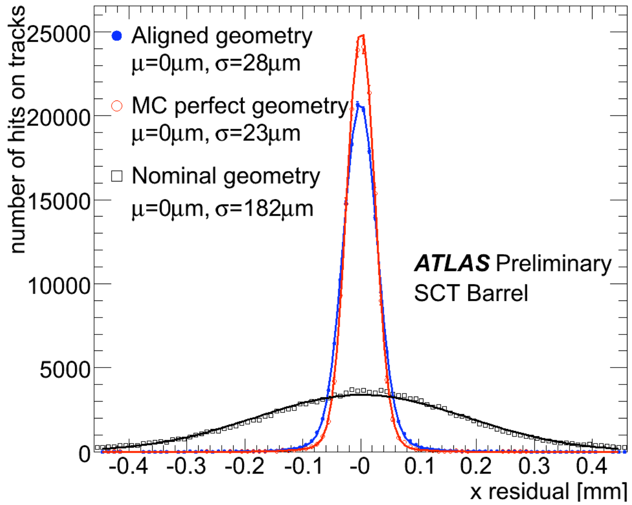
Alignment results with real cosmics

Pixel residuals

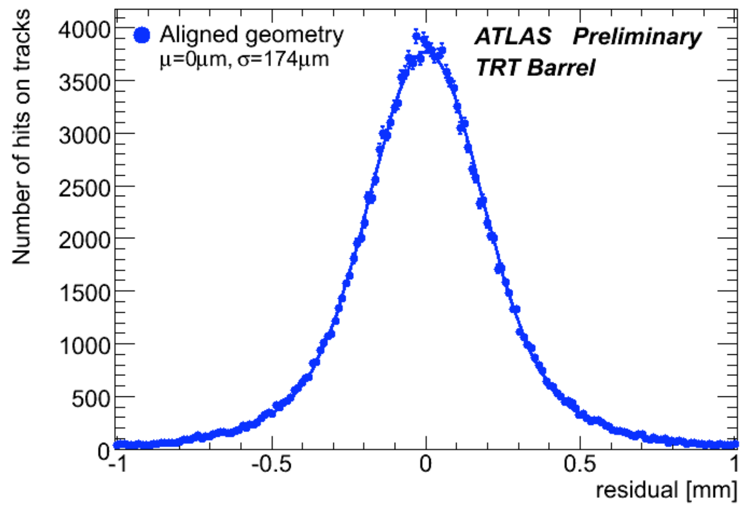




SCT residuals

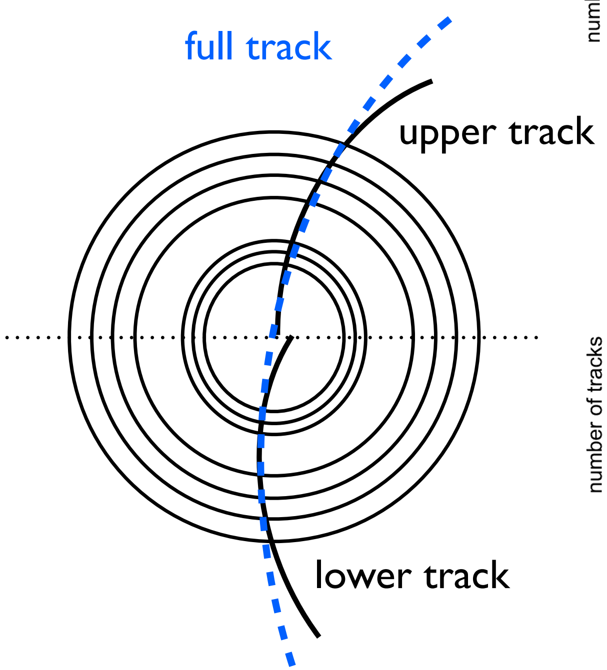


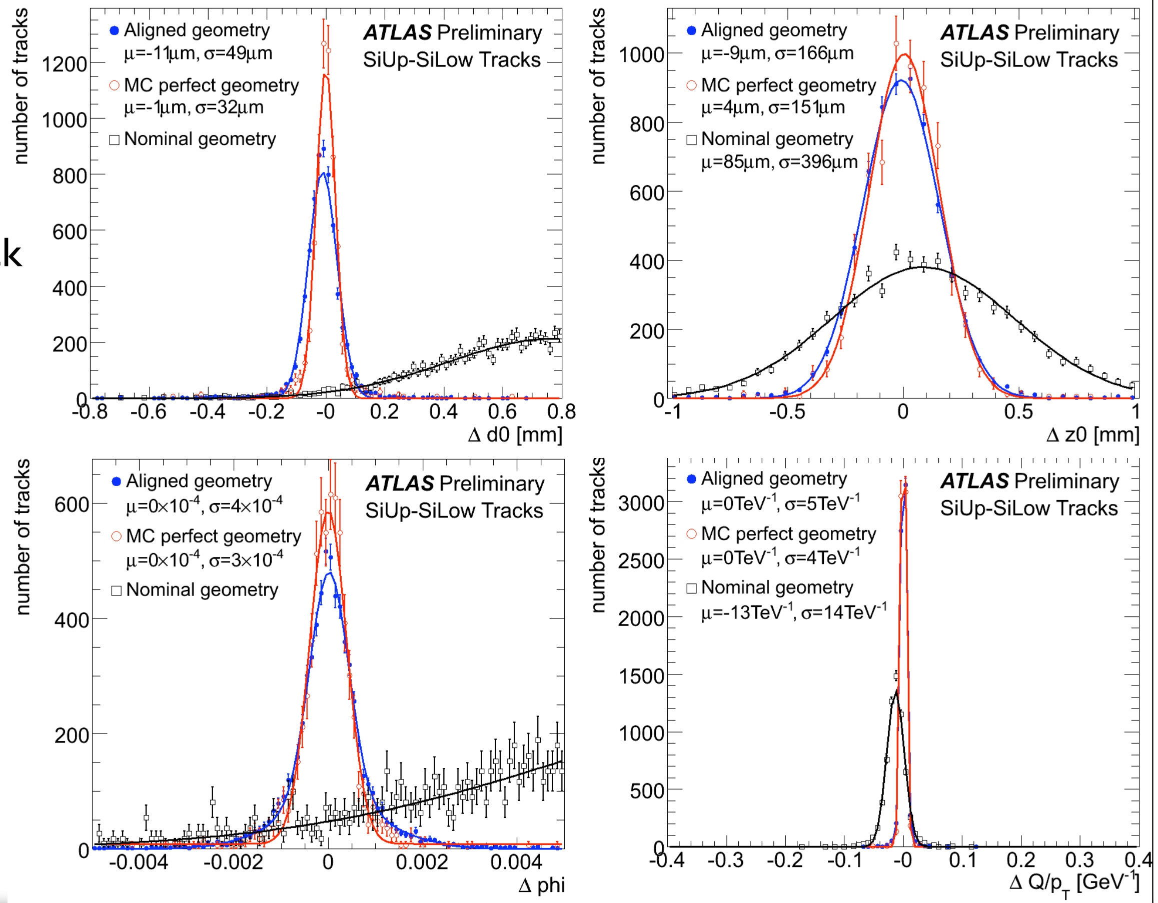
TRT residuals



Alignment validation with real cosmics

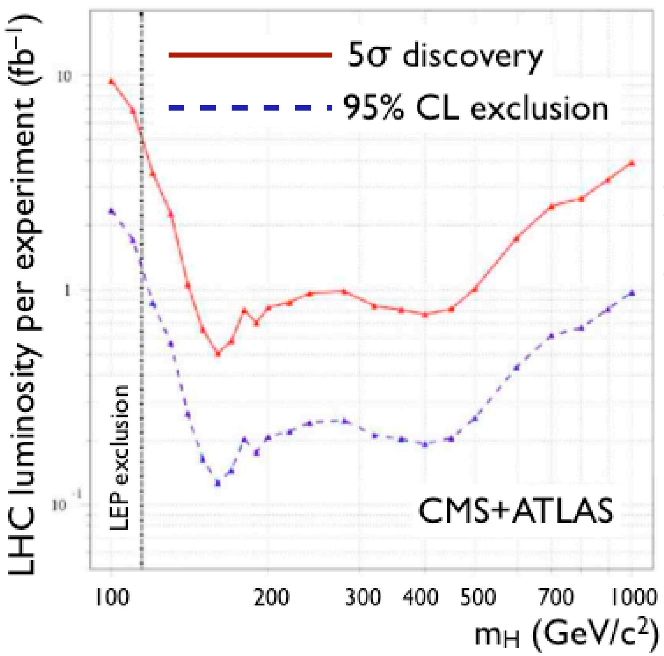
- Track parameter resolution:
  - A full ID track is splitted in two segments: upper and lower
  - The two tracks segments are refitted
  - The difference between the track parameters of the two tracks segments is used to validate the alignment

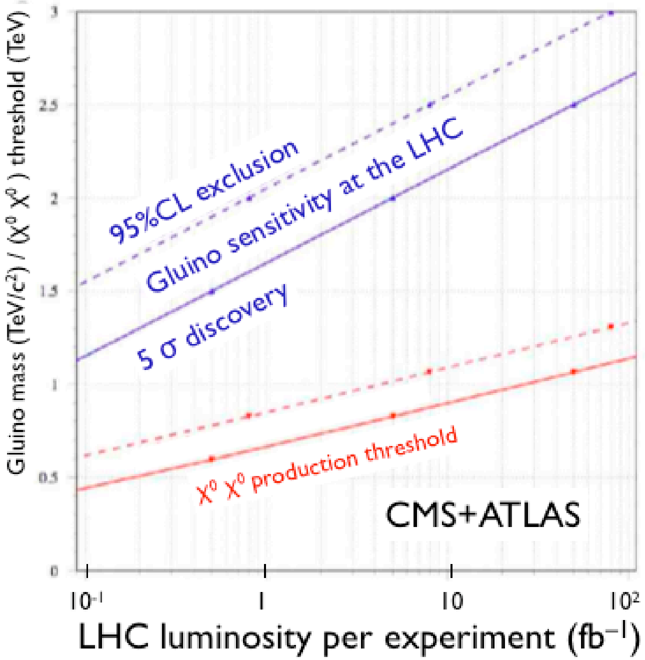




Why SLHC?

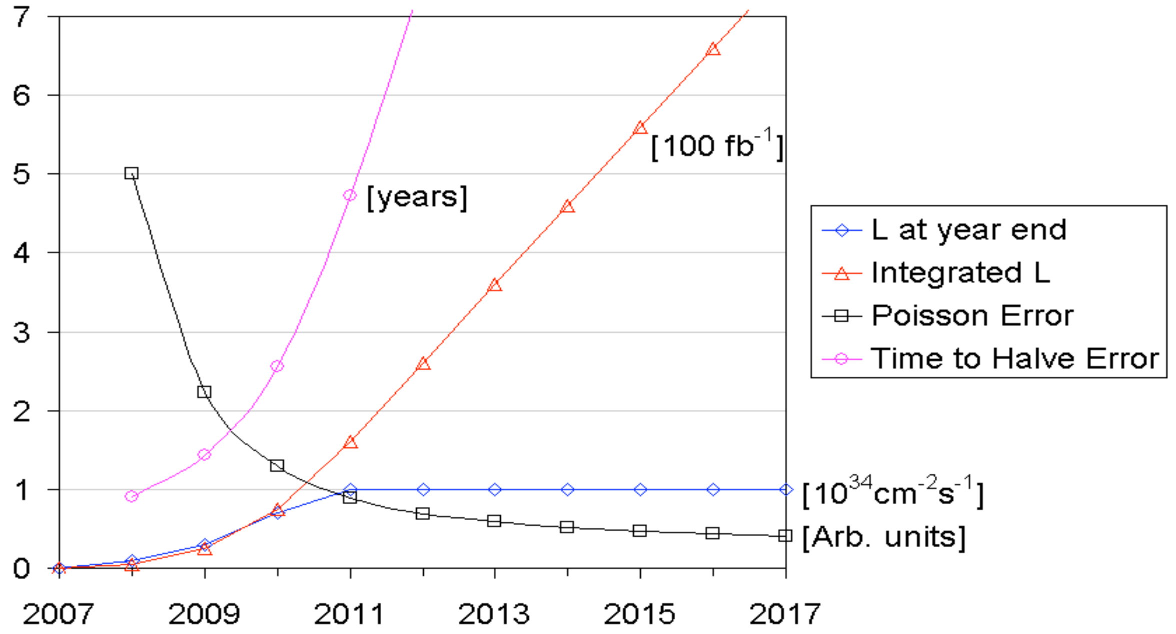
- **By 2012-13 we should already have a good picture of TeV scale physics**
  - **However more luminosity would be needed to explore further the phase space or to establish the possible discoveries done**



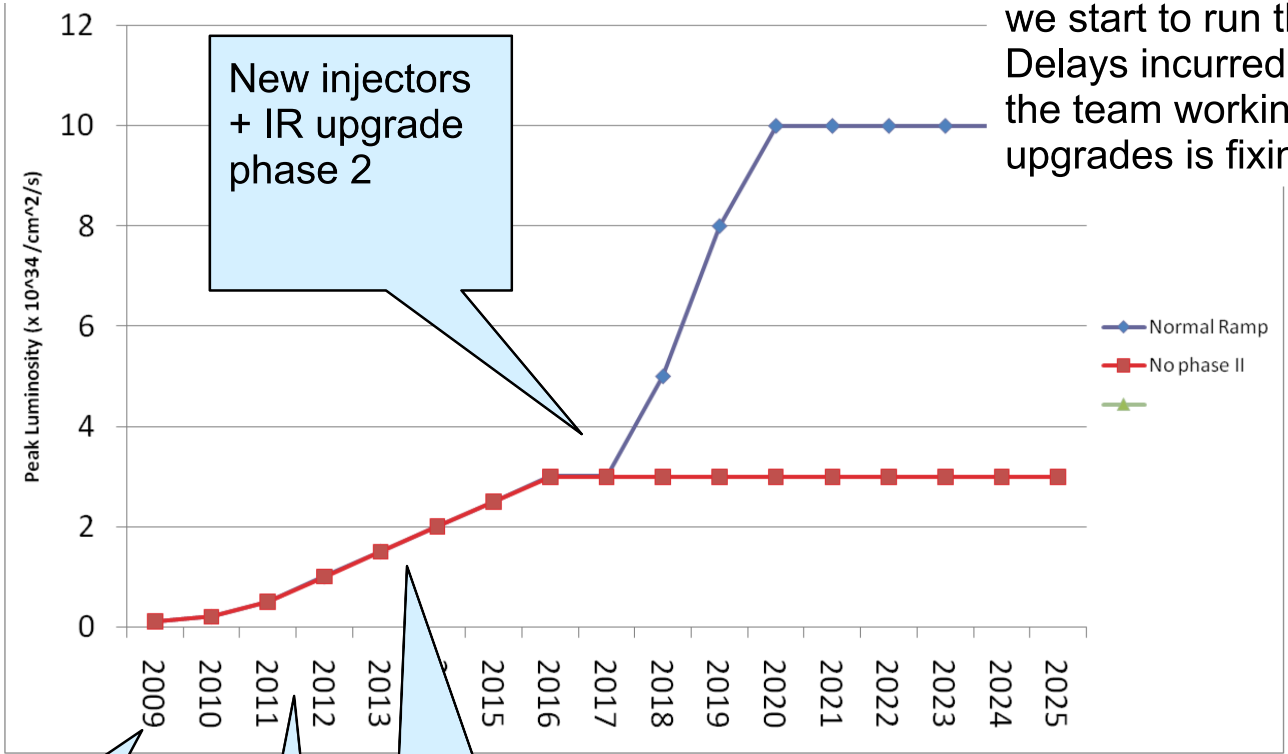


Why (and which) S-LHC?

- **CERN – TH/2002-78 Physics Potential and Experimental Challenges of the LHC Luminosity Upgrade**
  - **Conclusion 1:**
    - **Increasing the Energy of the LHC is very attractive, but very Expensive**
    - **Increasing the Luminosity by a factor of 10 could be possible**
  - **Conclusion 2:**
    - **Increase Luminosity by Factor 10**



LHC Luminosity Upgrade



New injectors + IR upgrade phase 2

Early operation

Collimation phase 2

Linac4 + IR upgrade phase 1

Revisit the long term when we start to run the LHC Delays incurred because the team working on upgrades is fixing dipoles

This schedule will be revised shortly to reflect situation after 3-4 incident

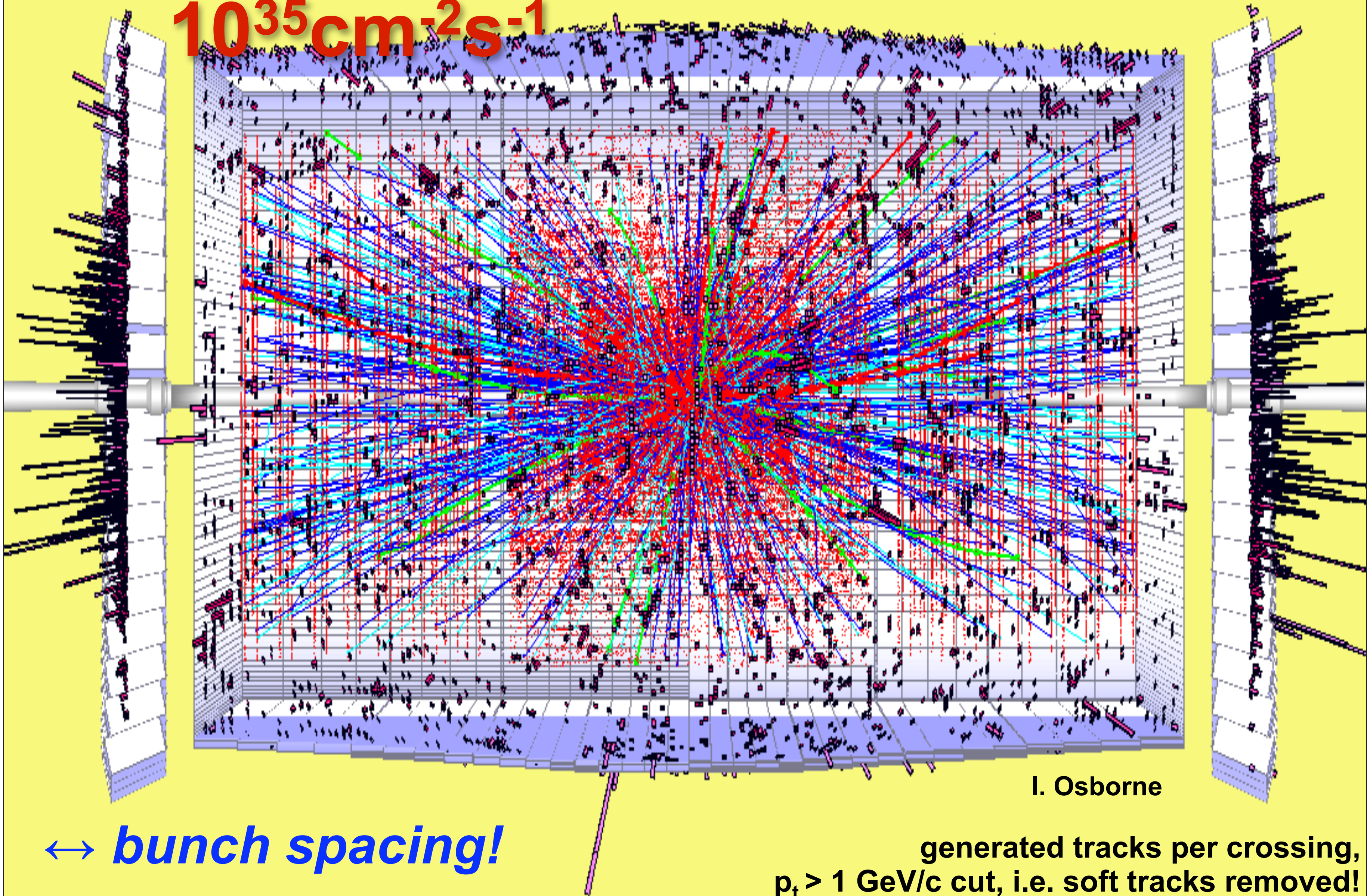
Implications for the Tracker

- **At 10^{35} cm^{-2} s^{-1}~400 interactions per bunch crossing**
  - About 12k primary tracks per bunch crossing (25 ns) in the Tracker volume $|\eta|<2.5$ ...
    - ...plus any other coming from γ conversions and nuclear interactions
  - **factor ~20 larger wrt LHC**
  - **higher radiation**
  - **larger occupancy**
- **Main issues for the Tracker**
  - **radiation hardness of up to 10^{16} n_{eq} cm^{-2} in the innermost layers**
    - **R&D for ultra radiation hard detectors: 3D-silicon, planar (n in p), diamond**
  - **data rate: output data rate at innermost layer ~ 4xLHC**
    - **fast low power electronics and data links**
  - **material budget**
    - **interplay between: resolution, pattern recognition, tracking**
    - **less material, new powering concepts (serial, DC-DC)**

detector pile up

< 200-300 events/#ing!?

$10^{35} cm^{-2} s^{-1}$

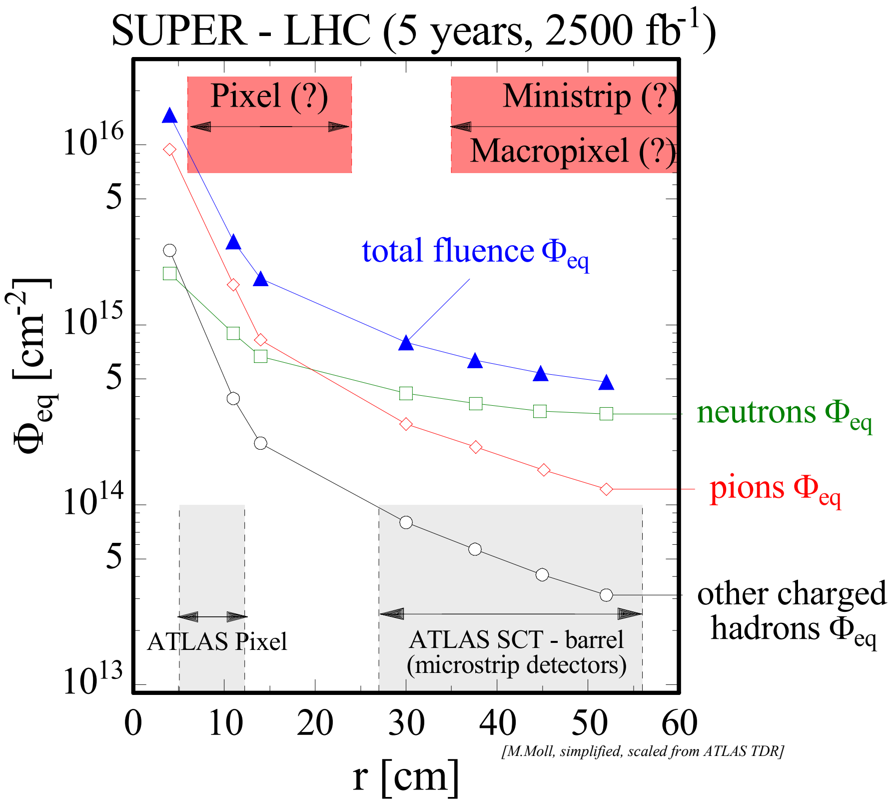


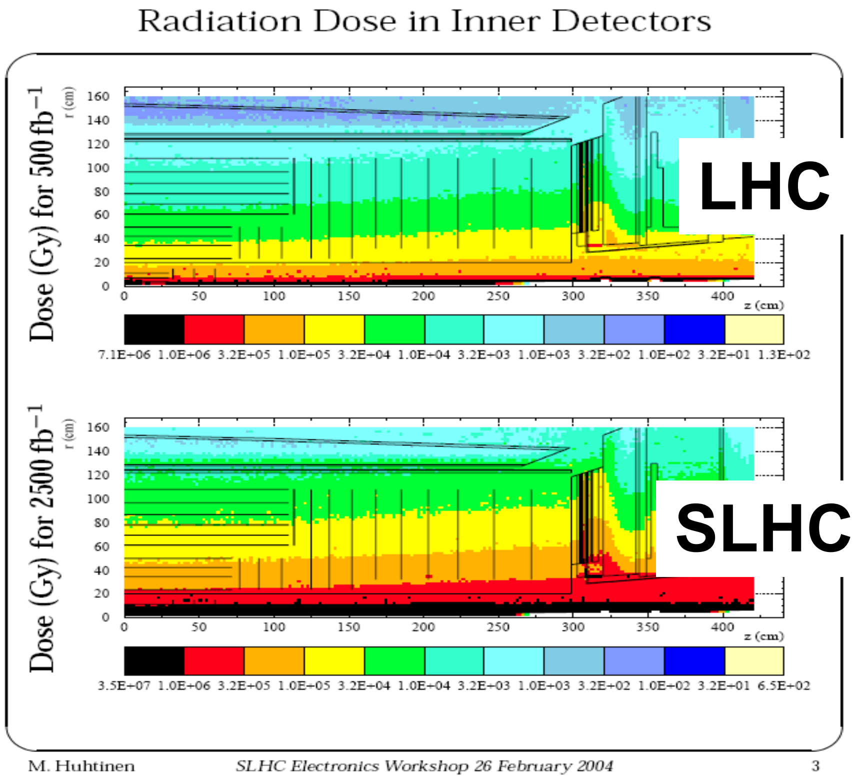
I. Osborne

↔ bunch spacing!

generated tracks per crossing,
p_t > 1 GeV/c cut, i.e. soft tracks removed!

Radiation Issues for SLHC



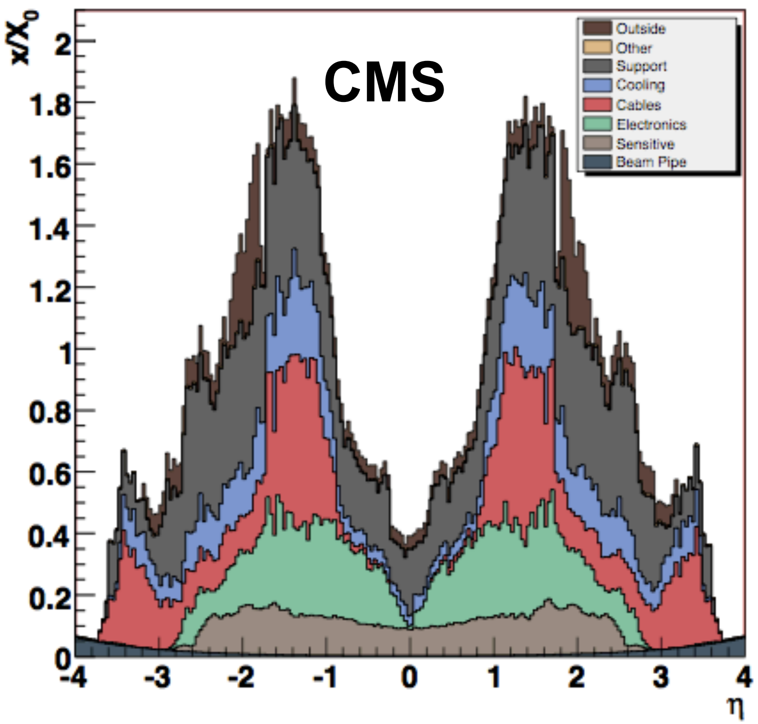


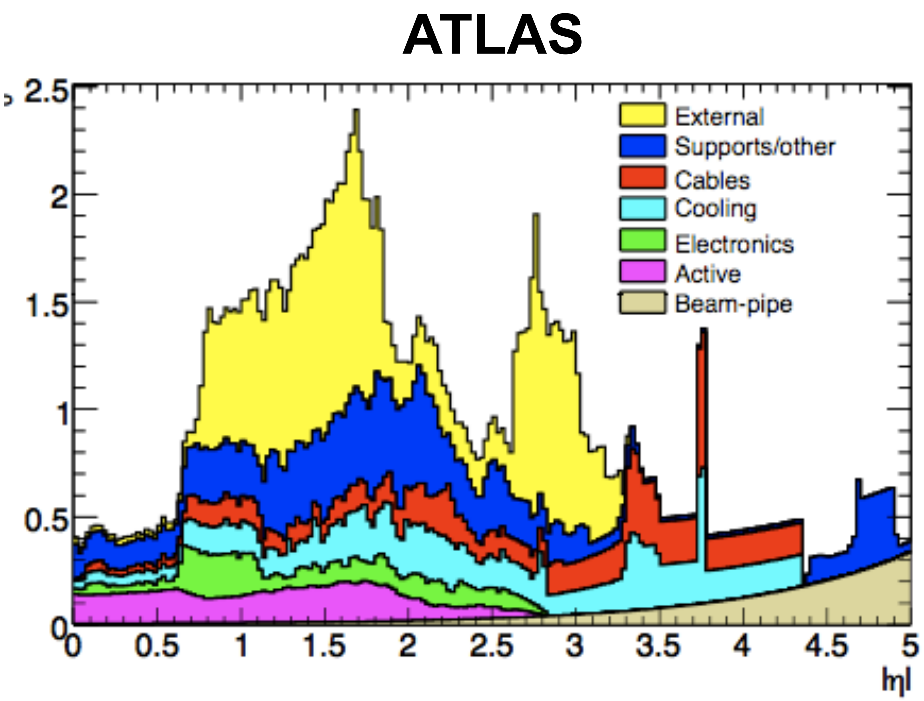
Can we improve Tracker for SLHC?

- At present no physics arguments (yet) to improve spatial and momentum measurement precision, but
  - strong general arguments to maintain tracking and vertexing performance
  - Heavy ion tracking simulations give encouraging performance
    - Track density similar to SLHC
    - Extra pixel layer would restore losses
- Sensors are one of many issues
  - Any new material technology must use large-scale commercial devices
- Electronic technology evolution will bring benefits
  - and also more complexity and much difficult work

Can we improve Tracker for SLHC?

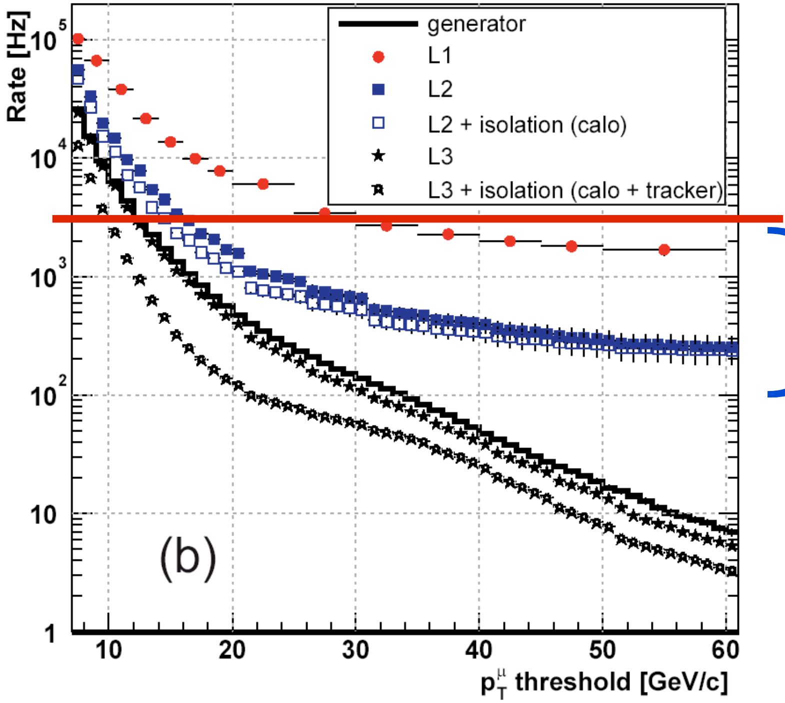
- **Material budget is weakest point**
  - e & γ conversions, hadronic interactions
  - Driven by power & cooling
    - pixels ~3.7 kW.m^{-2}, μstrips ~ 0.1–0.4 kW.m^{-2}
- **Then optimise layout for**
  - CPU-effective track finding & Triggering





Why tracker input to L1 trigger?

- **Single μ and e L1 trigger rates will greatly exceed 100 kHz**
  - **similar behaviour for jets**
    - **increase latency to 6.4μs but maintain 100 kHz for compatibility with existing systems, and depths of memory buffers**



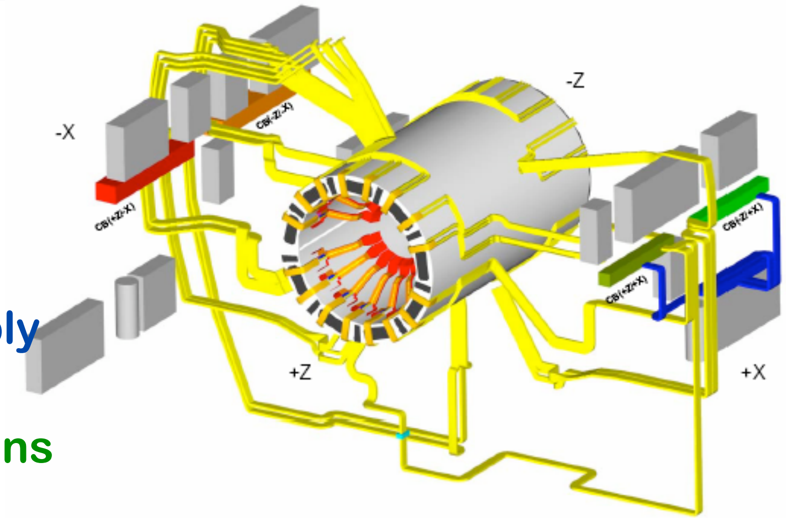
30 GeV: 30 KHz@10^{35}

Note limited rejection power (slope)
without Tracker information

$L = 10^{34}$ muon
L1 trigger rate

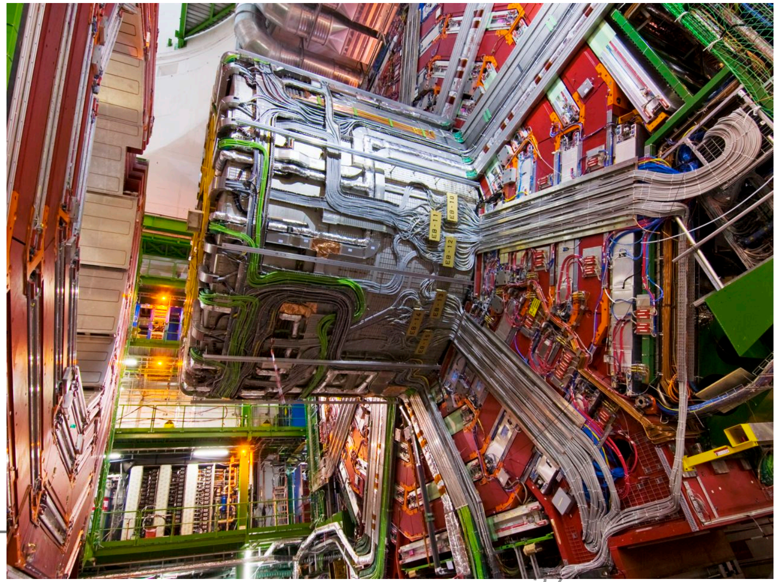
Constraints

- **Power & cooling services**
  - Complex, congested routes
  - Heat load of cables must be removed
  - $P_{cable} = R_{cable}(P_{FE}/V_s)^2$
  - Cable voltage drops exceed ASIC supply voltages
    - limited tolerance to voltage excursions
- **Installation was a huge, difficult job**
  - It is not considered possible to replace cables and cooling for Phase I or Phase II



$P_{FE} \approx 33kW$ I=15,500A $P_S = 300kVA$

However, CO_2 seems feasible for new pixel system and potentially for Phase II

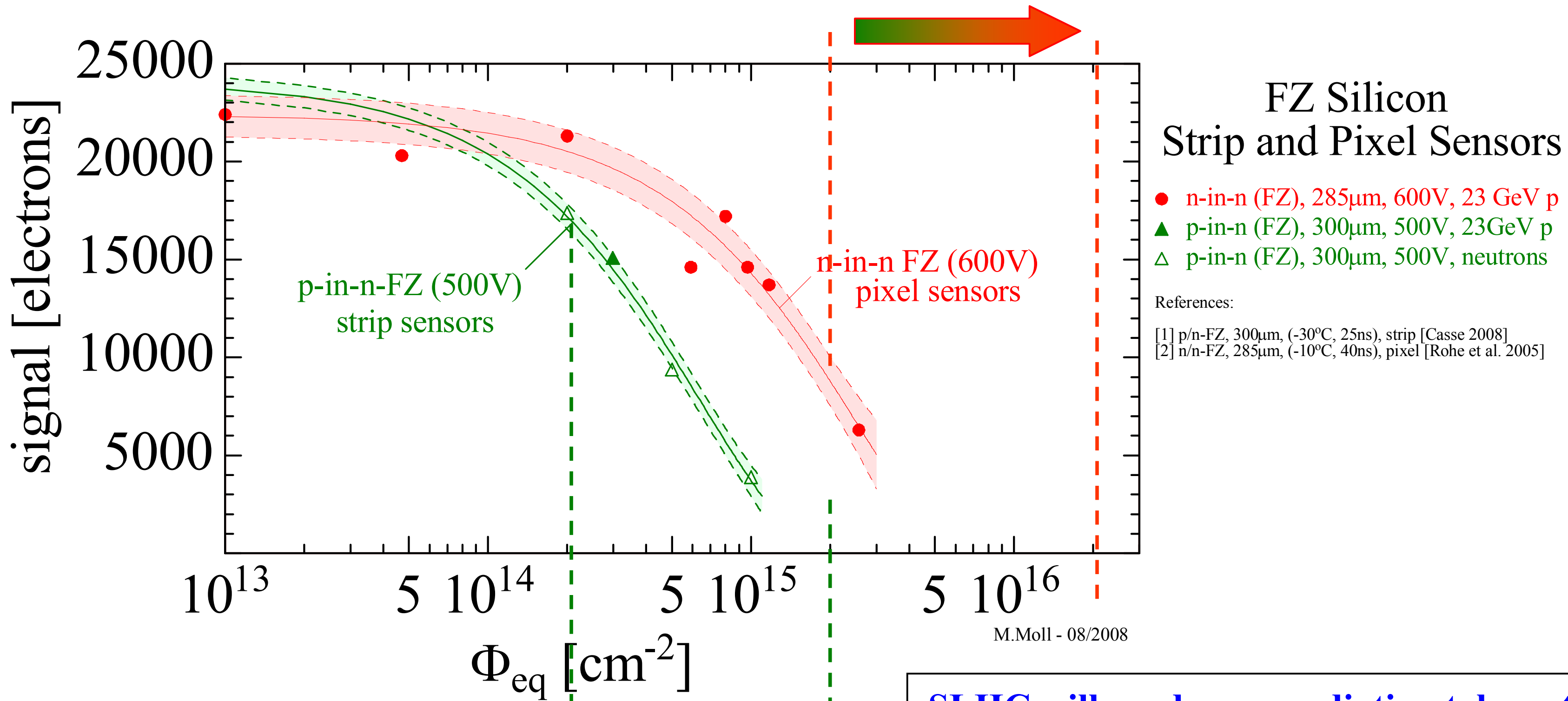


Sensors

Signal degradation vs fluence

Pixel sensors:

max. cumulated fluence for LHC and SLHC



Strip sensors:

max. cumulated fluence for LHC and SLHC

SLHC will need more radiation tolerant tracking detector concepts!

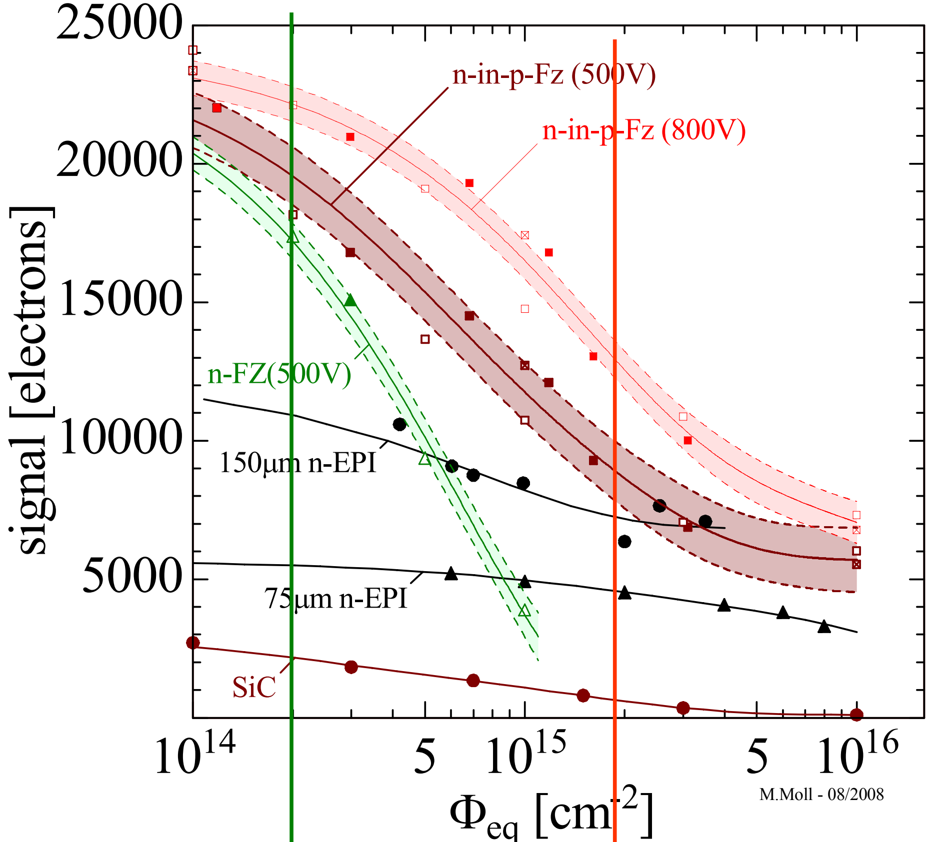
Boundary conditions & other challenges:

Granularity, Powering, Cooling, Connectivity, Triggering, Low mass, Low cost !

RD50 Silicon materials for Tracking Sensors

- **Signal comparison for various Silicon sensors**

Note: Measured partly under different conditions! Lines to guide the eye (no modeling)!



Silicon Sensors

- ● p-in-n (EPI), 150 µm [7,8]
- ▲ p-in-n (EPI), 75µm [6]
- ■ n-in-p (FZ), 300µm, 500V, 23GeV p [1]
- □ n-in-p (FZ), 300µm, 500V, neutrons [1]
- ⊠ n-in-p (FZ), 300µm, 500V, 26MeV p [1]
- ■ n-in-p (FZ), 300µm, 800V, 23GeV p [1]
- □ n-in-p (FZ), 300µm, 800V, neutrons [1]
- ⊠ n-in-p (FZ), 300µm, 800V, 26MeV p [1]
- ▲ p-in-n (FZ), 300µm, 500V, 23GeV p [1]
- △ p-in-n (FZ), 300µm, 500V, neutrons [1]

Other materials

- ● SiC, n-type, 55 µm, 900V, neutrons [3]

References:

[1] p/n-FZ, 300µm, (-30°C, 25ns), strip [Casse 2008]
[2] p-FZ,300µm, (-40°C, 25ns), strip [Mandic 2008]
[3] n-SiC, 55µm, (2µs), pad [Moscatelli 2006]
[4] pCVD Diamond, scaled to 500µm, 23 GeV p, strip [Adam et al. 2006, RD42]
Note: Fluenze normalized with damage factor for Silicon (0.62)
[5] 3D, double sided, 250µm columns, 300µm substrate [Pennicard 2007]
[6] n-EPI,75µm, (-30°C, 25ns), pad [Kramberger 2006]
[7] n-EPI,150µm, (-30°C, 25ns), pad [Kramberger 2006]
[8] n-EPI,150µm, (-30°C, 25ns), strip [Messineo 2007]

LHC → **SLHC**

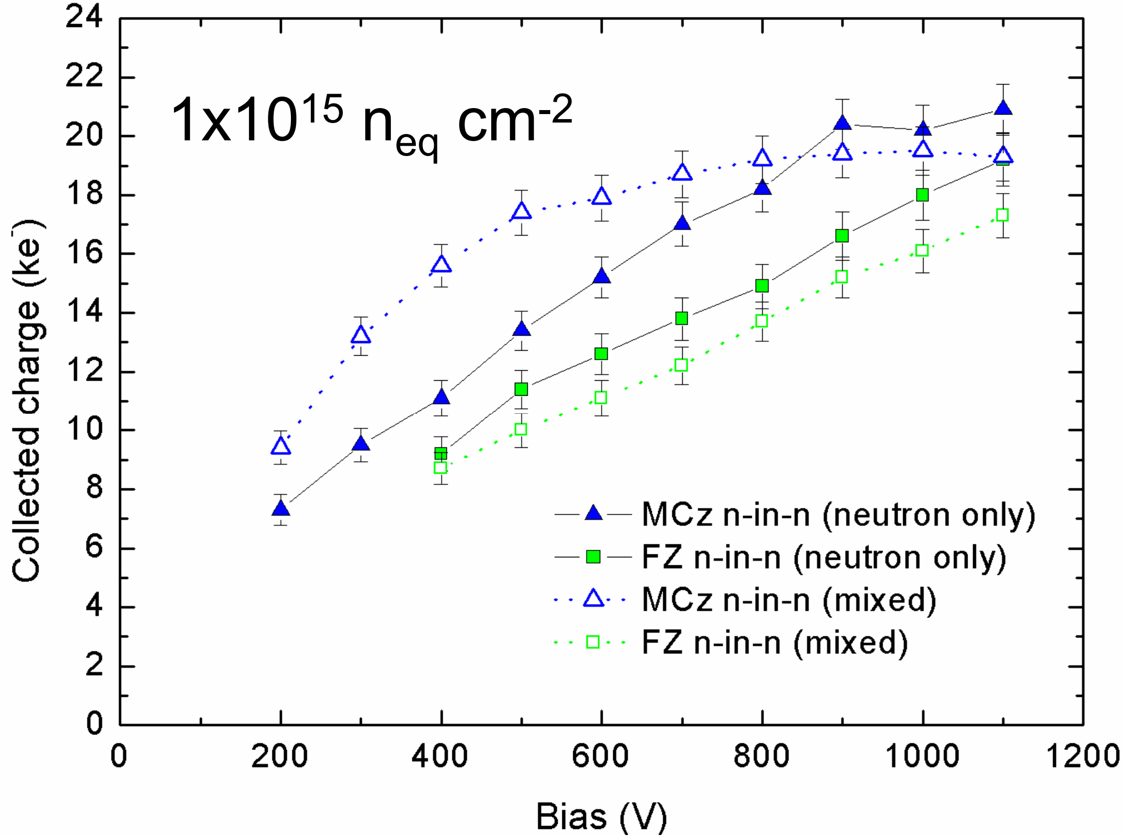
highest fluence for strip detectors in LHC: The used p-in-n technology is sufficient

n-in-p technology should be sufficient for Super-LHC at radii presently (LHC) occupied by strip sensors

RD50 Mixed Irradiations (Neutrons+Protons)

- **Both FZ and MCz show "predicted" behaviour with mixed irradiation**

  - **FZ doses add**
    - $|N_{eff}|$ increases
  - **MCz doses compensate**
    - $|N_{eff}|$ decreases

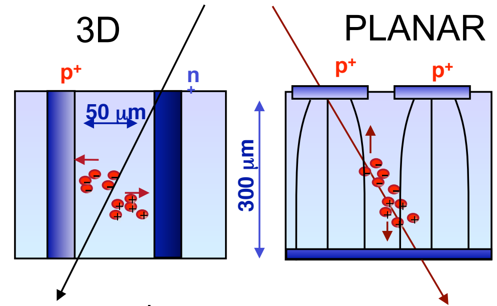


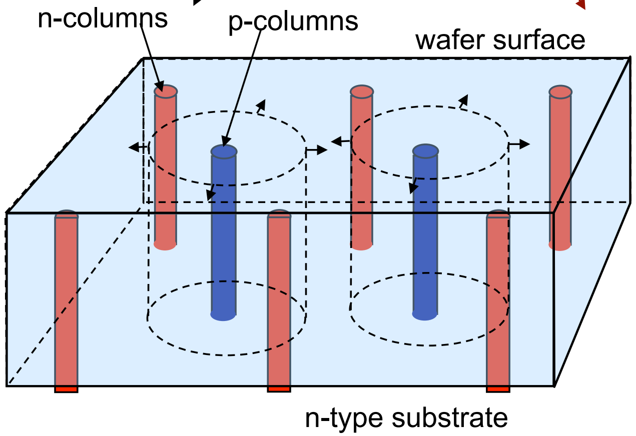
Needs further study with both nMCz and pMCz substrates and differing mixed doses

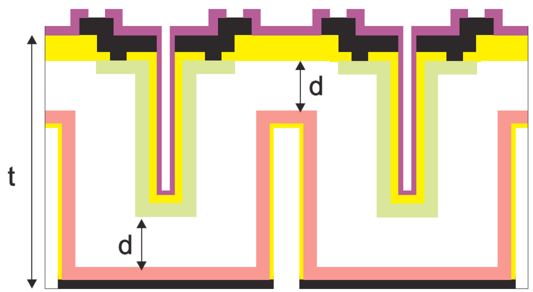
[A.Affolder 13th RD50 Workshop, Nov.2008]

3D detectors

- **3D detectors decouple thickness (signal) and depletion voltage**
  - **Depletion and charge collection is sideways**
- **Superior radiation hardness “by design”**
  - **less trapping (as collection distances are short)**
  - **Full depletion voltage less affected by growing acceptor concentration**
- **Original 3D designs conceived as pixel devices**
  - **can connect rows of columns to form strips**
- **Simplified 3D design**
  - **Single Type Columns (STC)**
  - **Double Sided Double Type Columns (DTTC)**

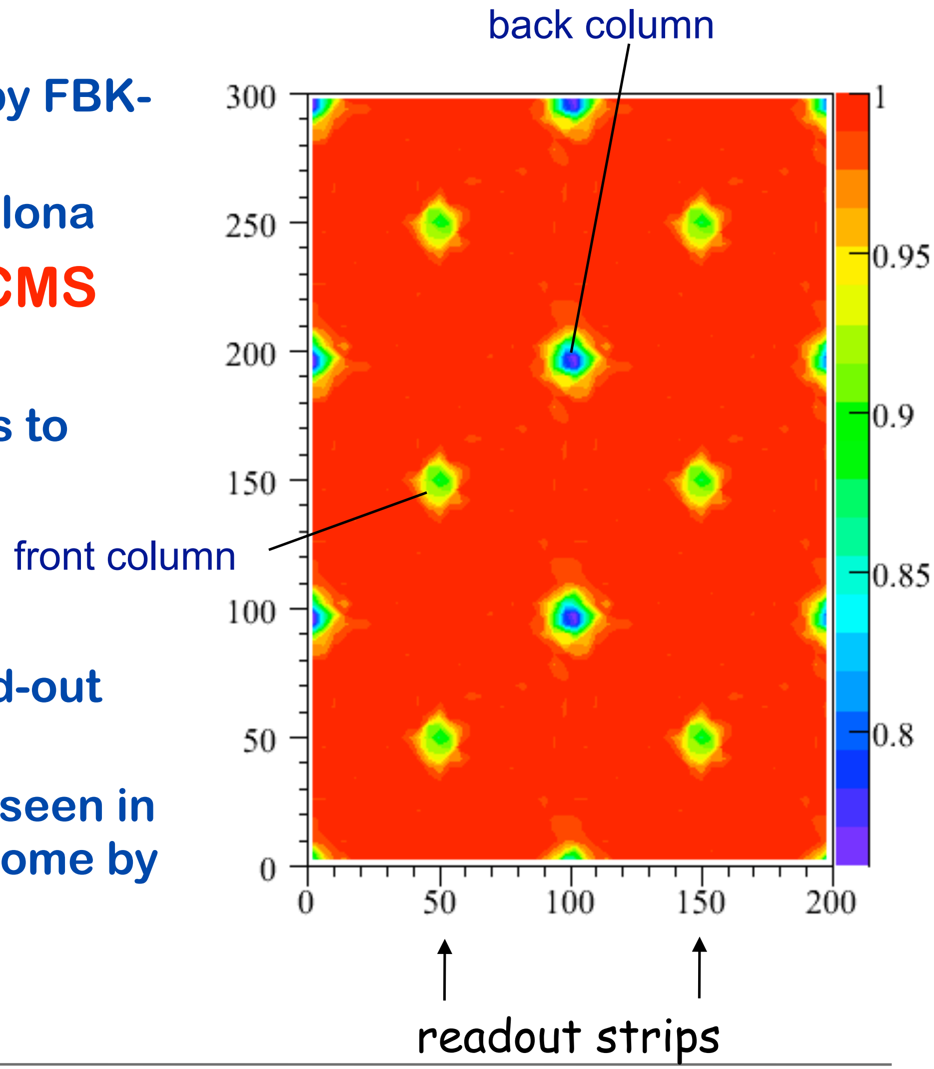






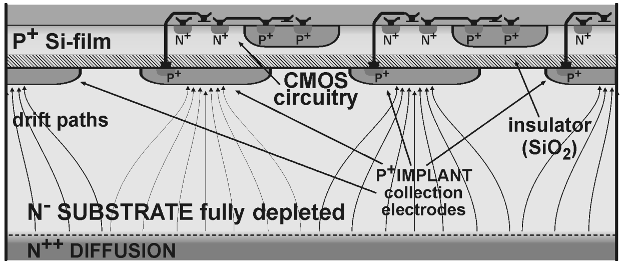
3D recent results

- **Sensor: 3D DTT**
  - p-in-n microstrip, 100 um pitch by FBK-irst, Trento
  - p-in-n microstrip by CNM, Barcelona
- **Readout: APV25, as used in CMS tracker**
  - Signal cut: SNR >5 (corresponds to ~6500 e-, 1 fC)
- **Efficiency low in columns**
  - Overall efficiency: 99 %
  - Uniform efficiency between read-out strips
  - Low field region between strips seen in 3D Single Type Column is overcome by 3D-DTC design



MAPS in SOI

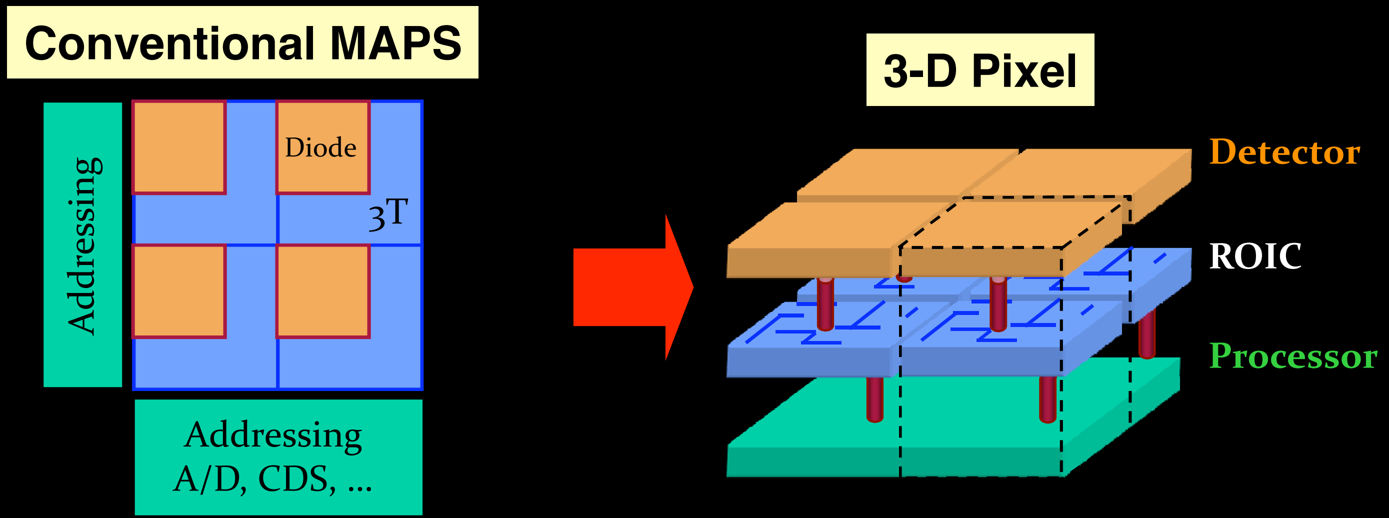
- Truly monolithic detector: High density, low material, thin device
- Standard CMOS can be used:
  - complex functions in a pixel
- No mechanical bonding
  - high yield, low cost



- However, the close proximity between sensors and Electronics (~200 nm) gives problems
  - electric field from sensor change electronics characteristics
  - crosstalk between sensor and electronics
  - electric field in oxide accelerates chance of holes traps at Si-SiO2 interface, thus reducing radiation tolerance
- KEK , Tsukuba Univ. , Osaka Univ, TohokuUniv. , Kyoto Univ. , AXA/ISAS , RIKEN LBNL, FNAL, OKI Semiconductor Co. Ltd. (effort started in 2005)

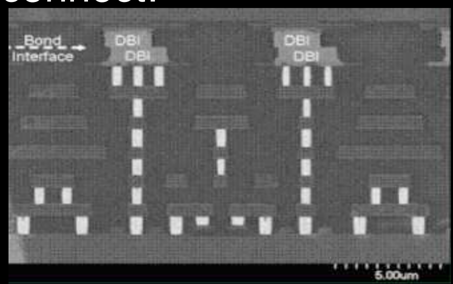
3DIT interconnections

- Vertical integration of thinned and bonded silicon tiers with vertical interconnects between the IC layers
- The 3D technology, driven by industry, can offer many benefits



- Via formation
- Wafer thinning
- Wafer bonding

Direct bond Interconnect:
3-micron and
1.5-micron pitch



(Ziptronix)

Yarema

Power

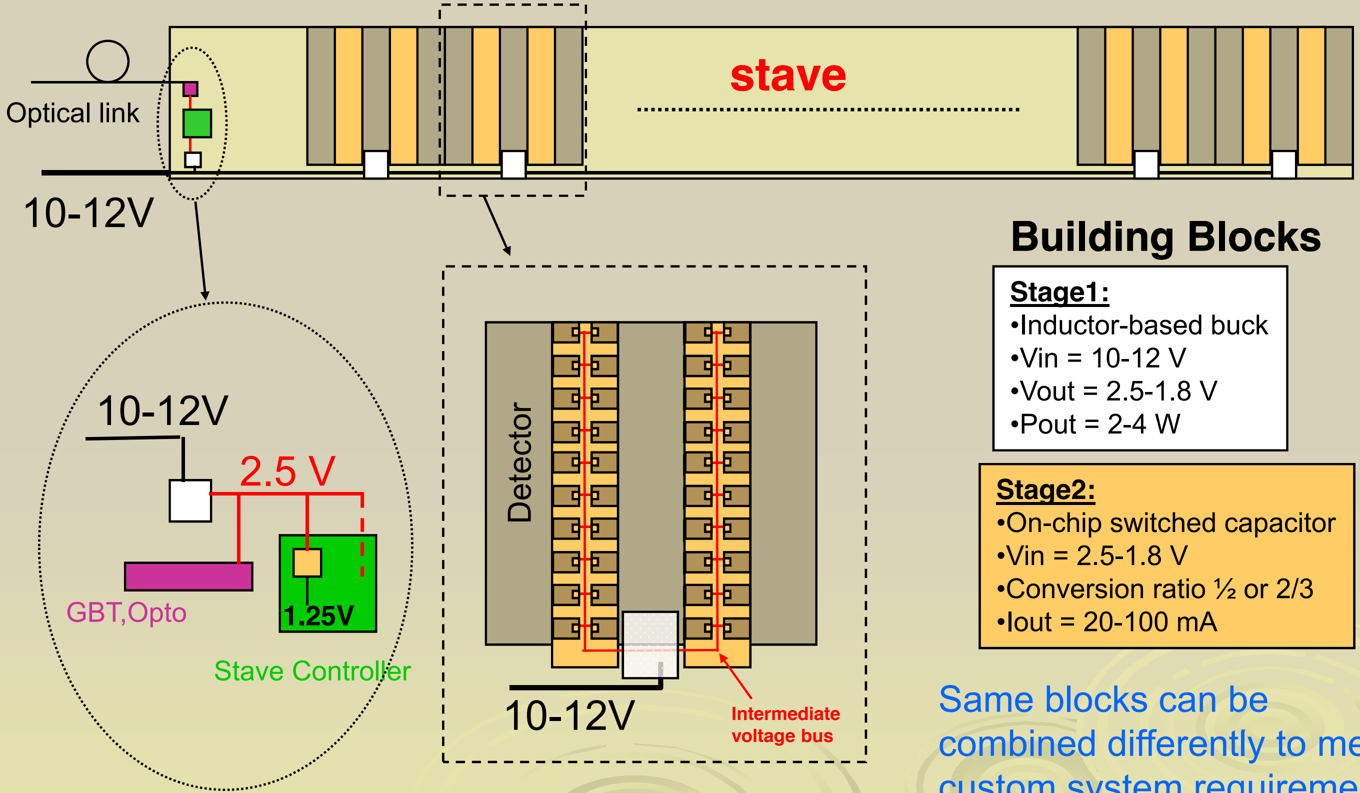
Power delivery

- **Example: In CMS there are ~ 2000 PS units that deliver ~ 70 kW ~ 15 kA (35 W/PSU)**
  - ~ 50% of it in the electronics and the rest in cables, out of which ~30% in cable dissipation inside the tracker cold volume (where electronics and detectors sit)
  - Even with advanced CMOS technologies, this is expected to increase and sensor leakage
  - Currents will also make significantly larger contributions to the total power budget at SLHC.
- **Power estimate for the Front End ~ 500 uW/channel in the strips and 120 uW for pixels**
  - Even with a total readout power of ~25-35kW larger currents will be required. Since this is impossible using existing cables, which cannot be supplemented, radical solutions are required.
  - Two alternative schemes under consideration
    - serial powering and on-detector DC-DC conversion, with custom circuits. Neither are proven or have been used in past systems and many problems remain to be solved; CMS favours DC-DC conversion based on its similarity to past designs and extensive experience with them which should offer lower risk.

DC-DC converter

Distribution based on 2 conversion stages

Example design shown for ATLAS short strip concept



Building Blocks

Stage1:
- Inductor-based buck
- Vin = 10-12 V
- Vout = 2.5-1.8 V
- Pout = 2-4 W

Stage2:
- On-chip switched capacitor
- Vin = 2.5-1.8 V
- Conversion ratio ½ or 2/3
- Iout = 20-100 mA

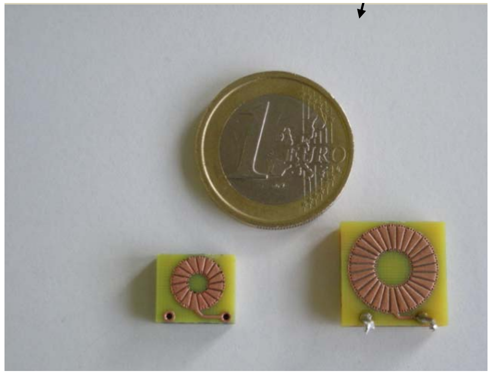
Same blocks can be combined differently to meet custom system requirements

Main Advantages

- **Standard grounding scheme**
  - Module ground potentials are all the same
  - Common ground reference for bias, analogue and digital voltage for whole substructure (rod, petal)
  - Bias voltage ground reference is the same for all modules
    - Note: in Serial Powering (SP) bias is referenced to “local ground“, which can differ by several tens of volts between first and last mo dule on a substructure.
- **Selective powering**
  - individual converter per modules/chips
    - With SP, the whole chain is powered on at once from a constant current so urce PS.
- **Flexibility to combine modules with different load**
  - different number of chips and/or standard modules vs trigger ones

Main disadvantages

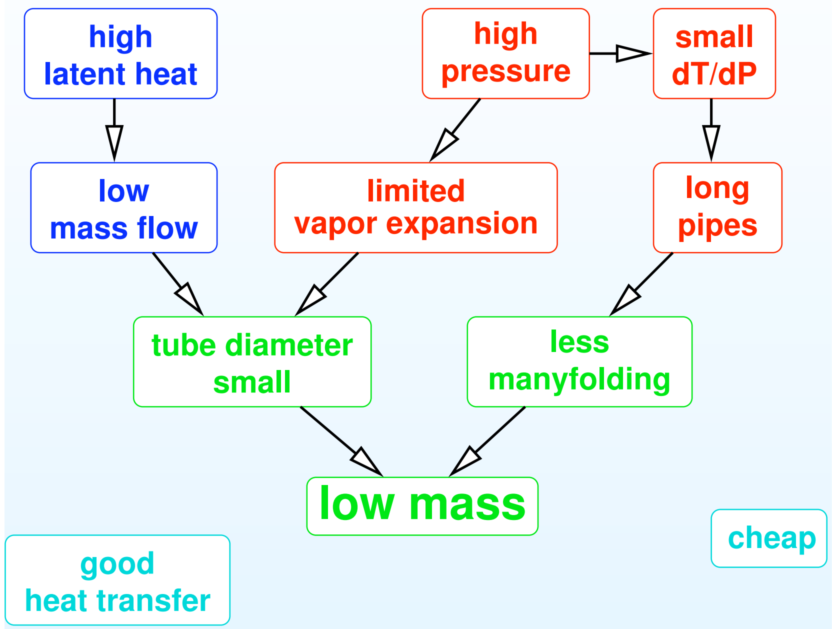
- Current in cables is larges in DC-DC vs Serial Powering
- Needs a large conversion efficiency (>~75%)
  - Local generation of heat
- Materials and spacing
- EM Noise
  - Conductive through cables
    - Can be reduced by proper layout.
  - Converters emit radiated noise.
    - Inductor should be shielded.
    - Coupling strongly decreases with distance.

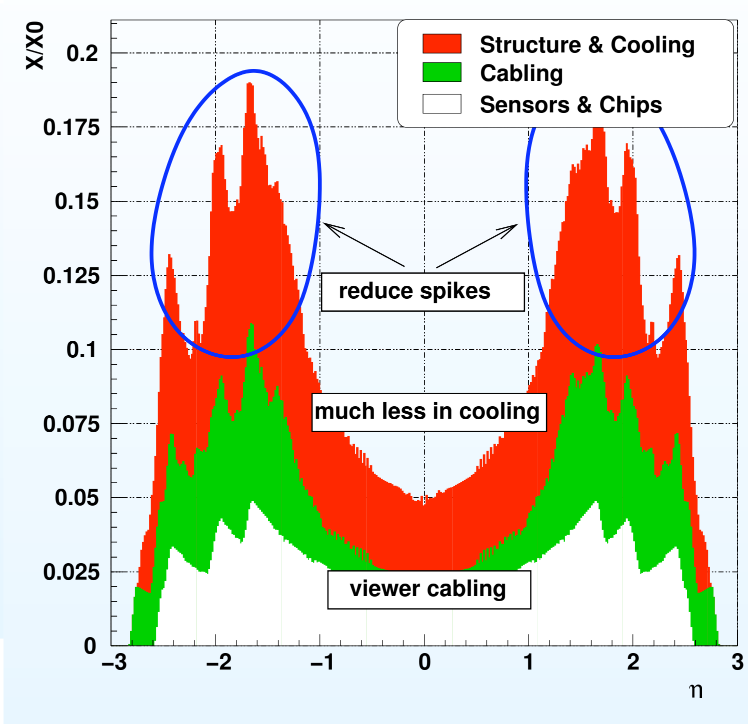


Cooling

CO_2 cooling

- **Evaporative cooling with CO_2 advantages**





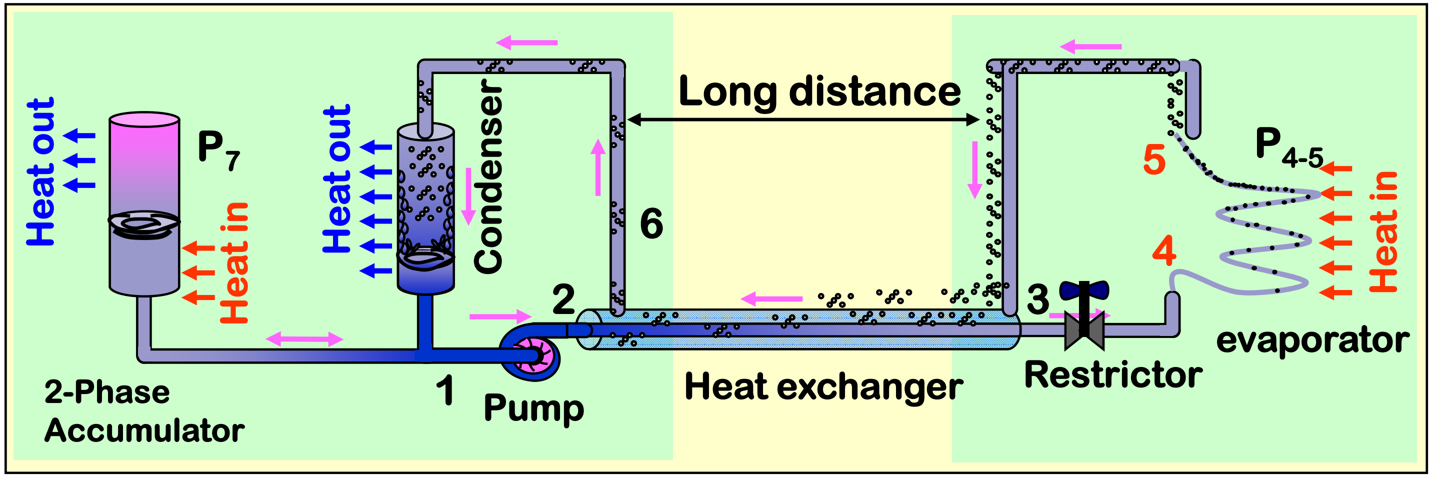
- **Drawbacks**
  - small pipes -> optimize cooling interfaces
  - high pressure need to reuse old low pressure pipes from current LHC services

Cooling – CO_2 vs C_3F_8

- *IBL cooling parameters:*
  - 15 staves with 112W each ← P_{total} =1.68kW
  - T_{sensor} -25°C, ΔT to coolant ≤10°C ← $T_{coolant}$ -35°C
- *Options (limited by main constraint: develop time & working experience):*
  - CO_2: copy of the LHCb VELO system, similar in cooling power.
  - FC: present C_3F_8 system (after modifications).
- *Consider the new ATLAS and CERN reorganisation of the Cooling group:*
  - ATLAS long term Upgrade and the improvement of present C3F8 system
  - Available Nikhef interest in contributing in the CO2 system ("cooling guru").

	C_3F_8	CO_2
$P_{evaporation}$	1.7 bar	17 bar
ΔT for ΔP=+-0.1bar	+1.4 C / -1.5C	+0.2 C / -0.2 C
ΔT for ΔP=+-1.0bar	+12 C / ~-20 C	+1.8 C / -1.9 C
ΔH for evaporation	100 J/g	280 J/g
Flow for 100 W	1.0 g/sec	0.4 g/sec
Volume flow	0.6 cm^3/sec	0.4 cm^3/sec

LHCb VELO Cooling System



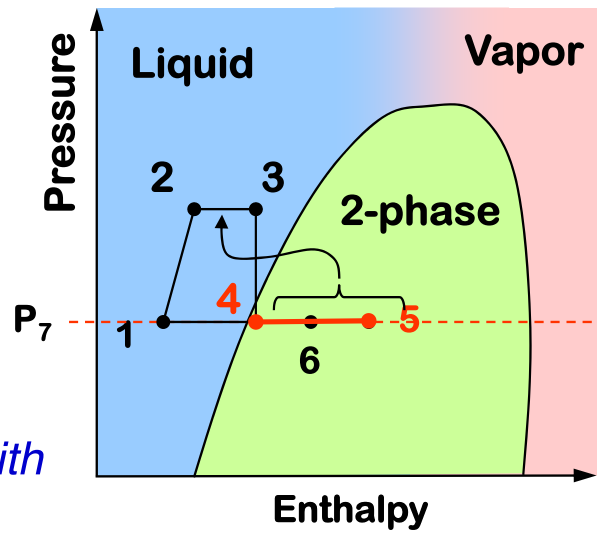
***2PACL** (2-Phase Accumulator Controlled Loop) principle of cooling:*

-*Liquid overflow => no mass flow control*

-*Low vapor quality => good heat transfer*

-*No local evaporator control, evaporator is passive in detector*

-*Very stable evaporator temperature control with 2-phase accumulator ($P_{4-5} = P_7$)*



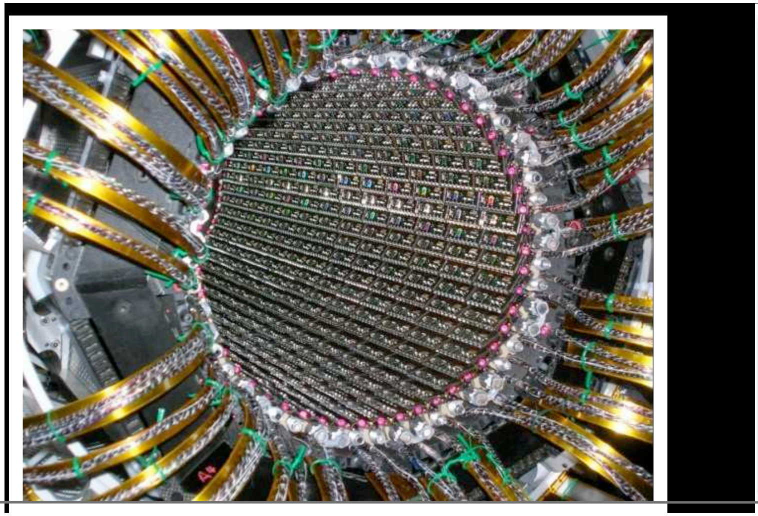
SLHC
Phase I

Pixel detectors replacement

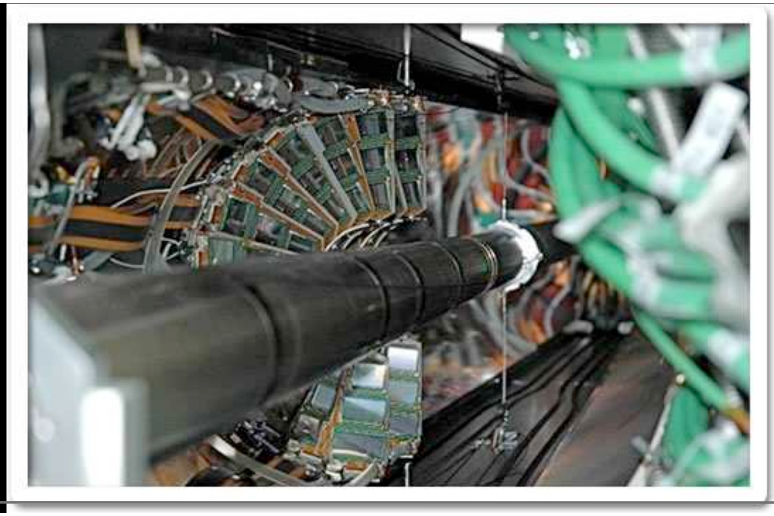
Phase 1: pixel replacements

- **Both ATLAS and CMS will replace (parts of) pixel systems in phase 1**
  - **cope against increased data rate (~2xLHC)**
  - **reduce the material budget**
- **ATLAS inner layer (Insertable B Layer) replacement**
- **CMS will replace the entire system and add one more layer**

ATLAS

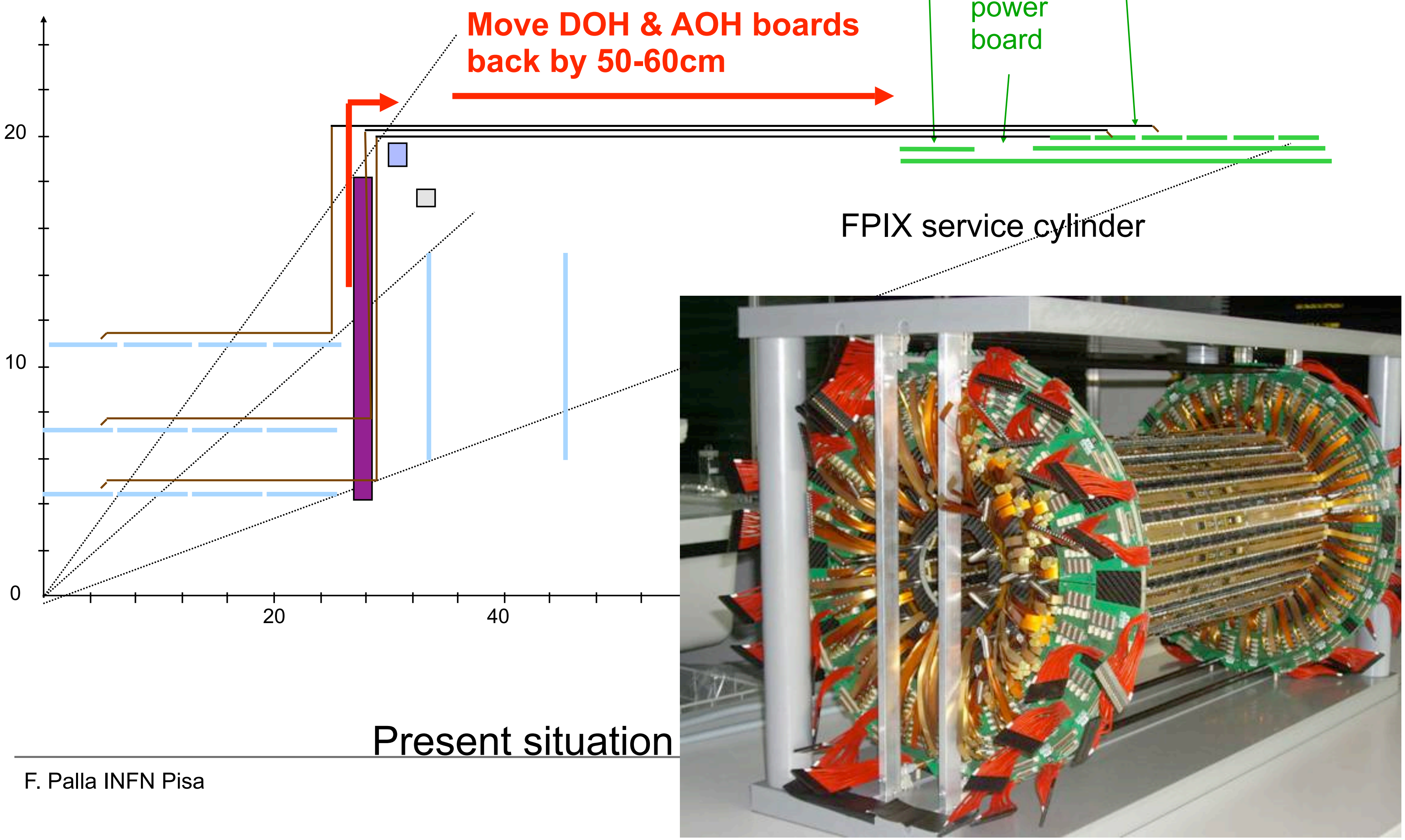


CMS



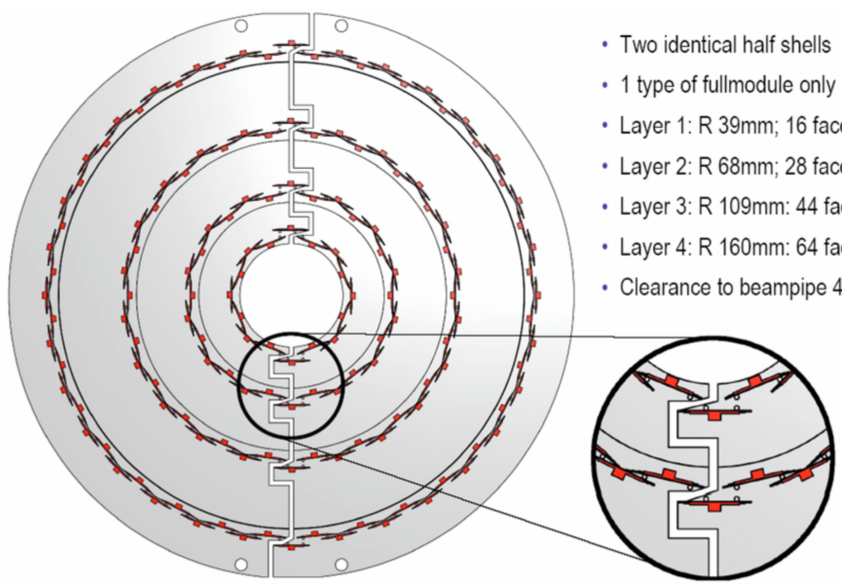
Shift PCB/Plug Material out of tracking Volume

- Modules with long pigtails (1.2m) CCA wires 16x(2x125μ)

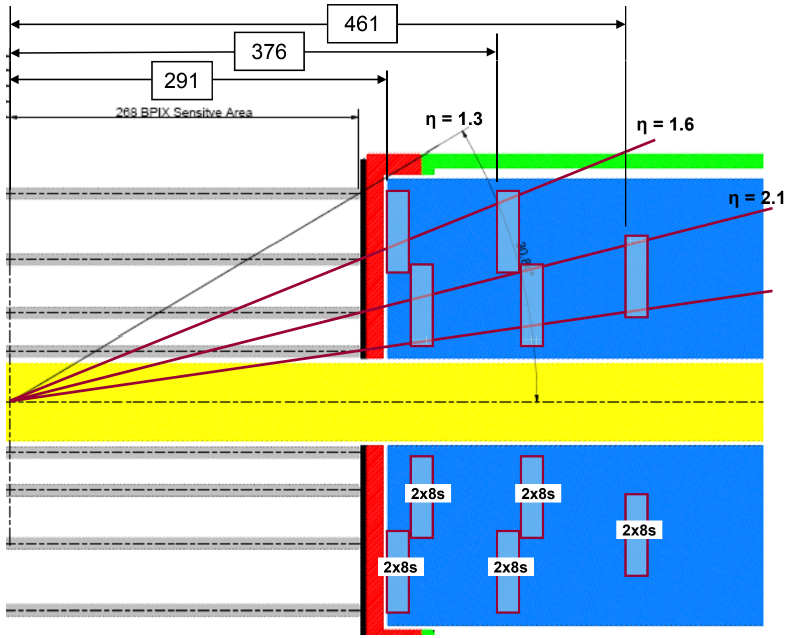


Present situation

CMS SLHC Phase 1 pixel



- Two identical half shells
- 1 type of fullmodule only
- Layer 1: R 39mm; 16 faces
- Layer 2: R 68mm; 28 faces
- Layer 3: R 109mm: 44 faces
- Layer 4: R 160mm: 64 faces
- Clearance to beampipe 4mm

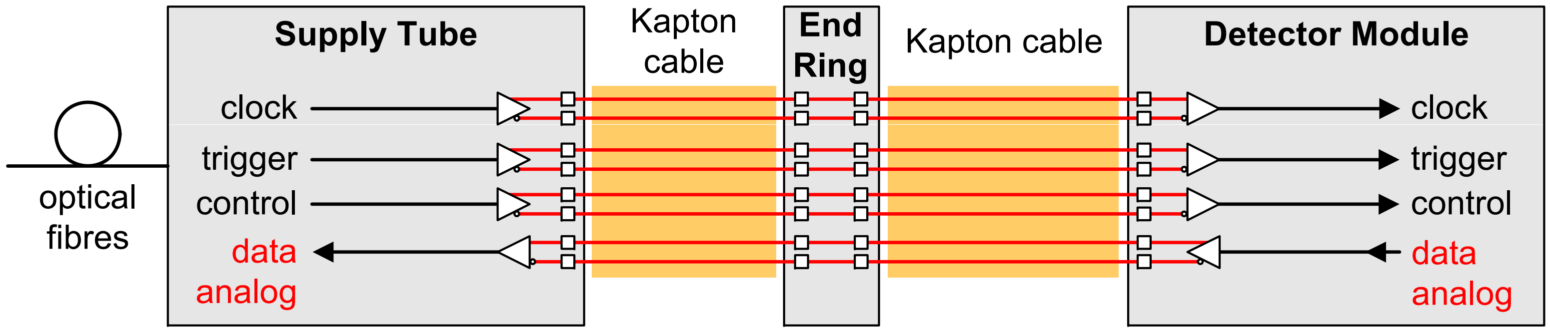


- 4 layer pixel system 4, 7, 11, 16 cm
- add one more forward disk in either sides
- Ultra light mechanics
- BPIX modules with high speed low mass and low power links
- Shift material towards high eta
- Modify PSI46 chip for 160 MHz digital readout & increase buffer length

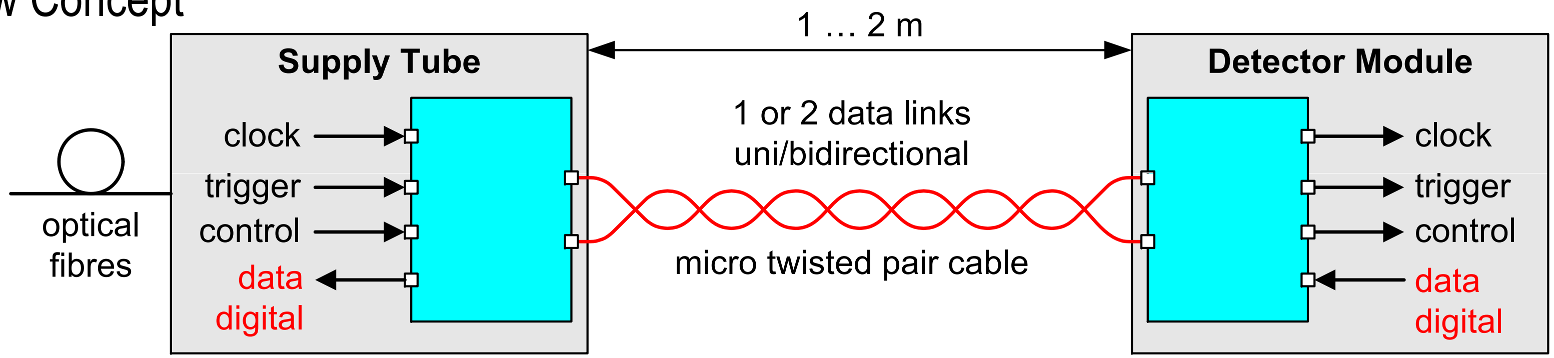
New copper links

Idea: reduce connectivity (no endring prints) and material

Existing System in CMS Pixel Detector

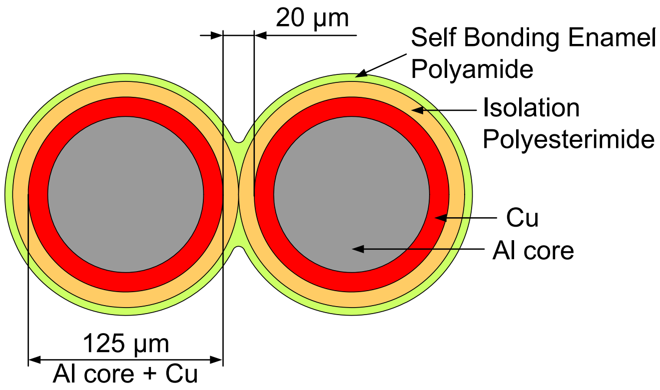


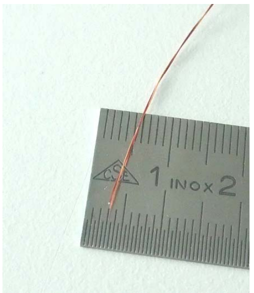
New Concept



Micro-twisted pairs

cross section





First Choice:

- twisted pair self bonding wire
- 125 m wire diameter (4um Cu)
- 10 mm per turn

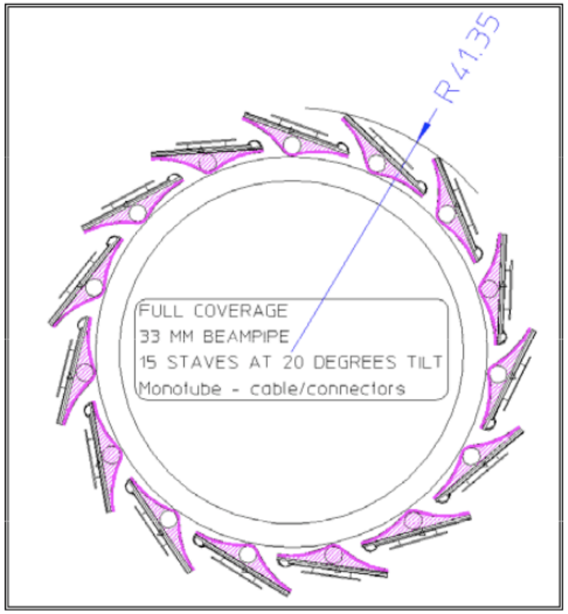
Electrical characteristics:

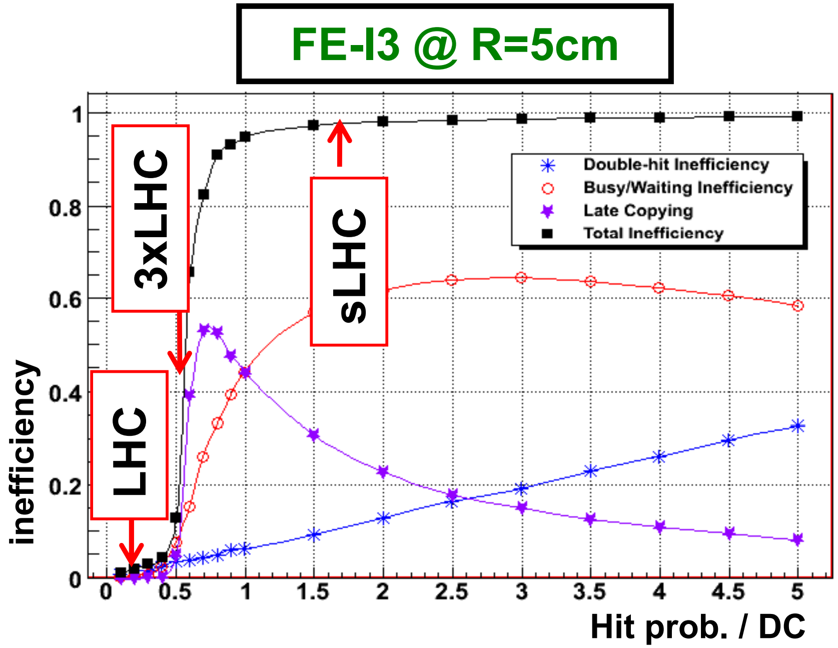
- Impedance: 50 Ohms (very low for differential line)
- Impedance change: 1.3 Ohms per 1 m distance variation
  (Calculation done with ATLC by Sandra Oliveros UPRM)
- v = 2/3 c_0 (5 ns/m)
- C = 100 pF/m, L=250 nH/m

Less than 10 pJ/bit over 2 meters (factor ~10 less than current electrical pixel links)
160 Mbps is ok
No crosstalk problems

ATLAS IBL

- Low radiation length (X0= 60% of B-Layer) and smaller detector radius improve current Pixel detector physics performance (even with inefficient B-Layer).
- Carbon-carbon foams with low density(~0.1 - 0.2g/cc)and reasonable thermal conductivity (K ~ 6-18 W/m•K).
- Head room in the cooling: low T, small fluid mass using CO2 cooling
- Electrical services low mass: Al (instead of Cu); high signal bandwidths.
- Larger active area in the modules (big FE chips).





SLHC
Phase II

- Using Phase I pixel system as starting point
- Provide trigger information
- Outer tracking with adequate performance

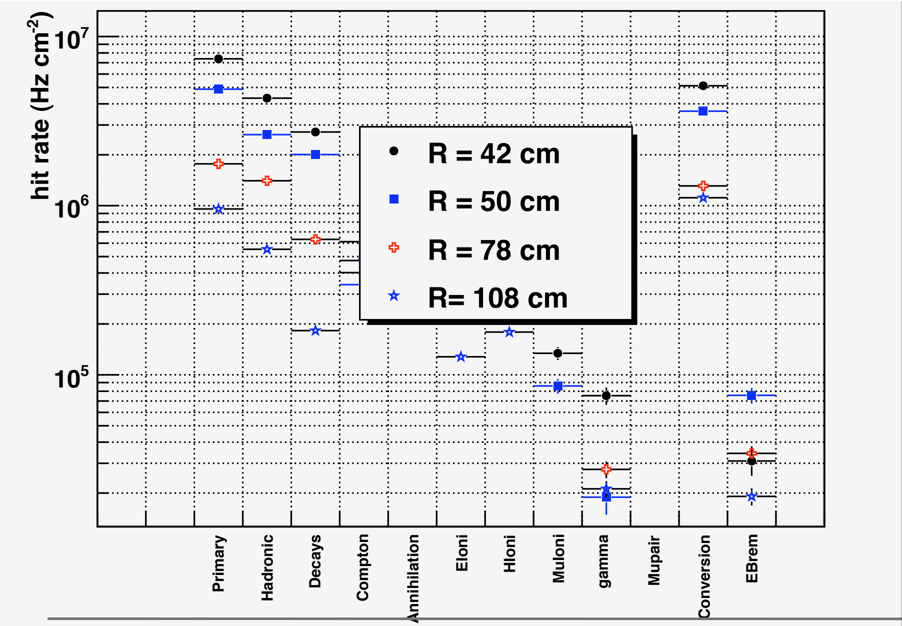
The track-trigger challenge

- **Impossible to transfer all data off-detector for decision logic so on-detector data reduction (or selective readout) essential**
  - The SLHC hit density and high combinatorial background will mean isolation cuts are less effective
  - Aim not to degrade tracking performance – but trigger layers will need extra power compared to normal layers
- **What are track-trigger requirements?   - still under study**
  - electron – Present HLT uses inner tracker point to validate projection from the calorimeter
  - muon - a tracker point in a limited $\eta - \phi$ window to resolve ambiguous muon candidates & improve p_T
  - jets – information on proximity/local density of high p_T hits ?
  - separation of primary vertices (ie: 300-400 in ~25cm)

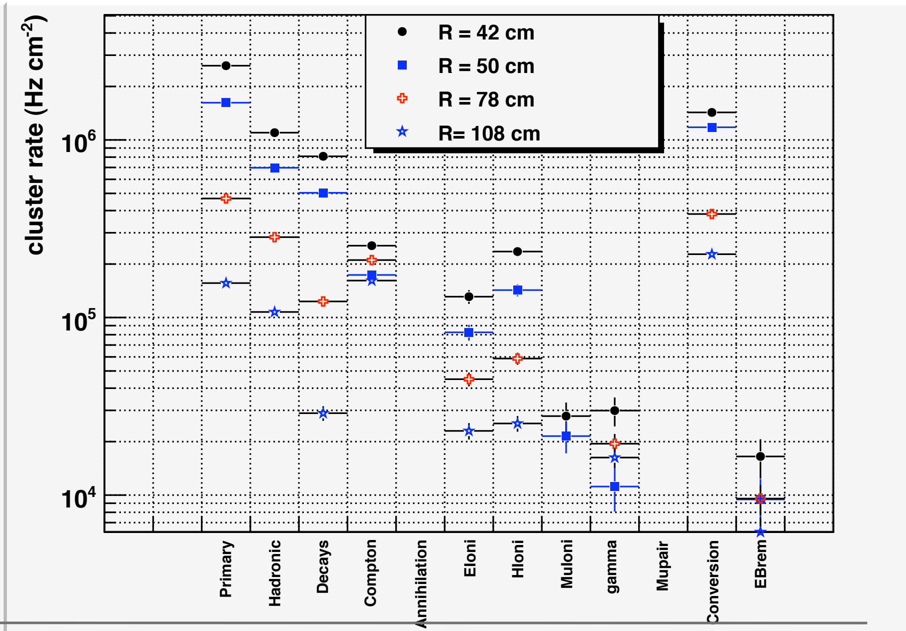
Data rate in Barrel

- **Huge data rate (at 10^{35} cm^{-2} s^{-1})**
  - **Use clusters instead of hits to first decrease the rate**
    - **R=42 cm: clusters (hits) ~7 (22) MHz cm^{-2}**
    - **R=78 cm: clusters (hits) ~1.6 (6) MHz cm^{-2}**
    - **R=108 cm: clusters (hits) ~0.7 (3.6) MHz cm^{-2}**

HITS

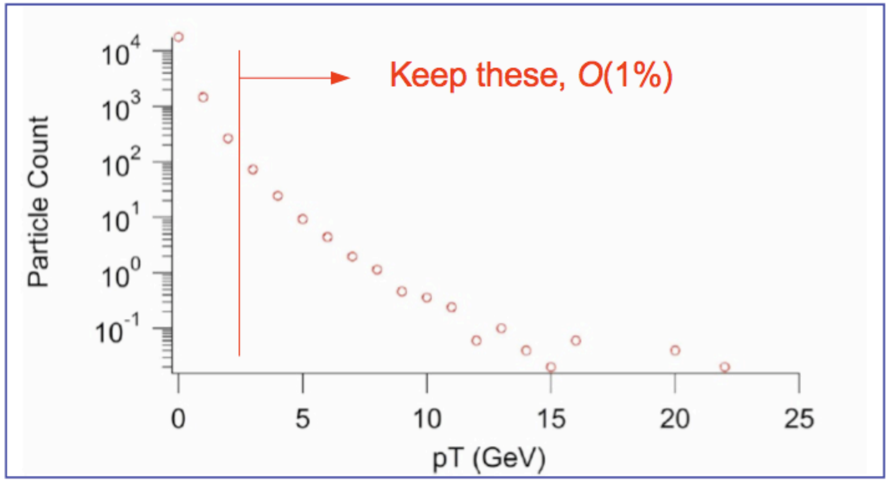


CLUSTERS



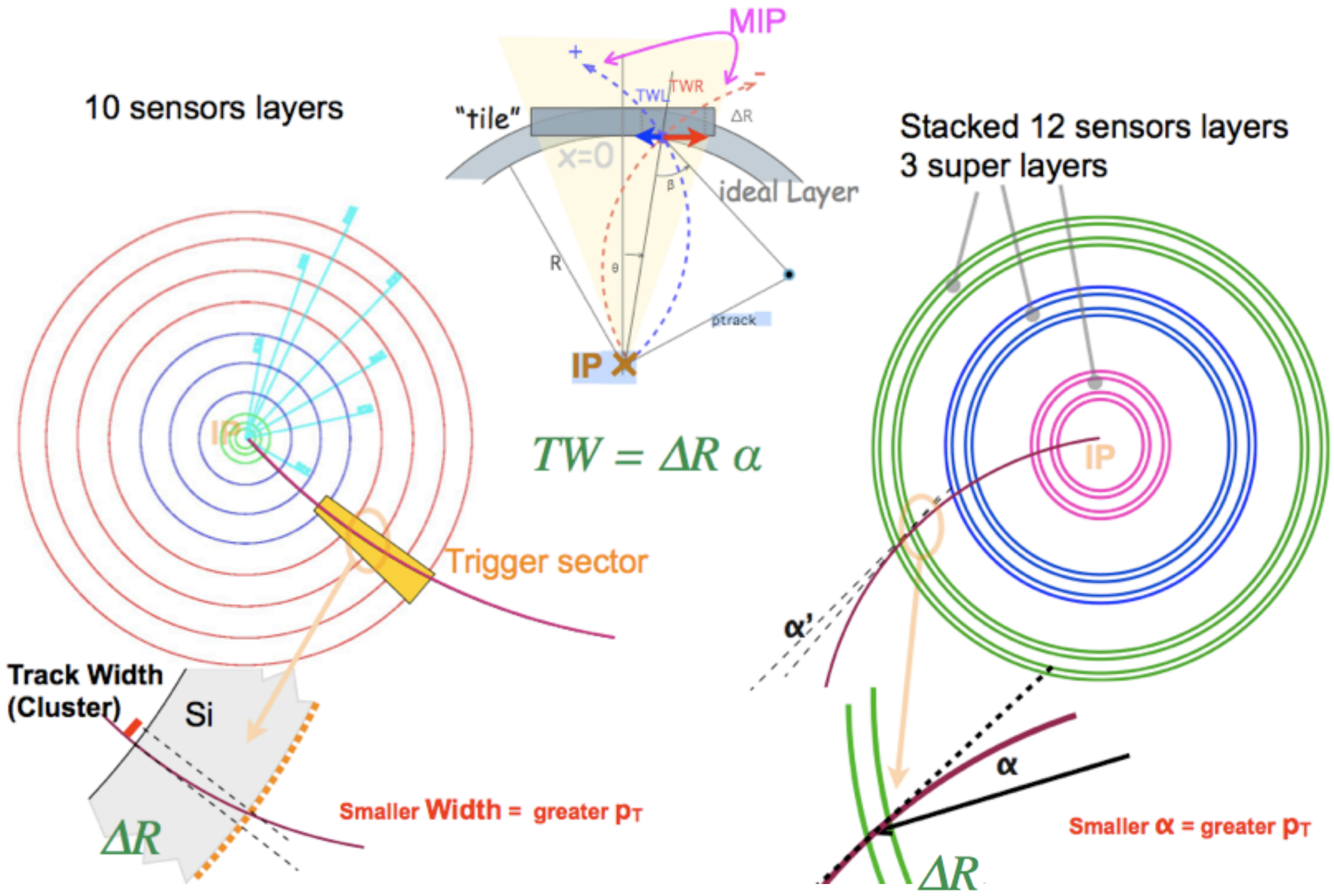
Tracking Trigger driving idea

- **Select only tracks above a given p_T since they are very few**



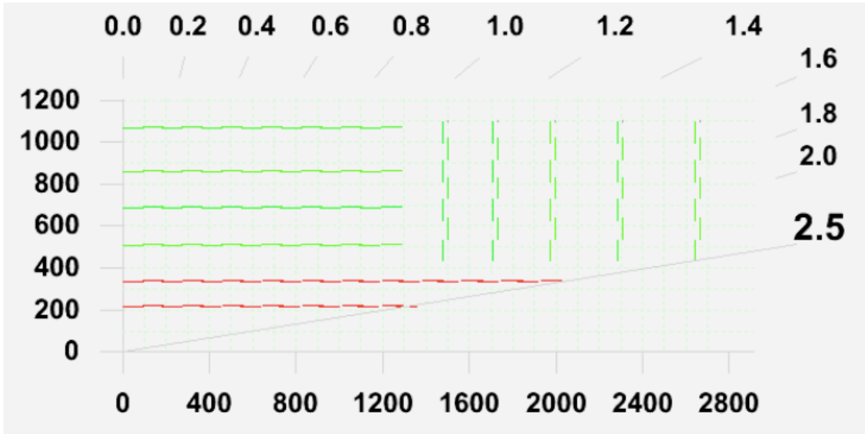
- **send reduced data volume from detector for further logic**
  - **eg factor 20 with p_T > few GeV/c**

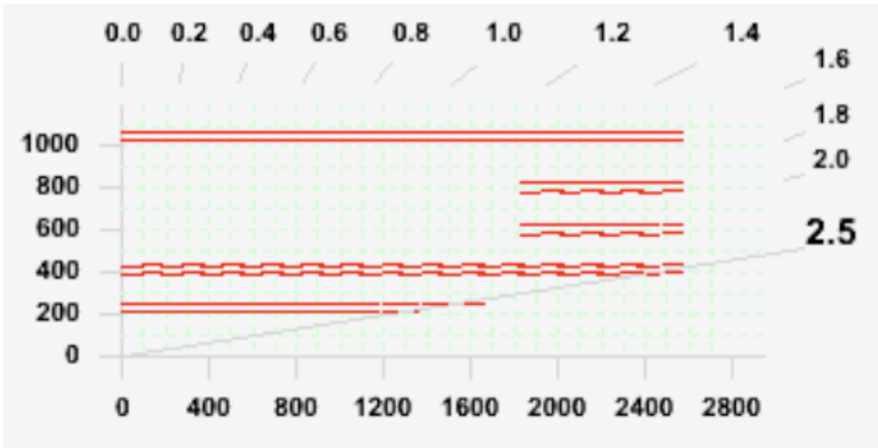
Layouts under study



Major variants being examined

- **Two PT layers**
  - cover full η range
  - R 25 – 35 cm
- **plus Outer tracker**
  - endcaps or long barrels?
  - short sensors ~ few cm
- **"All trigger" 3D**
  - long barrel layers constructed as doublets
  - pixels ~1mm x 100µm
- **Evaluate performance**
  - Tracking & trigger
  - material, power, cost, time…





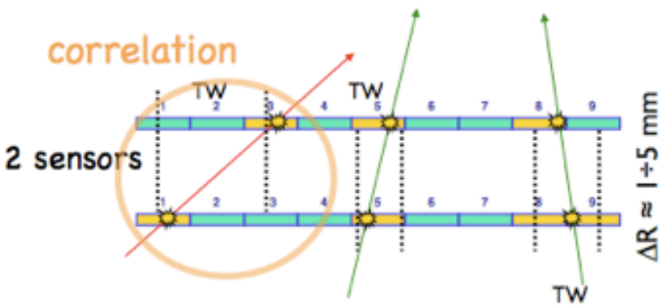
http://abbaneo.web.cern.ch/abbaneo/tkgeometry/summaries/

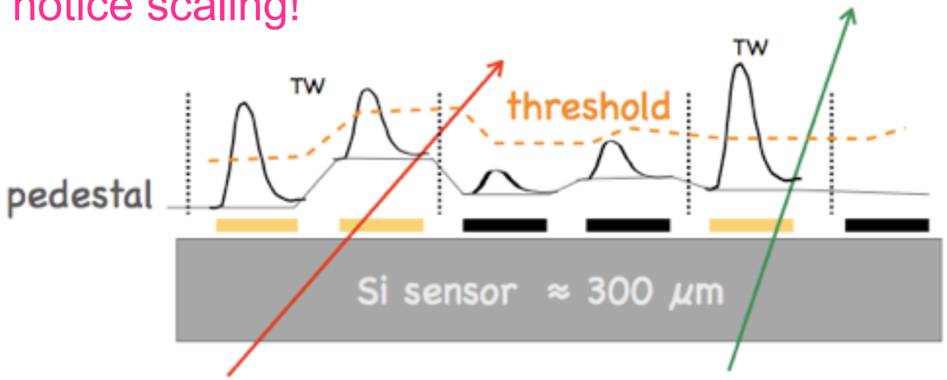
Track width measurements

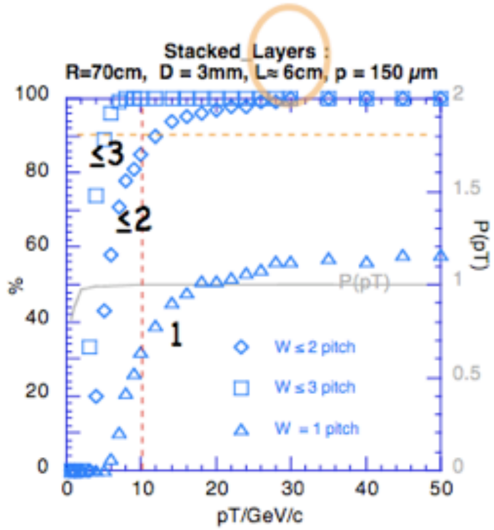
Stacked Layers

Very similar
notice scaling!

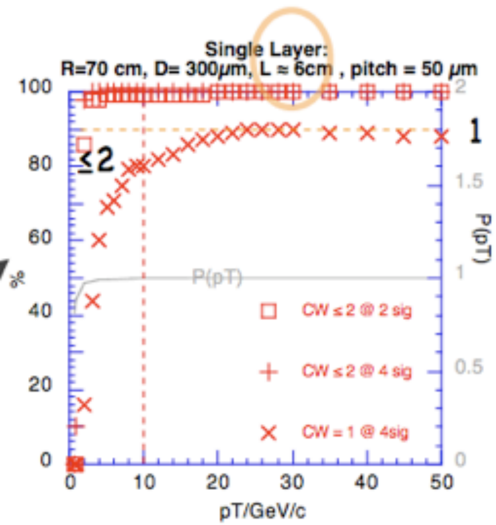
Single Layer



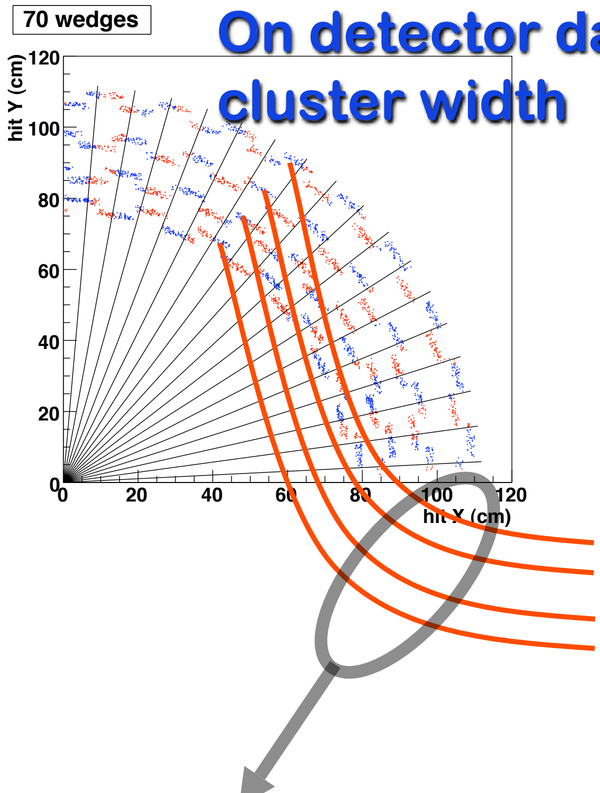




measurements give pT lower limits

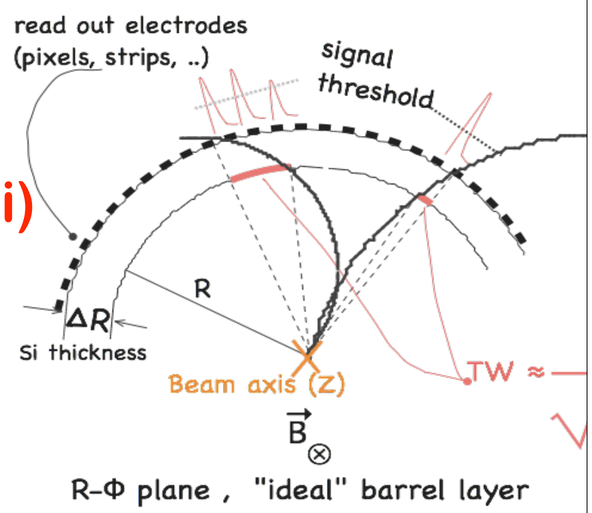


Multilayers approach



On detector data reduction using cluster width

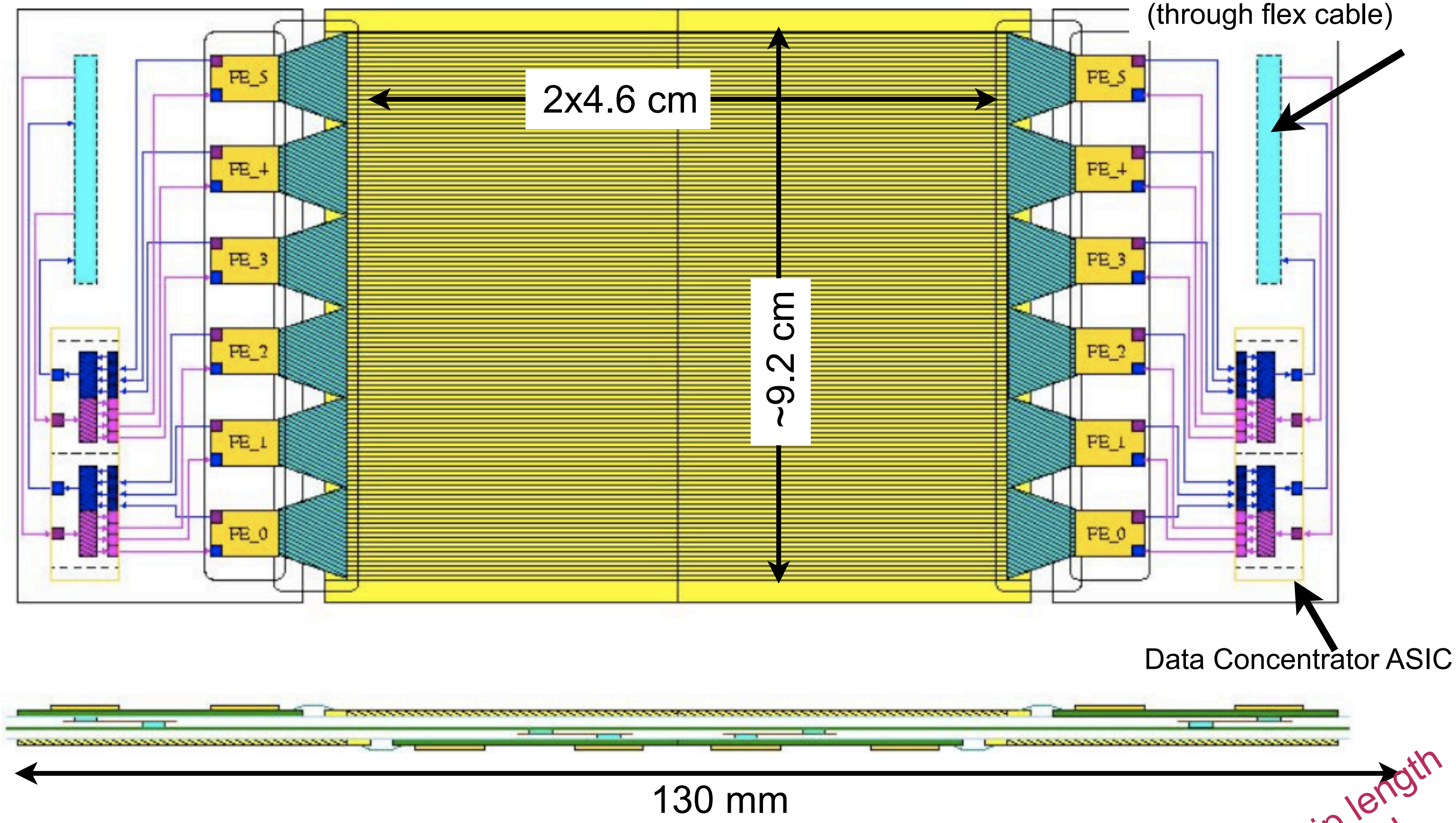
(F. Palla, G. Parrini)



Off detector, FPGA working in a small Δφ produce a set of tracks above a given p_T

Fast (~10 Gbps) data links

A possible module layout (outer layers)

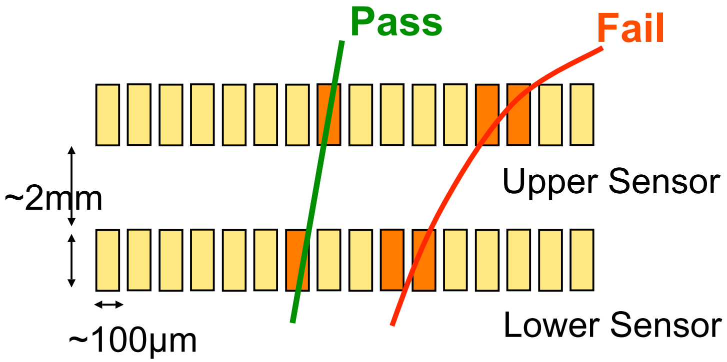


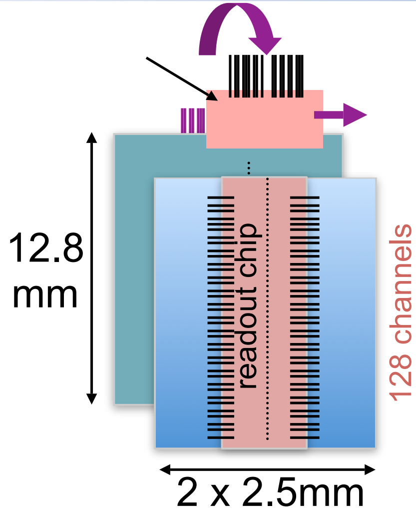
120 µm pitch
128 strips/FE
300 µm thick

Pitch and strip length not yet optimized

Stacked layer approach

- Compare pattern of hits in contiguous sensor elements in closely spaced layers
  - p_T cut set by angle of track in layer

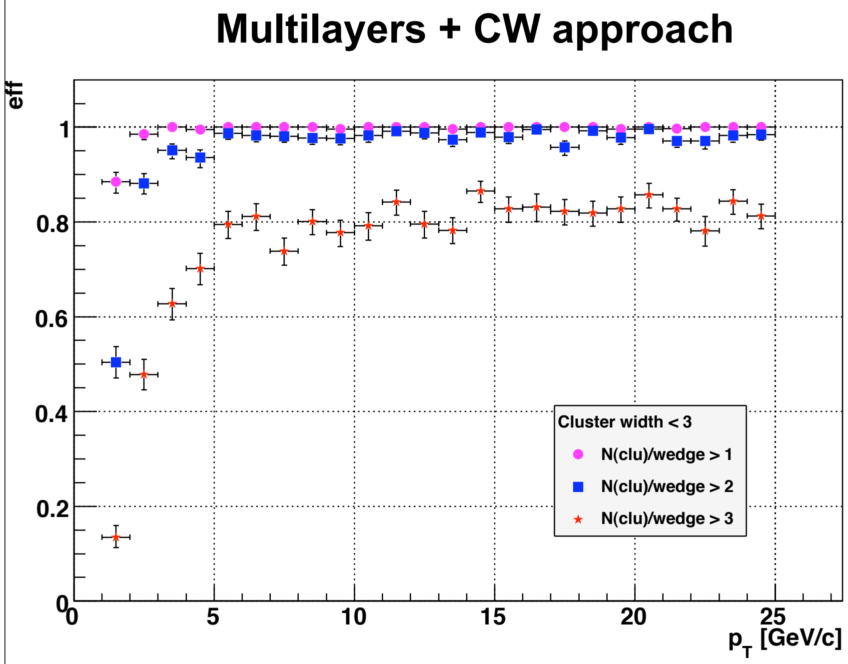


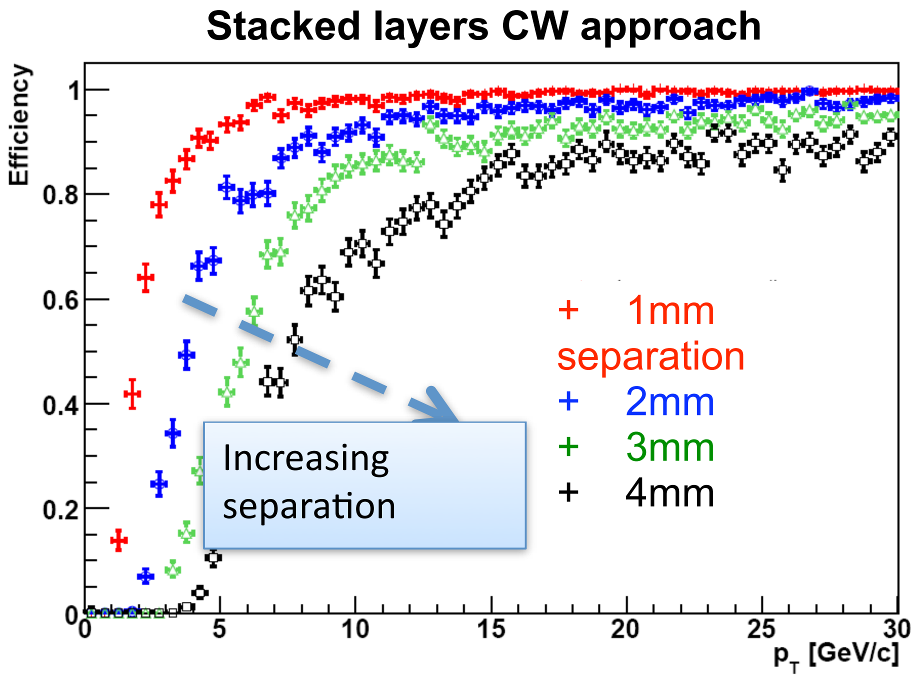


- (G Hall, M Pesaresi, M Raymond)

Track efficiency and fake rate

- **Similar behaviour for efficiency**

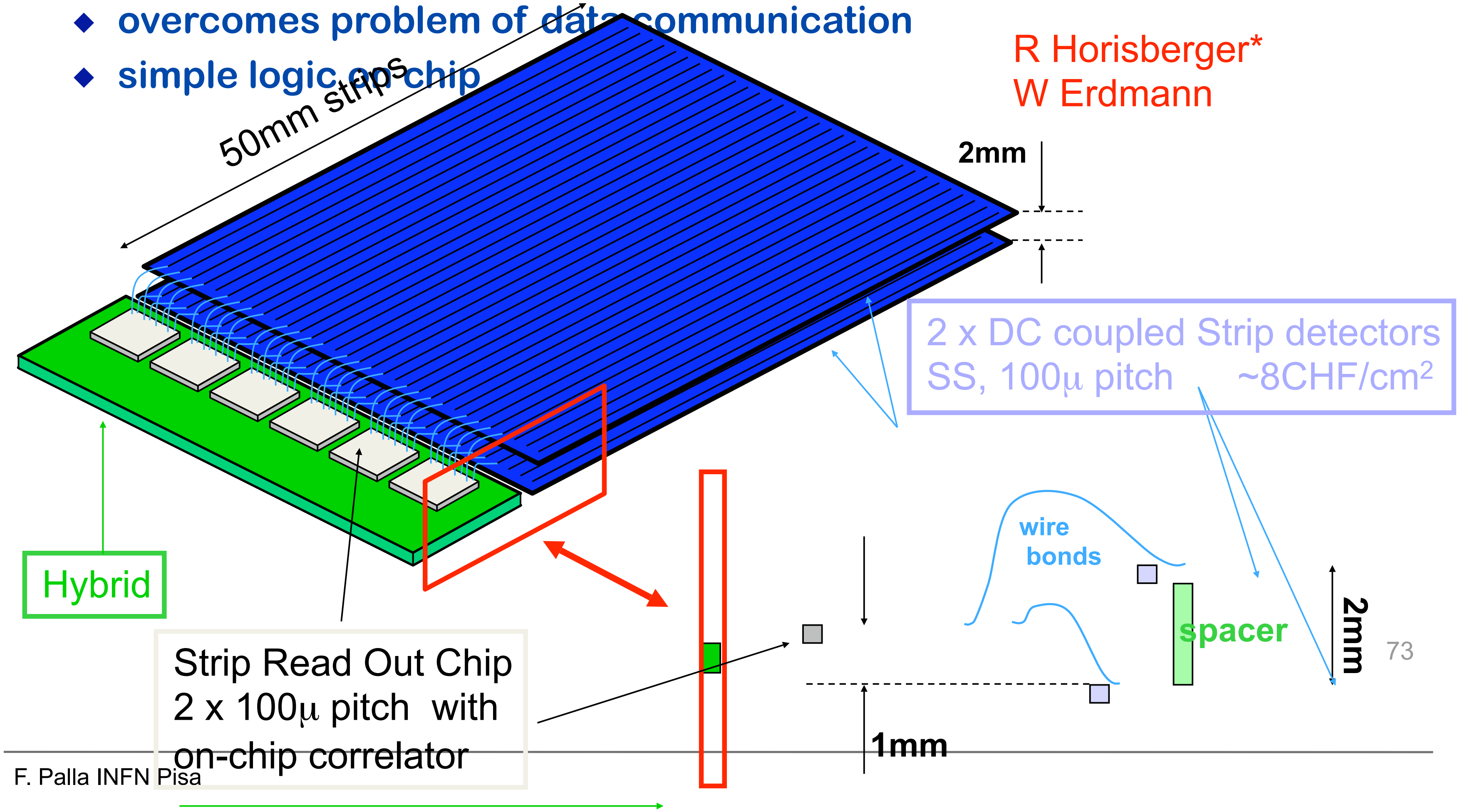




Possible PT module for outer Tracker

- **Bond sensor channels from upper/lower to RO ASIC – low cost**
  - overcomes problem of data communication
  - simple logic on chip

R Horisberger*
W Erdmann

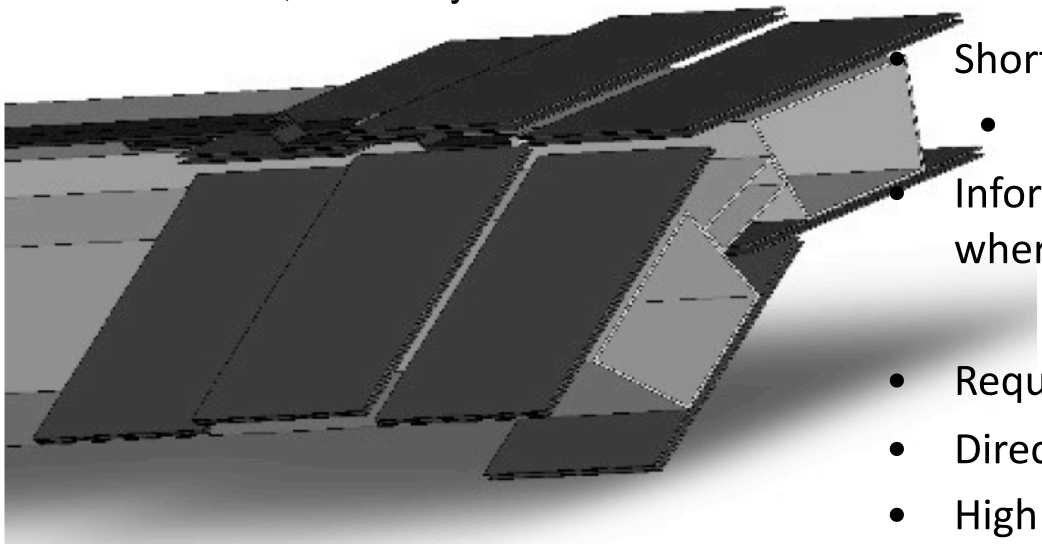


Other approaches to stacked layers

M. Mannelli, R Lipton et al

A. Marchioro, W Snoeys

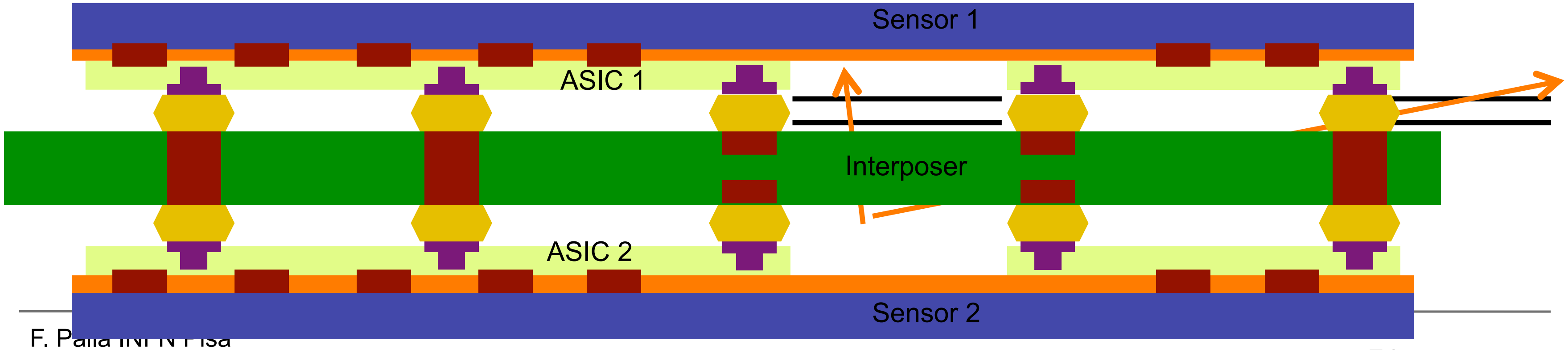
Monolithic technology or 3D electronic integration



- Short Data Path through Interposer:
  - Power advantage
- Information available regionally, close to where needed

3D Challenges:

- Requires Chip Through-Silicon-Vias (3D)
- Direct Oxide Bonding to Large Area device
- High rate data transmission without disturbing analogue performance

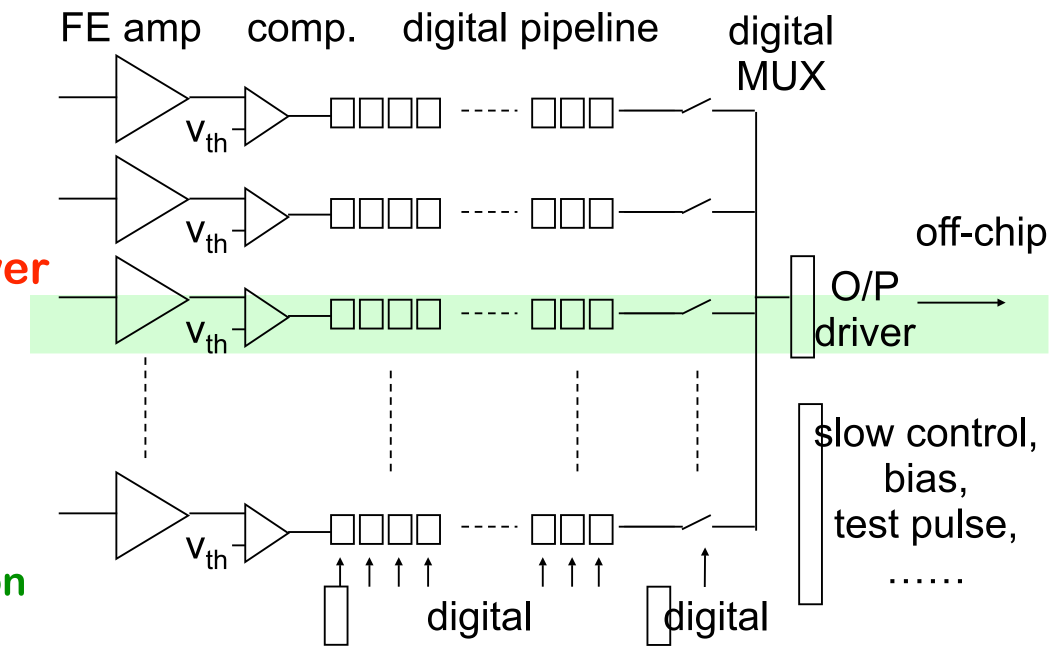


Outer readout

- **Present architecture**
  - analogue, unsparsified, analogue optical links, synchronous
  - external digitisation, cluster finding, zero suppression
  - 0.25μm CMOS, FP edge-emitting lasers, single-mode fibres
- **Pros**
  - works extremely well and easy to use with excellent diagnostic capability and noise robustness
  - occupancy insensitive – few power fluctuations
  - synchronous system easy to model and understand
  - cost effective, despite customisation
- **Possible cons for future**
  - must use fast digital optolinks – analogue no longer an option
  - if analogue information to be preserved, on-detector ADC

Binary – unsparsified - readout architecture

- **Fast front end in 130nm**
  - **comparator**
  - **binary pipeline**
  - **no ADC**
  - **Very simple & lowest power**
- **Features retained**
  - **simple synchronous**
    - **no timestamps**
  - **constant data volume**
    - **no trigger to trigger variation**

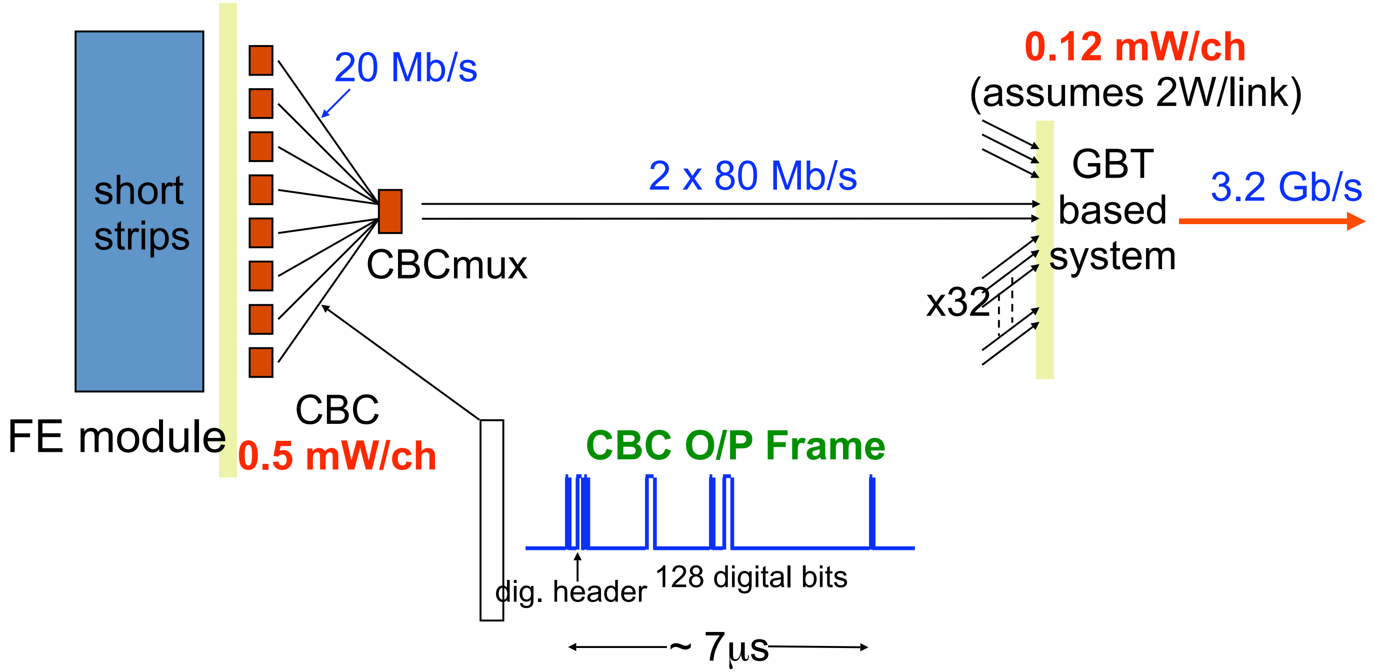


- Challenges
  - threshold management for large number of channels
  - fewer diagnostics
  - common mode immunity
  - binary position resolution

CBC = CMS Binary Chip

Target 0.5mW/channel

Overall system design

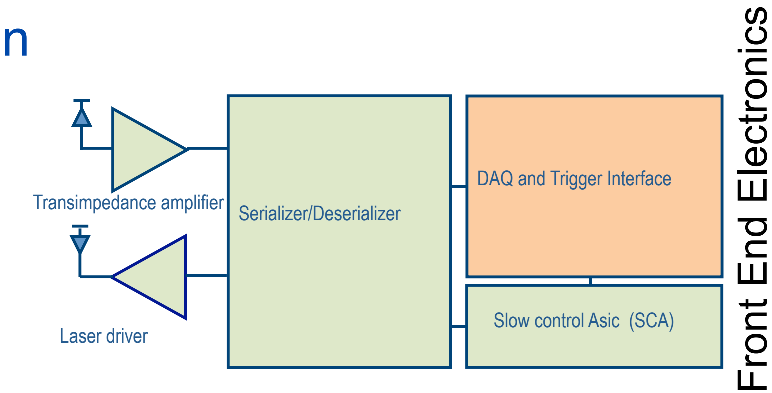


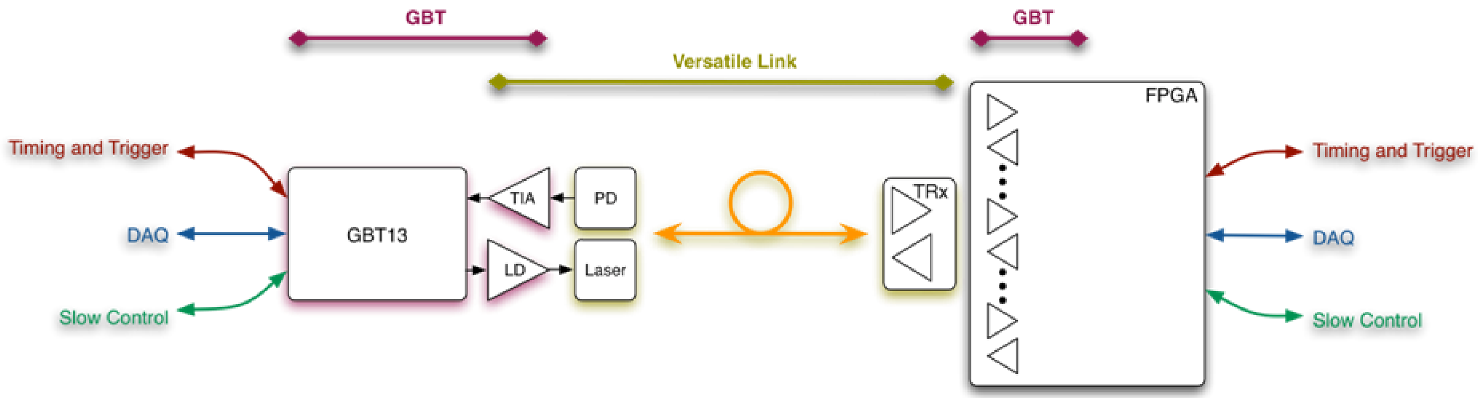
- **Provisional plans (M Raymond)**
  - **Output frame similar to APV, but binary**
  - **CBC output at 20Mbps in 7μs data frame**
  - **multiplex at 80 Mbps onto one low power electrical line to GBT**
  - **combine multiple 80Mbps lanes into 3.2Gbps link**

Fast links

GBT and fast links

- CERN is proposing a demonstrator for having a unique communication link designed in 0.13 μm CMOS technology
  - Bidirectional data transmission
  - Bandwidth
    - User 3.36 Gbps
    - Line 4.8 Gbps
  - Prototype ready by ~2011





On-Detector
Custom Electronics & Packaging
Radiation Hard

Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

Fast Links - I

Versatile Link project: target ~5 Gbps maybe too slow

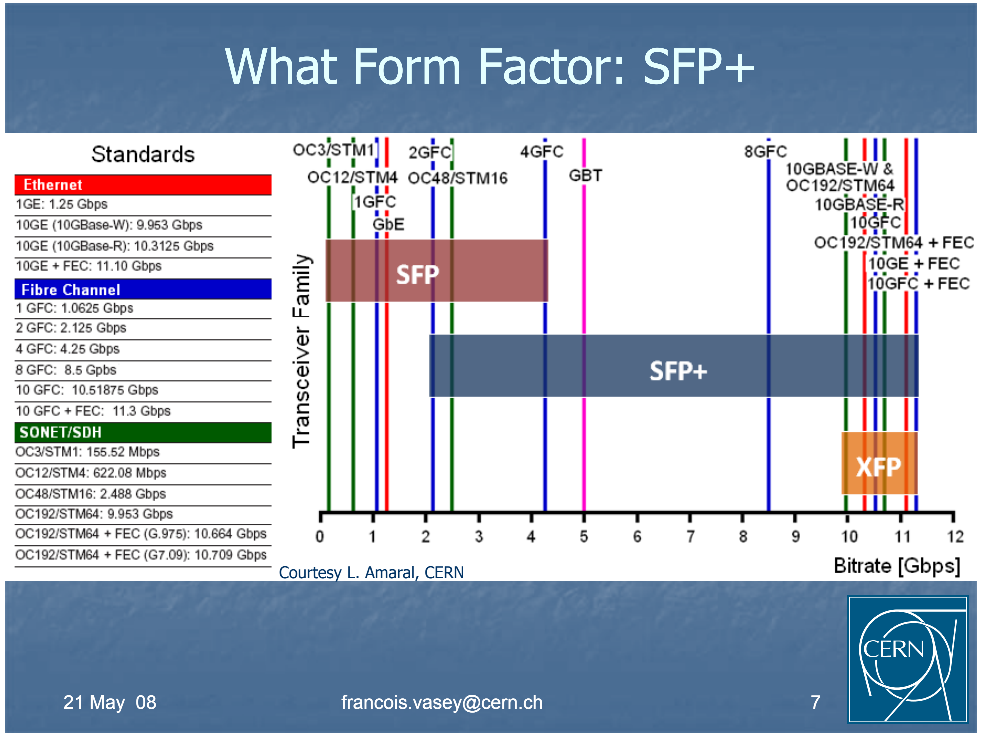
Conclusions

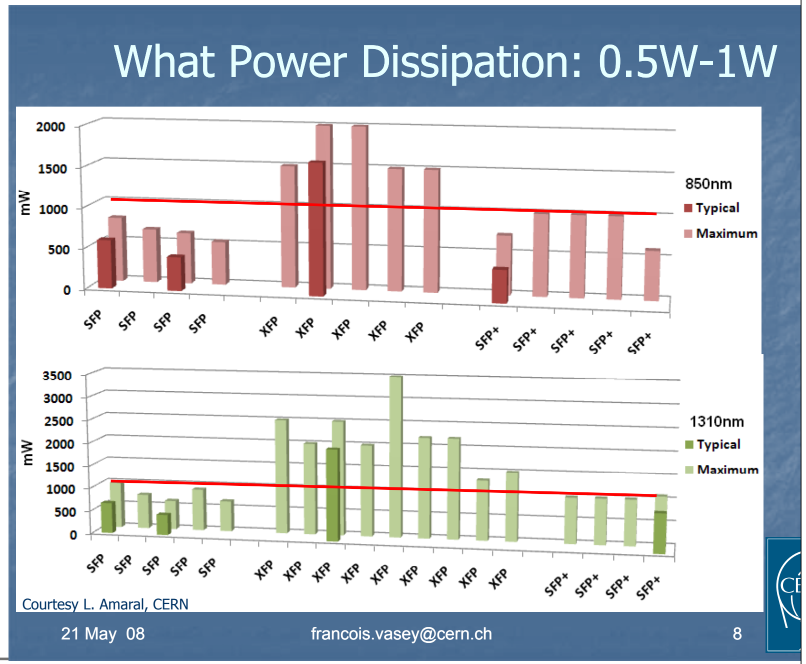
- Versatile link project is active
  - Currently ramping up to speed and getting equipped
    - SMU preparing FPGA test platform for P2P system
    - Oxford preparing γ irradiation test for SM and MM fiber
    - CERN concentrating on PIN-Rx
- Still looking for partners
    - PON-based system
    - Back-end components
- Trying hard to maintain compatibility with CMS-Tk fibre base
    - SM, 1310nm selected for analog transmission
    - Do not exclude MM 850nm, watch market evolution
- Bit-rate dependent on ASICs
  - GBT @ 4.8Gbps
    - Poor choice in terms of standard, cost and power dissipation
    - Good choice to start learning and progressively upgrade to 5-10Gbps
  - Practicing and testing with up to 10Gbps parts

21 May 08 francois.vasey@cern.ch 13

Fast links - issues

- Power consumption: O(1-2 Watt/link)

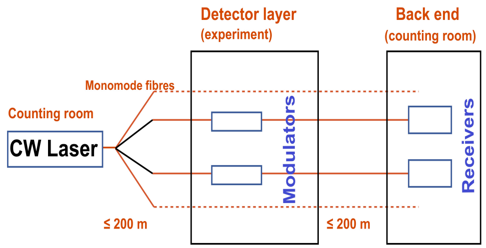


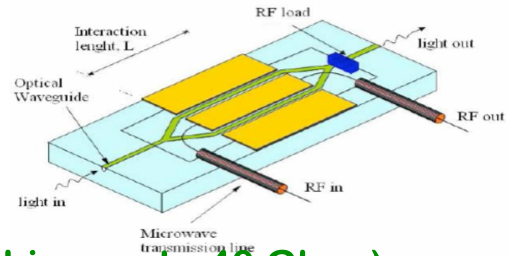


Fast Links - II

Telecommunication/IT standards

Put Laser power outside the detector and use modulators





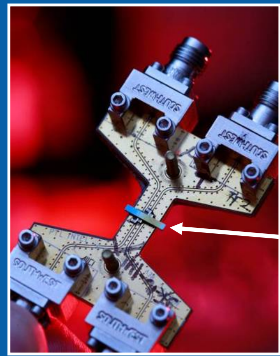
- **Normally uses electro-optical modulators (reaching up to 40 Gbps)**
- **Need to be tested in high B field, low temperature and high fluence**

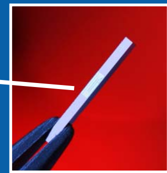
Modulator	Vpi @ 10Gb/s	Dyn. Extinction Ratio (dB)	Modulation Power	Power dissipated: driver (Typ)	Packaged Dimensions (Typ)	Laser Source	Notes
LiNbO3 (Avanex Small Form Factor)[2]	5 V	13	250 mW	1-1.5 W[8,9]	81 mm x 9.3 mm x 5 mm	External	Vpi L =9V
LiNbO3 (Avanex Low Voltage)[3]	4 V	14	200 mW	~1 W[8,9]	98 mm x 9.3 mm x 5 mm	External	
LiNbO3 ridge[4]	3 V	> 10	200 mW	0.5-1 W[10]	standard	External	Vpi L =7V (only R&D)
EAM (Bookham)[5]	2.7 V	11	200 mW	0.5-1 W[10]	60 mm x 13 mm x 5 mm	Internal (0.6 W cons.)	Rad Hard? High insertion loss (~7 dB)
EAM (OKI)[6]	2.5 V	9.5	200-300 mW	0.5-1 W[10]	25 mm x 13 mm x 6 mm	Internal (0.4 W cons.)	Rad Hard?
VCSEL (BeamExpress)[7]	2.5 V	>10	~30 mW	~200 mW	not std TBD	Direct modulation	Rad Hard?[11,12] Low temp?

Silicon based modulators

- Extremely attractive
  - reduced power consumption and dimensio[ns]
  - possibility to embed in the readout chip
  - expect available in >~5 years

40Gb/s Silicon Laser Modulator





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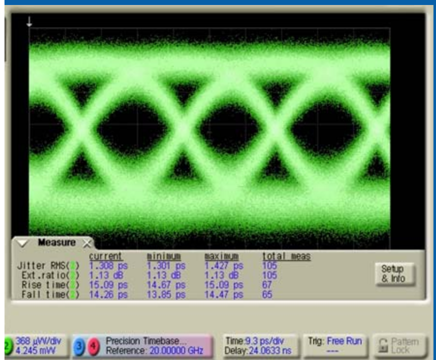
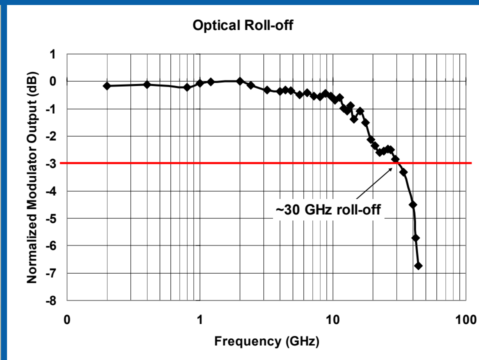
40Gb/s Data Transmission

Results presented at IPNRA





40Gb/s Data Transmission

Optical 3 dB roll off ~30 GHz

Worlds Fastest Silicon Laser Modulator

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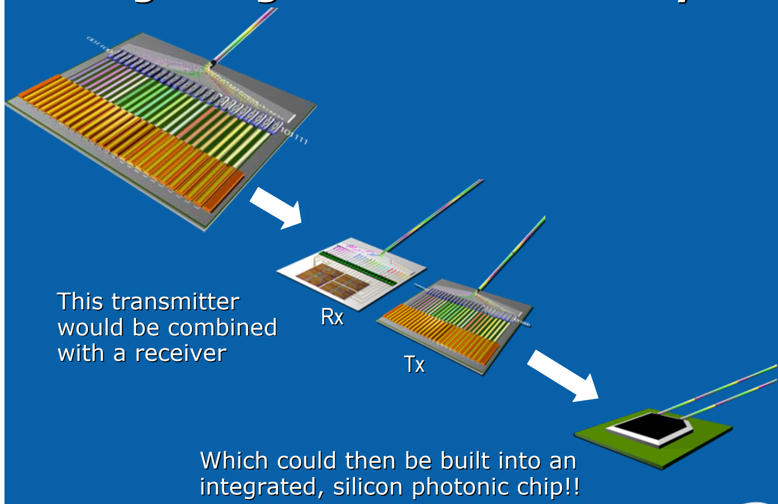
Integrating into a Tera-scale System



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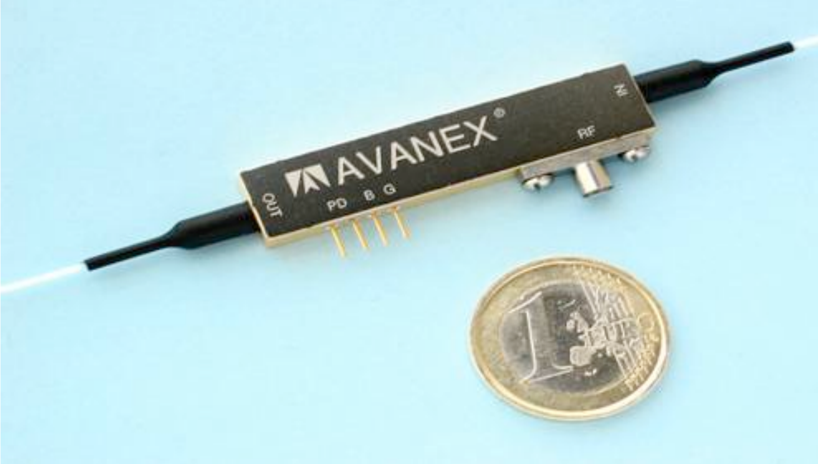
F. Palla INFN Pisa

Some interesting products

http://www.avanex.com/Products/datasheets/Transmission/2613_PwrBitXS10-1700-2000.pdf



SPECIFICATIONS

Parameters		Units
Optical		
Operating Wavelengths Range	C- and L-Band	
Insertion Loss	4	dB
Extinction Ratio (DC), 0-Chirp Version	≥ 20	dB
Note: Prechirped Versions for 1700 ps/nm, 2000 ps/nm or Custom are Available on Request.		
Optical Return Loss (without connectors)	≥ 45	dB
Electrical		
S_{21} Electro Optic Bandwidth (-3 dBe)	12.5	GHz
S_{11} Electrical Return Loss	< - 10	dB
RF V_π Voltage (@ 1 kHz)	5.0	V
Bias V_π Voltage (@1 kHz)	6.9	V
Dynamic Extinction Ratio (0-chirp version)	13	dB
10.7 Gb/s PRBS Electrical Drive Voltage (V_{amp})	5.0	V

CONNECTOR AND FIBER SPECIFICATIONS

RF Input Port	GPO
Bias and VOA Connector	Solder pins
Input Fiber	Corning/Fujikura SM15P UV/UV400
Output Fiber	Corning SMF-28™ or single mode ITU-T G.652[1]

Note 1. Other output fibers available on request.

OKI OL5172M
Integrated Laser+EAM
with small footprint (3.5 cm)
and 2.5 V driving voltage

CIP 10G-LR-EAM-1550
EAM
with footprint (5.1 cm)
and < 4 V driving voltage

4. OPTICAL AND ELECTRICAL CHARACTERISTICS

(T_{LD}= 45°C, Tc=0 to 75°C , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Threshold Current	Ith	CW	---	---	35	mA
Operation Current	Iop	---	---	---	100	mA
Fiber Output Power (Average)	P_{AVG}	If = Iop, under modulation	0	---	---	dBm
Peak Wavelength	λp	If = Iop	1530	---	1565	nm
Side Mode Suppression Ratio	SMSR	If = Iop	35	---	---	dB
LD Forward Voltage	Vf	If = Iop, CW, Vm = 0V	---	---	1.7	V
Monitor Current	Im	If = Iop, CW	50	---	1000	μA
ON-Level Modulation Voltage	Vo	---	-1.0	---	+0.5	V
Modulator Drive Voltage	Vpp	---	---	2.0	2.5	V
Extinction Ratio	ER	Note(1)	9.5	---	---	dB
Dispersion Penalty	DP	800 ps/nm, BER at 10^{-12} Note(1)	---	---	2.0	dB
Tracking Error	TRE	Im=const. 0/25/75°C	- 0.5	---	0.5	dB
TEC Current	Itec	If = Iop	---	---	1.0	A
TEC Voltage	Vtec	If = Iop	---	---	2.5	V
TEC Power Consumption	Ptec	If = Iop	---	0.65	---	W
Thermistor Resistance	Rth	25°C	9.5	---	10.5	kΩ
Thermistor B Value	Bth	25°C/50°C	---	3900	---	K

Note(1)9.95328Gb/s,2^{31}-1NRZ

Conclusions

- **LHC will upgrade its luminosity in about 10 years to 10^{35} cm^{-2} s^{-1}**
  - Phase I (2014?)& II (2020?)
    - Phase I only pixel replacements
    - Phase II is the real challenge with increased radiation doses and huge data rates to cope
- **The largest challenges are**
  - power delivery and distribution
  - provision of triggering data
  - the schedule

  - but many further developments of sensors, readout, cooling,… are also expected

Backup

Lines of investigation in RD50

- Material Engineering -- Defect Engineering of Silicon
  - Understanding radiation damage
    - Macroscopic effects and Microscopic defects
    - Simulation of defect properties & kinetics
    - Irradiation with different particles & energies
  - Oxygen rich Silicon
    - DOFZ, Cz, MCZ, EPI
  - Oxygen dimer & hydrogen enriched Silicon
  - Influence of processing technology

Radiation Damage to Sensors:

- Bulk damage due to NIEL
  - Change of effective doping concentration
  - Increase of leakage current
  - Increase of charge carrier trapping
- Surface damage due to IEL

(accumulation of positive charge in oxide & interface charges)

- Material Engineering-New Materials (work concluded)
  - Silicon Carbide (SiC), Gallium Nitride (GaN)

- Device Engineering (New Detector Designs)
  - p-type silicon detectors (n-in-p)
  - thin detectors
  - 3D detectors
  - Simulation of highly irradiated detectors
  - Semi 3D detectors and Stripixels
  - Cost effective detectors

Available Irradiation Sources in RD50

- 24 GeV/c protons, PS-CERN
- 10-50 MeV protons, Jyvaskyla +Helsinki
- Fast neutrons, Louvain
- 26 MeV protons, Karlsruhe
- TRIGA reactor neutrons, Ljubljana

- Development of test equipment and measurement recommendations

RD50 Silicon Materials under Investigation

standard for particle detectors

used for LHC Pixel detectors

"new" silicon material

Material	Thickness [μm]	Symbol	ρ (Ωcm)	$[O_i]$ (cm^{-3})
Standard FZ (n- and p-type)	50,100,150, 300	FZ	$1–30\times10^3$	$< 5\times10^{16}$
Diffusion oxygenated FZ (n- and p-type)	300	DOFZ	$1–7\times10^3$	$\sim 1–2\times10^{17}$
Magnetic Czochralski Si, Okmetic, Finland (n- and p-type)	100, 300	MCz	$\sim 1\times10^3$	$\sim 5\times10^{17}$
Czochralski Si, Sumitomo, Japan (n-type)	300	Cz	$\sim 1\times10^3$	$\sim 8\text{-}9\times10^{17}$
Epitaxial layers on Cz-substrates, ITME, Poland (n- and p-type)	25, 50, 75, 100,150	EPI	50 – 100	$< 1\times10^{17}$
Diffusion oxyg. Epitaxial layers on CZ	75	EPI–DO	50 – 100	$\sim 7\times10^{17}$

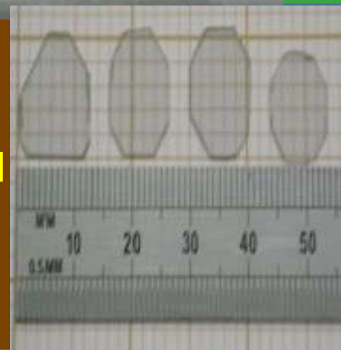
- **DOFZ silicon** - Enriched with oxygen on wafer level, inhomogeneous distribution of oxygen
- **CZ/MCZ silicon** - high Oi (oxygen) and O_{2i} (oxygen dimer) concentration (homogeneous)
  - formation of shallow Thermal Donors possible
- **Epi silicon** - high O_i, O_{2i} content due to out-diffusion from the CZ substrate (inhomogeneous)
  - thin layers: high doping possible (low starting resistivity)
- **Epi-Do silicon** - as EPI, however additional O_i diffused reaching homogeneous O_i content

RD42: Diamond

- Poly crystalline and single crystal
- Competitive (to Si), used in several radiation monitor detectors
- Large band gap (x5 Si)
  - no leakage current
  - no shot noise
- Smaller ε_r (x 0.5 Si)
  - lower input capacitance
  - lower thermal and 1/f noise
- Small Z=6 →large radiation length (x2 in g/cm^2)
- Narrower Landau distribution (by 10%)
- Excellent thermal conductivity (x15)
- Large w_i (x 3.6) →smaller signal charge

- poly-CVD diamond wafers can be grown >12 cm diameter, >2 mm thickness.
- Wafer collection distance now typically 250μm (edge) to 310μm (center).
- 16 chip diamond ATLAS modules

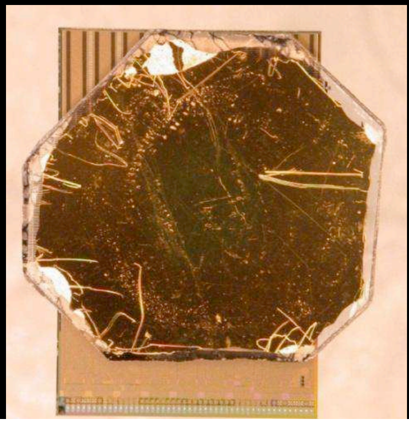
- sc-CVD sensors of few cm^2 size used as pixel detectors
- High quality scCVD diamond can collect full charge for thickness 880μm

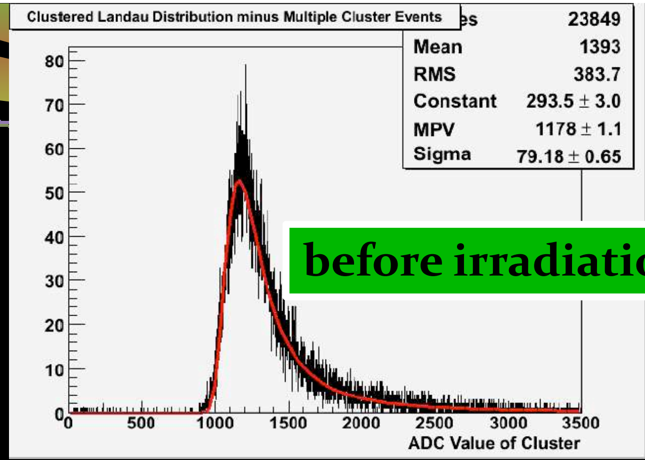


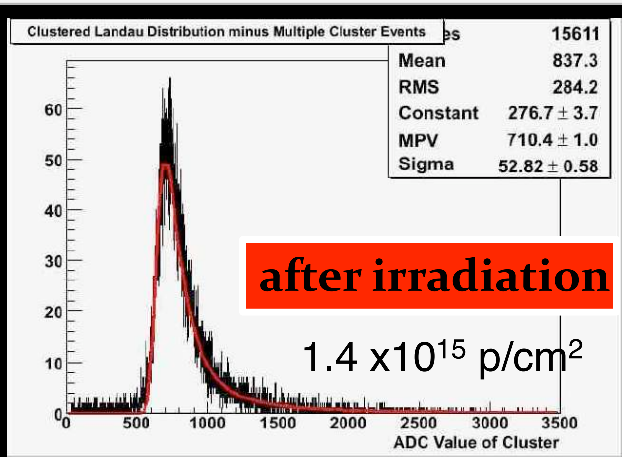
- Industrialize the metallization and bump-bonding
  - Full-size ATLAS pixel module assembled by industrial partner (IZM)

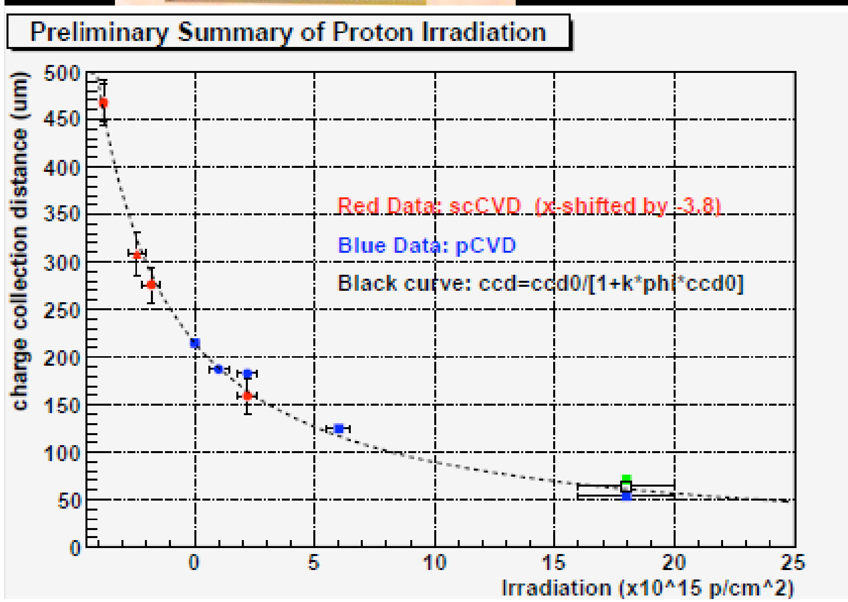
Diamond

- Single crystal diamond pixel detector









- Studies of pCVD (blue) and scCVD diamond (red) at E=1V/μm up to 1.8 × 10^{16} p/cm^2.
- pCVD and scCVD diamond follow the same damage curve:

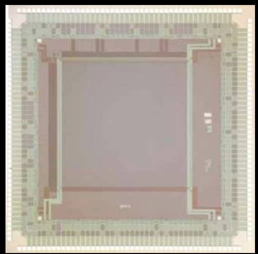
  $1/ccd = 1/ccd0 + k\,\varphi$.

MAPS in SOI

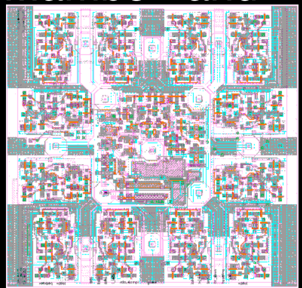
Arai, Deptuch

- HISTORY:
  - F. X. Pengg, “Monolithic Silicon Pixel Detector in SOI Technology”, PhD thesis, University of Linz, Austria, (1996)
  - 2003: W. Kucewicz et al. Nucl.Instrum.Meth.A549:112-116,2005.
  - New development focused on OKI 0.2 μm FD-SOI Pixel Process

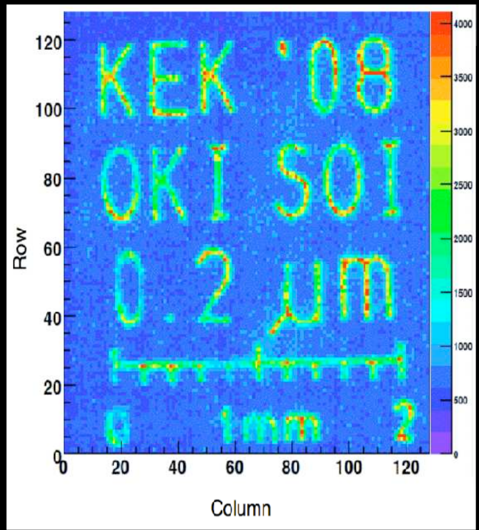
- Integration Type Pixel (INTPIX)



- Mambo I and II

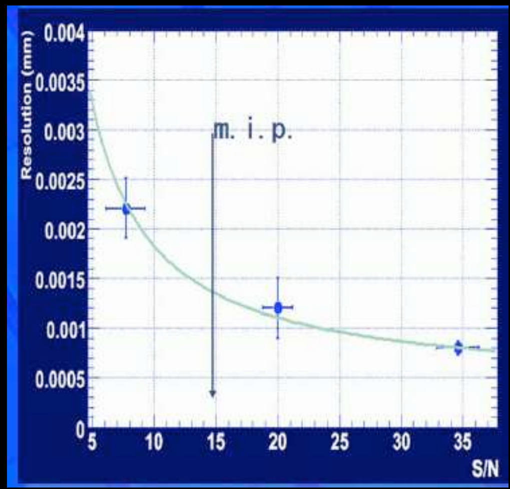


- INTPIX2



2.56 mm

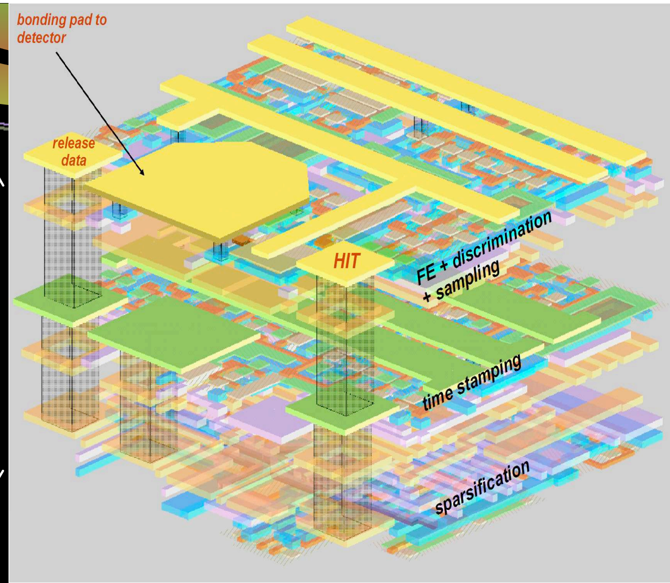
SOI analog 10 μm pixels demonstrate ~ 1 μm resolution

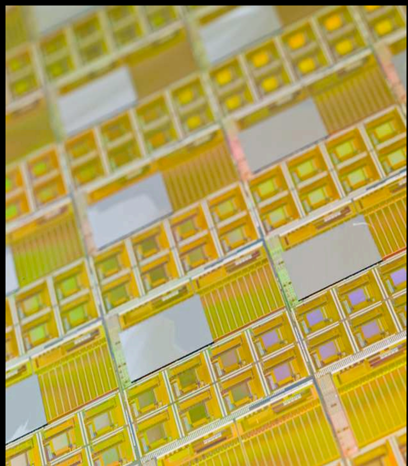


3DIT

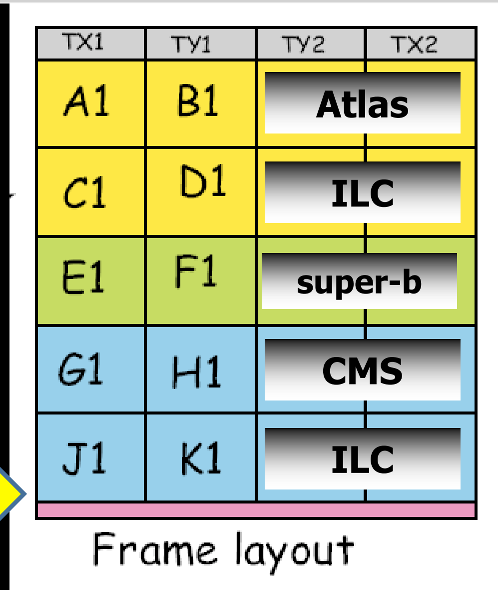
- VIP Pixel readout chip for ILC (FNAL and MIT-LL)
- 64 x 64 pixel array
- Pixel size 20x20 μm
- First demonstration of technology for HEP

22μm





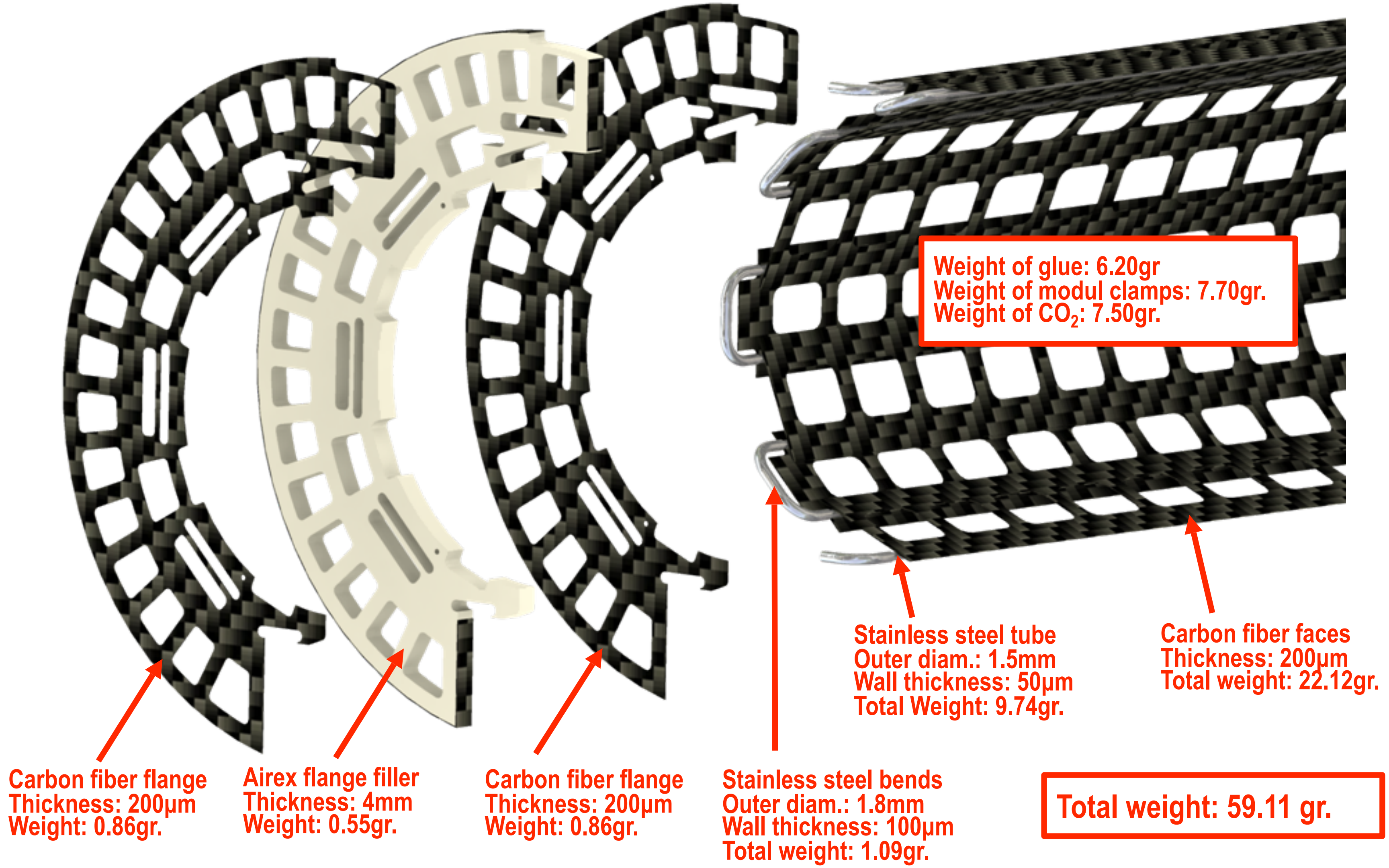
- Demonstrated increased circuit density by integrating 3 circuit tiers
- Showed that extreme circuit thinning (7um) was possible
- Showed that small vias (~1.5 um) were possible thus allowing for small pixel sizes.
- Showed that 3D vias and bonding were reliable



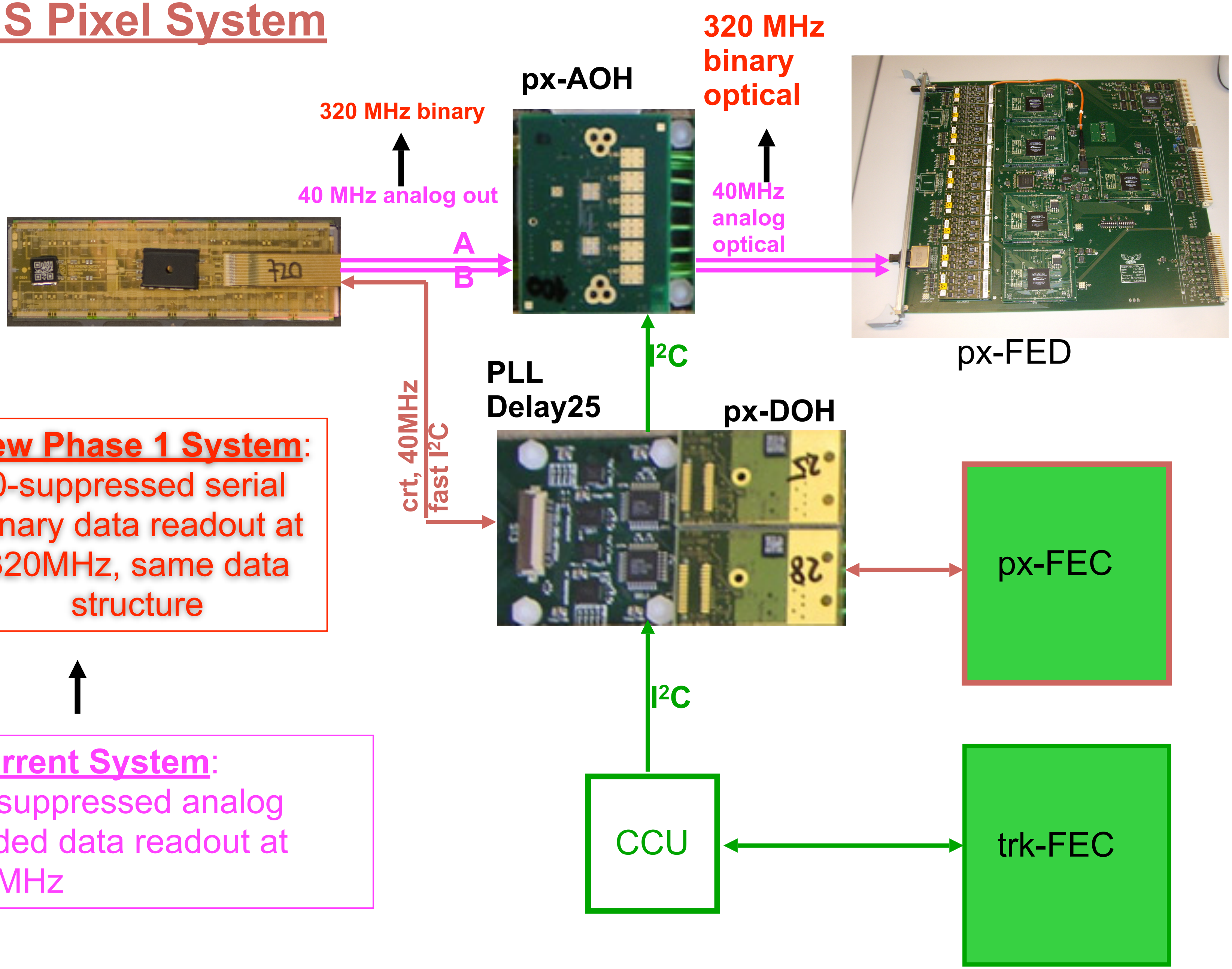
- Multi-Project Wafer run in 3D technology with Tezzaron / Chartered (FNAL and international collaboration)

Italy, France, Germany, USA

PBIX mechanics 2013 in detail



CMS Pixel System



New Phase 1 System: 0-suppressed serial binary data readout at 320MHz, same data structure

Current System: 0-suppressed analog coded data readout at 40MHz

New weight of replacement/upgrade BPIX detector (2013)

	Present BPIX	**New 2013 BPIX**	**Comments**
Empty mechanics	1103 g	550 g	possible, with ~ 94g for 1.5mm/1.4mm pipes
384 Module	872 g	522 g	1.36g/mod no SiN strips 75μ ROC no HV-cap
384 Signal cable	167g	7 g	2 x (2x125μ CCA)
384 Power (6x250μ CCA)	82g	68 g	5x250μ CCA
384 Power plug	16g	0 g	none
32 Print	499 g	32 g	radial power cable to ST
Cooling (C_6F_{14})	810 g	83 g	CO_2 in 1.45mm diam. pipe
Silicon tube incl. fluid	372g	5 g	CO_2 pipes to supply tube
Total	**3921g**	**1267 g**	**factor 3.1 down**

Power Dissipation of Pixel ROC's

- ROC architecture and designs have considerable influence on actual power dissipation
- 3 chips in same 0.25μ technology for same LHC environment

	# Pixels / chip	Pixel area [$m\mu^2$]	Idig [mA]	Iana [mA]	Power/ chip [mW]	Power/ pixel [μW]	Power density [mW/cm^2]
ALICE	8192	21'250	150	300	810	99	466
ATLAS	2880	20'000	35	75	190	67	335
CMS	4160	15'000	32	24	121	29	194
		CMS no on-chip regulators			87	21	142

Average power density of pixel chips = **330 mW/cm^2**

simulated FE amplifier performance

0.13 μm simulation example

for short strips (C_{SENSOR} ~ 5 pF) choose preamp and shaper input device currents (and Rfs) to achieve 50 and 20 nsec CR-RC pulse shapes

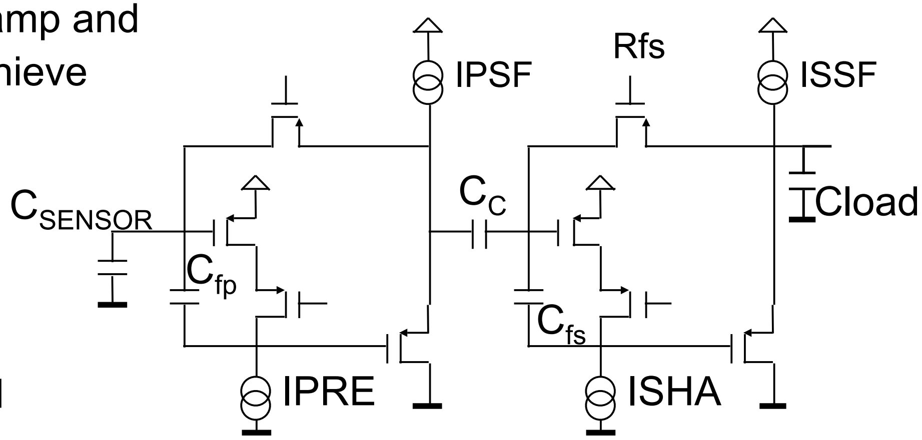
peaking time	50 ns	20 ns
IPRE [uA]	40	90
IPSF [uA]	15	15
ISHA [uA]	10	30
ISSF [uA]	35	15
total [uA]	100	150
power [uW]	120	180
noise [e]	800	890

speed (IPRE, ISHA)

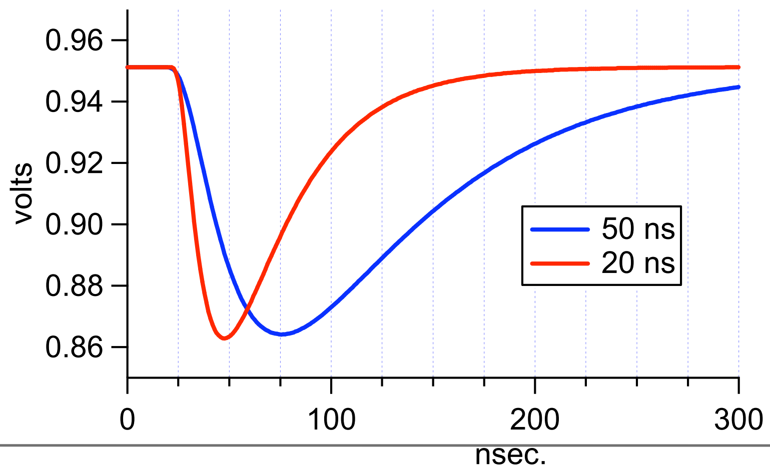
pipe capacitance (ISSF)

=> for short (~few cm) strips can get quite good preamp/shaper noise performance for > factor 5 less than APV (~1 mW) even with only 2 rails

0.13μm preamp/shaper – 2 supply rails only



simulated pulse shapes (C_{SENSOR} = 5 pF)



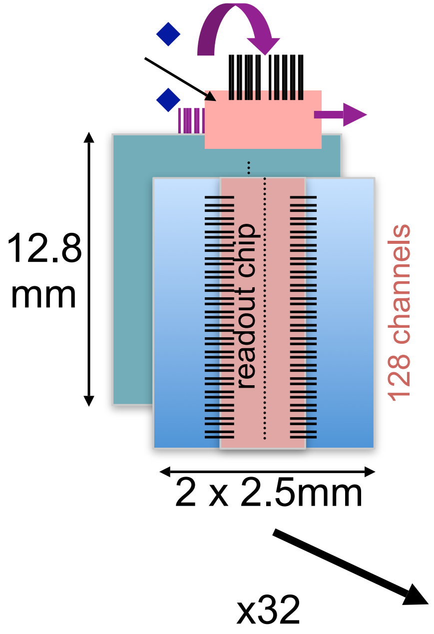
PT layer module

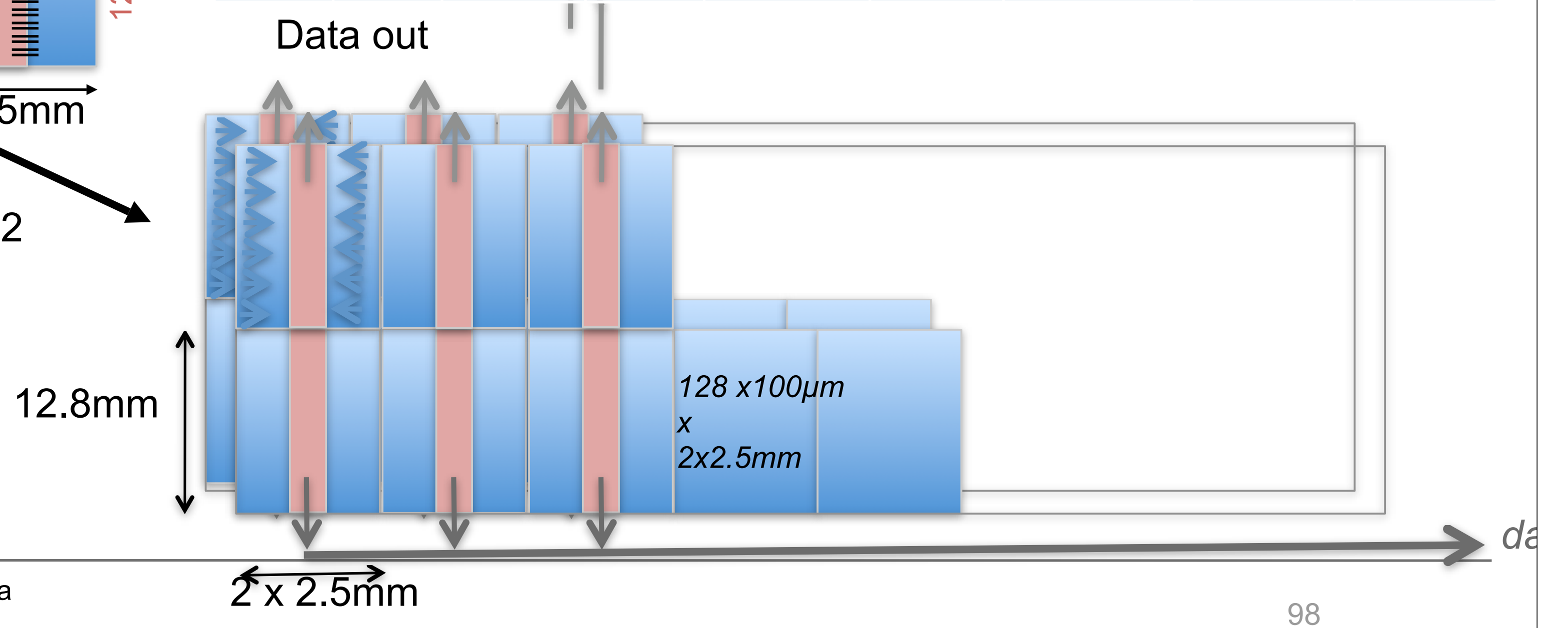
- **Possible "conventional" design (G Hall, M Pesaresi, M Raymond)**

data reduction from correlation ~ x20

transmit remaining data off-detector for L1 logic

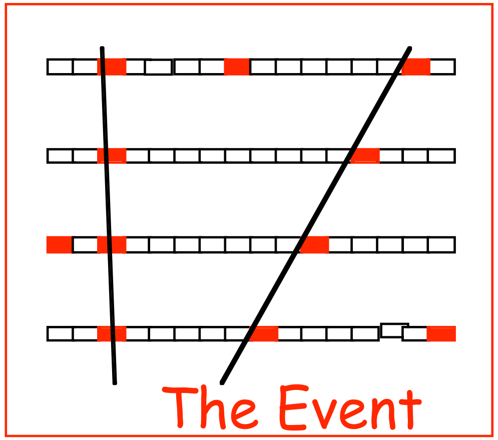
R [cm]	L [m]	A [m²]	N_{face}	N_{chan}	N_{ROC}	N_{module}	N_{links}	P [kw]
25	3.0	9.6	64	38.5M	150k	4700	920	4.6
35	4.2	18.7	88	75M	293k	9200	1790	9.0

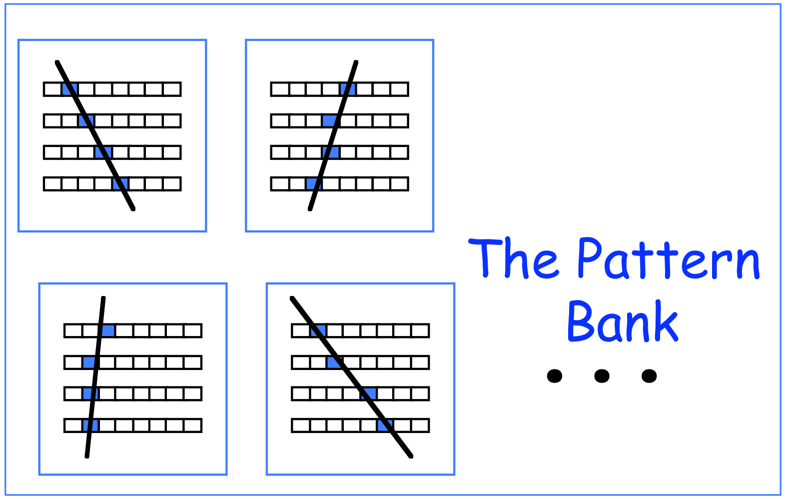




Pattern matching with AM

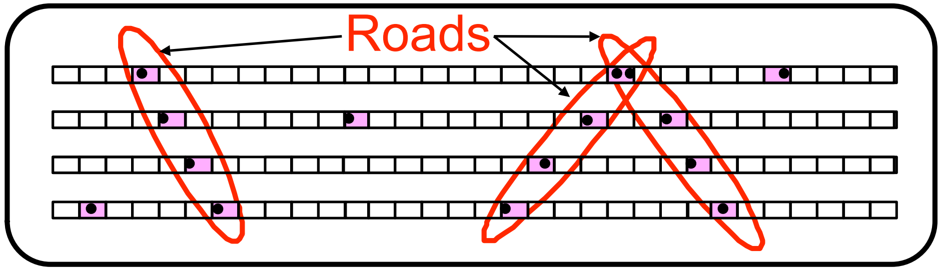
- The pattern bank is a set of pre-calculated patterns
  - can accommodate for alignment
  - changing detector conditions
  - beam displacements
- An Associative Memory holds different patterns banks and compares them with the current event pattern





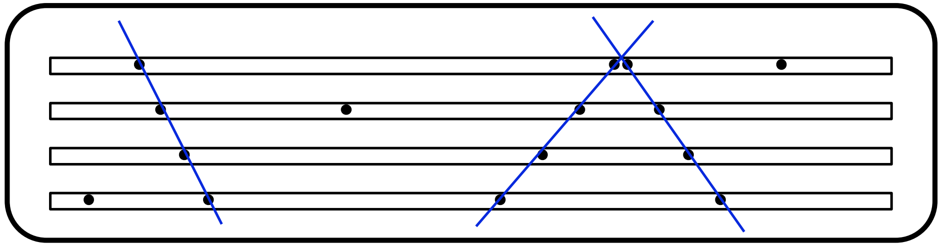
Too large AM? 2 step approach

1. Find low resolution track candidates called "roads". Solve most of the pattern recognition



Super Bin (SB)

2. Then fit tracks inside roads. Thanks to 1st step it is much easier

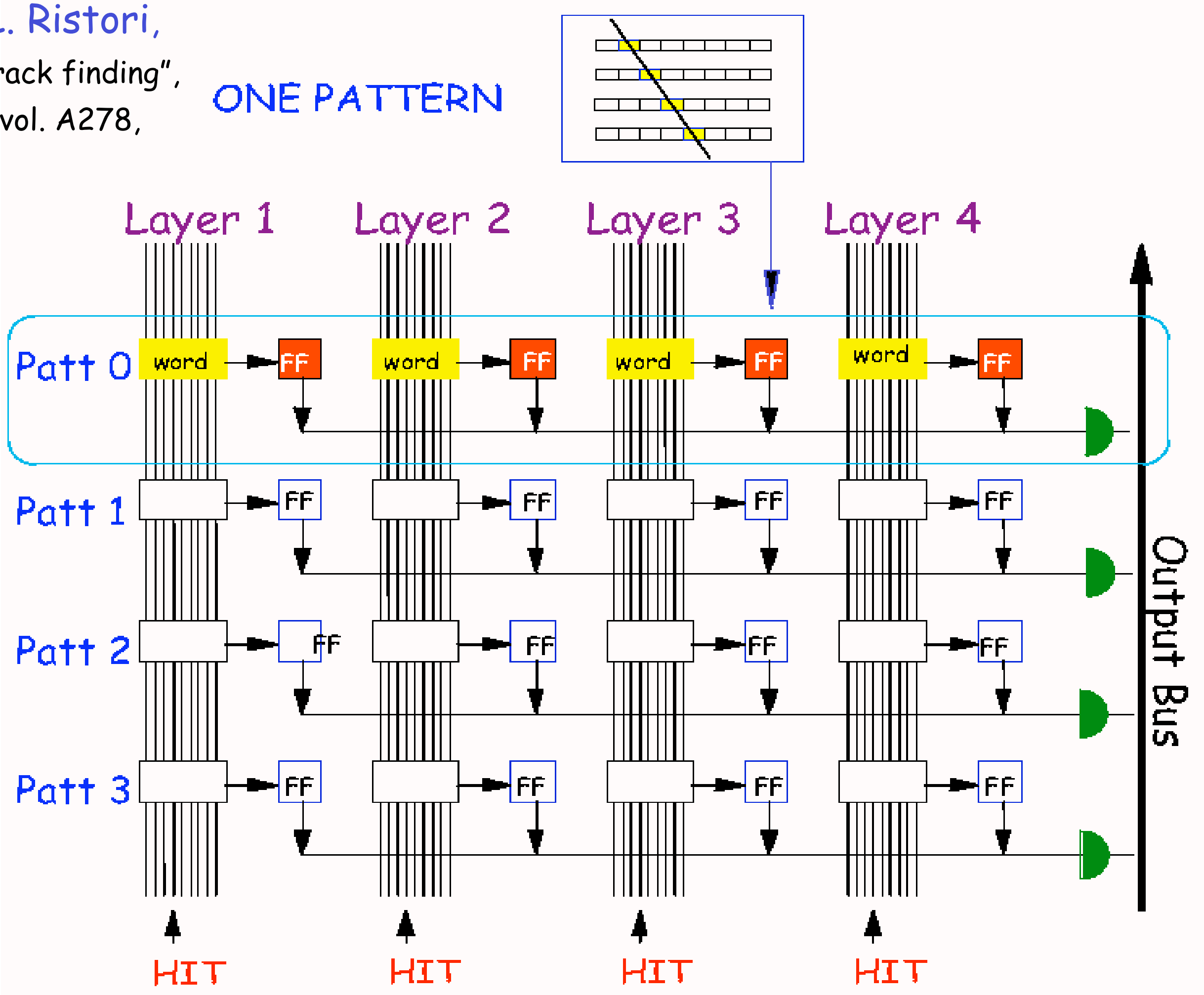


IFF smaller resolution wanted (probably not for Trigger)
OTHER functions are needed:
Hit Buffer + **Track fitter** + **Hit Finder**

Associative Memory for pattern matching

M. Dell'Orso and L. Ristori,
"VLSI structures for track finding",
Nucl. Instr. and Meth., vol. A278,
pp. 436-440, (1989).

1 register
1 comparator
1 match FF
/ layer
/ pattern



Associative memories evolution

- Long history
  - 1990: Full custom VLSI chip - 0.7 μm (INFN-Pisa), 128 patterns/chip: high pattern density, not easy design
  - FPGA approach 1998: easier design but fewer density
  - A good compromise is the standard cell approach currently used for the SVT CDF upgrade: J. Adelman et al., Nuclear Science Symposium, 2005 IEEE, vol. 1, 2005, p. 603.
    - 0.18μm (INFN-Pisa), 5000 patterns/chip, 6 buses input lines, 50 MHz/bus, 18 bits/bus
      - produced by UMC (Taiwan) - design time ~8 months + 2 months production
- Forecast for 2013:
  - 90 or 65 nm technology would allow higher density pattern
  - Factor 4 higher clock speeds achievable
  - All in all: allow to reach ~30K patterns/chip with 200 MHz/bus speed