Radiation effects in devices and technologies

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Radiation effects in devices and technologies

Outline

General view
 Total Ionizing Dose (TID)
 Displacement damage
 Single Event Effects

 SEU, SET
 Destructive events

The LHC

Overall view of the LHC experiments.



The LHC



Radiation Levels in ATLAS

During the experiment lifetime (10 years)

Detector zone	Total dose [rd]	Neutrons (1 MeV eq.) [n/cm ²]	Charged hadrons (> 21 MeV) [n/cm ²]
Pixels	112 M	1.47-10 ¹⁵	2-10 ¹⁵
SCT Barrel	7.9 M	1.4-10 ¹³	1.1-10 ¹⁴
ECAL (barrel)	5.1 k	1.7.10 ¹²	3.6-10 ¹¹
HCAL	458	2.5-10 ¹¹	5.6-10 ¹⁰
Muon det.	24.3 k	3.8-10 ¹²	8.7-10 ¹¹

- TID = energy deposited via ionization per unit mass SI unit = Gy = 100 rd

- Neutron and Ch. Hadrons "intensities: are expressed in fluence = integral of flux over time (10 years in this case)

- Hadrons are particles subject to the strong interaction, mainly p and n (and pions) in our context

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Summary of radiation effects

Total Ionizing Dose (TID)

Potentially all components

Cumulative effects

Displacement damage

Bipolar technologies Optocouplers Optical sources Optical detectors (photodiodes) Permanent SEEs SEL CMOS technologies <u>SEB</u> Power MOSFETs, BJT and diodes <u>SEGR</u> Power MOSFETs

Single Event Effects (SEE)

Static SEEs <u>SEU, SEFI</u>

Digital ICs

Transient SEEs Combinational logic Operational amplifiers

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TID in MOS structures



Trapped charge ALWAYS POSITIVE!

Interface states Can trap both e⁻ and h⁺

Role of interface states

Interface states can trap charge of both polarities. What is their role for NMOS and PMOS structures?



In NMOS, negative

charge is trapped

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In PMOS, positive charge is trapped

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Contributions to the V_T shift



Different evolution of defects

- All charge trapped in the oxide or in the interface states affect the electric field across the oxide (hence the Vt of the structure).

- The evolution of charge trapping and interface state formation during and after irradiation is different. This is very relevant for the overall evolution of the measured behavior.

Example: very thick oxide NMOS



- Annealing, or self-healing, is typically driven by thermal energy or hopping of carriers from the Si layer (only about 3nm range). It is normally effective for trapped charge only, not for interface states (exception recently pointed out for thick field oxides)

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Bias dependence

Bias condition during irradiation is VERY relevant for the radiation effects. During irradiation, the worst-case bias condition "pushes" holes towards the Si-SiO₂ interface.

Example: Vth shift of NMOS in 3 different bias conditions



CMOS 130nm tech W/L=0.16/0.12um

The larger the positive bias, the larger the Vth shift

RULE: Power circuits in their operational condition, or a condition known to be worst-case!

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Transistor level leakage





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Transistor level leakage: example

NMOS - 0.7 μ m technology - t_{ox} = 17 nm



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IC level leakage



The charges trapped in the thick oxide (LOCOS or STI) decrease the Vth of the MOS structure, and the p substrate can be inverted even in the absence of an electric field. A leakage current can appear.

IC level leakage - FoxFETs

Between n+ diffusions





Example: FOXFET nwell-nwell Techno 130nm CMOS W/L=200/0.92um



TID-induced failure

In modern technologies, leakage current is typically the killer



TID in CMOS

Summary of the problems

- Main transistor:
 - Threshold voltage shift, transconductance and noise degradation
 - Effects get negligible in modern deep submicron (as from 250-180 nm techs)
- Parasitic leakage paths:
 - Source drain leakage
 - Leakage between devices
 - This are still potentially deleterious although things looks to be better as from 130nm techs

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Bipolar transistors





Current Gain = $\beta = I_C / I_B$

 $\mathbf{g}_{\mathbf{m}} = \mathbf{I}_{\mathbf{C}} / \mathbf{\phi}_{\mathbf{t}}$

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TID in bipolar devices

Substrate, sidewall and surface inversion (in oxide-isolated processes)



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TID in bipolar devices

Gain degradation: Increase of the surface component of the base current



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Low dose rate (LDR) effect



A.H.Johnston et al., IEEE Trans. Nucl. Science. Vol.41, N.6, 1994

Summary: LDR appears to be consistently inconsistent

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Examples of LDR effects



LDR: possible test procedures

High temperature test (also advised by JPL, but for TID above 30krad)
 JPL advice:

TID _{spec} < 30krad	TID _{spec} > 30krad	
50 & 0.005 rad/s test at room T compare	test up to 30krad in 3 conditions: 50 & 0.005 rad/s at room T, 1rad/s at 90°C	
if failure in any condition	compare	
(@TID<1.5TID _{spec}) => do not use!	if comparable => use 90°C test	
	BUT take an additional $SF = 2$ on TID_{spec}	

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Displacement damage: sensitive devices

✓ Bipolar linear ICs
 ✓ Optocouplers
 ✓ Some type of optical sources
 ✓ Optical detectors

Displacement in bipolar devices

Gain degradation due to increased
 recombination of minority carriers in the base

Displacement damage equation: $1/\beta - 1/\beta_0 = \Phi / [K(2\pi f_T)]$

 β_0 is the pre-rad value, β is the value at a cumulative fluence Φ NB: The majority of linear ICs are still manufactured in old junctionisolated processes, BUT using less conservative approaches (more PNP transistors used in critical places)

 Results on biased and unbiased devices are almost identical

Bipolar technologies

TID

Leakage paths and **β** degradation Sensitive with dose rate effects Variable failure levels Simultaneous effects: <u>they add up</u>

Displacement damage β degradation Voltage regulators, comparators, op amps

Displacement in bipolar devices: example

LM117 positive voltage regulator; effect of TID and displacement add up!



B.G.Rax et al., to be published in IEEE Trans. Nucl. Science, Vol.46, n.6, December 1999

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Displacement in bipolar devices

Effects for lateral and substrate PNP



B.G.Rax et al., to be published in IEEE Trans. Nucl. Science, Vol.46, n.6, December 1999

B.G.Rax et al., to be published in IEEE Trans. Nucl. Science, Vol.46, n.6, December 1999

Displacement damage effects are generally negligible below 3-10¹⁰ p/cm² (50MeV) also for PNP transistors

At levels above about 3-10¹¹ p/cm², they start to become significant also for NPN transistors

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Displacement for optocouplers: example

Radiation tests of the ATLAS DCS front-end electronics at the CERN TCC2 area for the CAN Fieldbus - B. Hallgren

MOCD223 from Motorola HCPL-0731 from HP ILD206A from Siemens => normalized CTR 0.65%
=> normalized CTR 77%
=> normalized CTR 3.5%



B.Hallgren, CERN, 1999

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Ionization from different radiation

Traceable to the energy deposition initiated by one single particle, in a precise instant in time. Due to its stochastic nature, this can happen at any time – even at the very beginning of the irradiation
 Which particles can induce SEEs? In the figure below, a schematic view of the density of e-h pairs created by different radiation is shown.



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Density of e-h pairs is important (1)

 Not all the free charge (e-h pairs) generated by radiation contributes to SEEs. Only charge in a given volume, where it can be collected in the relevant amount of time by the appropriate circuit node, matters



1. Ion strike: ionization takes place along the track (column of high-density pairs) 2. Charges start to migrate in the electric field across the junctions. Some drift (fast collection, relevant for SEEs), some diffuse (slow collection, less relevant for SEEs) 3. Charges are collected at circuit nodes. Note that, if the relevant node for the SEE is the p+ diffusion, not all charge deposited by the ion is collected there.

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Density of e-h pairs is important (2)



The density of pairs depends on the stopping power of the particle, or dE/dx, or Linear Energy Transfer (LET). The figure above (right) shows this quantity in Si for different particles. Even protons, at their maximum stopping power, can not induce SEE in electronics circuits. Only ions, either directly from the radiation environment or from nuclear interaction of radiation (p, n, ...) in Silicon can deposit enough energy in the SV to induce SEEs.

Single Event Upset (SEU) (1)

The e-h pairs created by an ionizing particle can be collected by a junction that is part of a circuit where a logic level is stored (logic 0 or 1). This can induce the "flip" of the logic level stored. This event is called an "upset" or a "soft error". This typically happens in memories and registers. The following example is for an SRAM cell.







e-h pairs in this region recombine immediately (lots of free electrons available in this n+ region)

Depletion region: e-h pairs are collected by n+ drain and substrate => those collected by the drain can contribute to SEU

High density of e-h pairs in this region can instantaneusly change effective doping in this low-doped region, and modify electric fields. This is called "funneling". Charge can hence be collected from this region to the n+ drain, although a portion of it will arrive "too late" to contribute to SEU

Single Event Upset (SEU) (2)

1. Initial condition (correct value stored)



Charge collected at the drain of NMOS T1 tends to lower the potential of the node B to gnd. PMOS T2 provides current from Vdd to compensate, but has a limited current capability. If the collected charge is large enough, the voltage of node B drops below Vdd/2 2. Final condition (wrong value stored)



When node B drops below Vdd/2, the other inverter in the SRAM cell changes its output (node A) to logic 1. This opens T2 and closes T1, latching the wrong data in the memory cell.

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"Digital" Single Event Transient (SET)

 Particle hit in combinatorial logic: with modern fast technologies, the induced pulse can propagate through the logic until it is possibly latched in a register
 Latching probability proportional to clock frequency
 Linear behaviour with clock frequency is observed



"SEU" in optical receivers (1)



"SEU" in optical receivers (2)



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SEU cross-section (1)

- Sensitivity of a circuit to SEU (or in general to any SEE) is characterized by a cross-section
- The cross-section contains the information about the probability of the event in a radiation environment

Example: what is the error rate of an SRAM in a beam of 100MeV protons of flux 10⁵ p/cm²s?

1. Take the SRAM and irradiate with 100MeV proton beam. To get good statistics, use maximum flux available (unless the error rate observed during test is too large, which might imply double errors are not counted => error in the estimate)

100MeV SRAM

2. Count the number of errors corresponding to a measured fluence (=flux x time) of particles used to irradiate

Example: N of errors = 1000Fluence = 10^{12} p/cm²

Cross-section (σ)= N/F = 10⁻⁹ cm²

3. Multiply the cross-section for the estimated flux of particles in the radiation environment. The result is directly the error rate, or number of errors per unit time.

If $(\sigma) = 10^{-9} \text{ cm}^2$

and flux = $10^5 \text{ p/cm}^2\text{s}$

Error rate = 10^{-4} errors/s

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SEU cross-section (2)

- In reality, things are generally more difficult the real radiation environment is a complex field of particles
- One needs models to translate cross-sections measured at experimental facilities (protons or heavy ions beams) into error rates in the field
- The better the experimenter knows the sensitivity of the circuit, the better he/she can estimate the error rate in the real environment
- Heavy lons (HI) irradiation tests are very good to probe completely the sensitivity of a circuit. With HI, it is possible to vary the LET of the particles (hence the energy deposited in the SV), and measure the correspondent cross-section.

cross section (cm^2)

LET= 1 MeVcm²/mg



The path of this particle in the SV is 1um. Since the density of Si is 2.32g/cm³, the energy deposited in the SV is about 232keV. If the LET is changed, by changing the

ion, to 5, then the deposited energy exceeds 1MeV.

It is possible to chart the measured cross-section for different LET of the ions, as shown in the figure to the right.



SEU cross-section (3)

- Heavy ions tests are more expensive and more complicated to perform (few facilities, need to expose circuit without package)
- As an alternative, for High Energy Physics applications (in particular for LHC detectors) it is possible to rely on mono-energetic proton beam data
- Given the complexity of the radiation field in the LHC experiments, a study has been carried with the help of Monte-Carlo simulation codes and main results and implications are discussed in the following

SEU rate estimate in LHC

Hadron-dominated particle environment
 Hadrons have low LET, no "direct" SEU
 Nuclear interaction probability has to be computed, with LET and track of the fragments
 This work has been carried on in a collaboration RD49/CMS, and published
 Main conclusions highlighted here (see the following paper for more details)

M.Huhtinen, F.Faccio, "Computational method to estimate Single Event Upset rates in an accelerator environment", Nuclear Instruments and Methods in Physics Research A 450 (2000) 155-172

Simulation geometry & methods

- Monte-Carlo simulation approach
- ✓ Different SV shape and size used
- SV surrounded by silicon and topped by a 6µm SiO₂ layer (equivalent to Si)
- Event generators to compute the interaction probability and produced recoils

Energy loss of all recoils computed



"Threshold energy"

- There is a "threshold energy" of the incoming particle, below which the probability of observing an SEU drops dramatically
 - This can be easily explained when looking at the curve to the right, which depicts the probability to produce, from nuclear interaction, fragments of the energy indicated along the X axis: the lower the energy of the incoming particle (neutrons in this case), the lower the energy of the fragments – hence the lower the energy they can deposit in the SV
 - As a consequence, It is not useful or at best difficult to exploit – to test for SEEs with beams below 50-60MeV. Nonetheless, very modern CMOS technologies that are very sensitive can have the same cross-section above some 15-20MeV, so this "threshold energy" is lower than for older technologies



Probability curves

- The main output of the simulation is a probability curve for a given SV size and a given radiation environment
 - The curve is plotted with the energy deposited in the SV as X axis (E_{dep})
 - On the Y axis, there is the probability (per unit flux and per unit SV) for any energy deposition. This contains the information on how often an energy EQUAL OR LARGER than E_{dep} is deposited in the SV

Example of the use of one such curve

- The curve to the right is for a SV of 1µm³ in a mono-energetic proton beam of 20, 30, 60 and 200 MeV.
- Suppose that we have a circuit whose threshold for SEU corresponds to a deposition of 1MeV in the SV. Every time an energy equal or larger than 1MeV is deposited, the circuit has an SEU
- The error rate in a 200MeV proton beam is the probability at E_{dep}=1MeV multiplied by the proton flux

Rate = probability x flux



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Influence of the environment

- The comparison of the probability curve for different radiation environments is very interesting
 - In the figure below, the comparison between a mono-energetic 60MeV proton beam and the complex CMS tracker environment is shown
 - The probability curves are very similar. This implies that a reasonable estimate of the error rate in the CMS tracker environment (and hence in the LHC experiments) can be obtained by measuring the cross-section of the circuit in a proton beam of at least 60MeV
- The suggested procedure for the estimate is therefore:
 - 1. Measure the σ in a 60MeV proton beam (or higher energy if available)
 - 2. Multiply the σ for the flux of particles in the LHC environment, where only hadrons above 20MeV have to be counted
 - The procedure is based on the assumption, which appears reasonable from this study, that all hadrons above about 20MeV have roughly the same effect on the circuit (hence their σ is very comparable)



Conclusions of the simulation work

- Despite the large number of approximations in the model, a good agreement with available experimental data has been found
- SEU rates in LHC will in most devices be dominated by hadrons with E>20MeV. It is reasonable to assume in the estimate that all hadrons above 20MeV have the same effect
- ✓ To estimate error rates in LHC, use proton beams of 60-200MeV to measure the cross-section of the circuits. Multiply the measured s for the flux of hadrons with E>20MeV in the location where the circuit has to work. This procedure has been adopted by all LHC experiments as a "standard" for circuit qualification
- A useful information to situate the sensitivity of circuits in the LHC is the maximum LET of recoils from nuclear interaction of hadrons with the Si nuclei. The maximum LET is for a Si recoil and the LET is about 15 MeVcm²mg⁻¹. This information can be used to judge if a circuit for which Heavy Ion data is available will experience a high error rate in the LHC.

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Destructive SEEs (Hard errors)

✓ SEBO => Single Event Burnout occurring in power MOSFET, BJT (IGBT) and power diodes ✓ SEGR => Single Event Gate Rupture occurring in power MOSFET => Single Event Latchup ✓ SEL occurring in CMOS ICs They can be triggered by the nuclear interaction of charged hadrons and neutrons

Single Event Latchup (SEL)

Electrical latchup might be initiated by electrical transients on input/output lines, elevated T or improper sequencing of power supply biases. These modes are normally addressed by the manufacturer.

Latchup can be initiated by ionizing particles (SEL) in any place of the circuit (not only IOs) $$V_{\rm DD}$$



A.H. Johnston et al., IEEE TNS, Apr. 1996

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SEL: experiments

- Experiments aim at measuring the cross-section. To avoid destruction after the first occurrence, power (both core and I/Os) has to be shut off promptly upon detection of the SEL
- SEL sensitivity is enhanced by temperature, hence the test should be done at the maximum foreseen T
- Though in general modern technologies should be less sensitive to SEL, there are exceptions!
- SEL can be induced by high energy protons and neutrons
 - This is not very frequent, but in literature one can find at least 15-20 devices for which SEL was experimentally induced by proton or neutron irradiation
 - When looking at devices for which Heavy Ion data exist in literature, a rule of a thumb is: if they do not latch below an LET of 15 MeVcm²mg⁻¹, they will not latch in a proton-neutron environment. In fact, typically they need to have an SEL threshold around 4 MeVcm²mg⁻¹ to be sensitive (but take this figure with precaution, since it is base on little statistics available...)
 - If a component is suspected to be sensitive, use high energy protons for the test (the SEL cross-section can be even 15 times larger for tests at 200MeV than for tests with 50MeV protons). Also, use a large fluence of particles for the test – at least 5x10¹⁰ cm⁻² – and to enhance SEL probability increase the T during the test

SEBO (SEB)

Double-diffused MOS (DMOS) power transistor and power BJT transistors are vulnerable

Power DMOS Metal Polysilicon Gate Polysilicon Gate Gate Oxide P+ Plug N+ Substrate Drain Contact





J.H.Johnson & K.F.Galloway, IEEE NSREC short course, 1996

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SEBO (SEB)

Mechanism: passage of the ion in the OFF state, generating a transient current. A regenerative feedback occurs until second breakdown sets in and permanently destroys the device (short source-drain or emitter-collector).



J.H.Johnson & K.F.Galloway, IEEE NSREC short course, 1996

Important mechanism in the regenerative feedback: avalanchegenerated hole current in the collector region of the parasitic (or main) bipolar transistor.

SEB Example: DC-DC converter (1)

Power MOSFETs used in candidate DC-DC converter for LHC were mounted in test cards (below, left) and irradiated a different Vds with 60MeV protons. Burnout started from a Vds of about 350V.





SEB Example: DC-DC converter (2)

From previous curve and with analysis of the converter, it is possible to select a working condition where Vds of the MOSFET never exceeds 300V (this technique is called "derating" and is often used)



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SEGR in power MOSFETs

SEGR is caused by heavy-ion-induced localized dielectric breakdown of the gate oxide. SEGR test is destructive!



J.H.Johnson & K.F.Galloway, IEEE NSREC short course, 1996

SEGR in ULSI CMOS

Recent concerns in possible trend of SEGR in modern technologies



F.W. Massengill et al., "Heavy-Ion-Induced Breackdown in Ultra-Thin Gate Oxides and High-k Dielectrics", *IEEE Transactions on Nuclear Science*, vol. 48, no. 6, December 2001, pp. 1904-1912.

SEGR does not seem to be a problem even in the most advanced CMOS processes

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Summary Table

Device	TID	Displacement	SEEs	
Low voltage CMOS	Yes ¹	No	SEUs in logic and memories SETs relevant if fast logic (1GHz) SEL possible ²	
Low voltage Bipolar	Yes, with ELDR possible	Yes ³	SEL extremely rare – if at all SETs	
Low voltage BiCMOS	Yes	Yes	Combination of CMOS and Bipolar	
Power MOSFETs	Yes	Yes at very large fluence (>10 ^f)	SEB SEGR	
Power BJTs	Yes	Yes	SEB	
Optocouplers	Yes	Yes	SETs	
Optical receivers	Yes	Yes (tech dependent)	"SEUs"	

¹The threshold for sensitivity varies with technology generation and function. Typically failures are observed from a minimum of 1-3krd, and sensitivity decreases with technology node (130nm less sensitive than 250nm for instance)

²Sensitivity typically decreases with technology node. When Vdd goes below about 0.8-1V, then SEL should not appear any more

³Sensitivity depends on doping and thickness of the base, hence decreasing in modern fast processes

Particles and damages

Radiation	TID	Displacement (NIEL)	SEE
X-rays ⁶⁰ Co γ	Expressed in SiO_2 Almost identical in Si or SiO_2	No	No
p	Equivalences in Si ^{\$} @60MeV 10^{11} p/cm ² =13.8krd @100MeV 10^{11} p/cm ² =9.4krd @150MeV 10^{11} p/cm ² =7.0krd @200MeV 10^{11} p/cm ² =5.8krd @250MeV 10^{11} p/cm ² =5.1krd @300MeV 10^{11} p/cm ² =4.6krd @23GeV 10^{11} p/cm ² =3.2krd	Equivalences in Si ^{\$,*} @53MeV 1 p/cm ² = 1.25 n/cm ² @98MeV 1 p/cm ² = 0.92 n/cm ² @154MeV 1 p/cm ² = 0.74 n/cm ² @197MeV 1 p/cm ² = 0.66 n/cm ² @244MeV 1 p/cm ² = 0.63 n/cm ² @294MeV 1 p/cm ² = 0.61 n/cm ² @23GeV 1 p/cm ² = 0.50 n/cm ²	Only via nuclear interaction. Max LET of recoil in Silicon = 15MeVcm ² mg ⁻¹
n	Negligible	Equivalences in Si ^{\$,*} @1MeV 1 n/cm ² = 0.81 n/cm ² @2MeV 1 n/cm ² = 0.74 n/cm ² @14MeV 1 n/cm ² = 1.50 n/cm ²	As for protons, actually above 20MeV p and n can roughly be considered to have the same effect for SEEs
Heavy Ions	Negligible for practical purposes (example: 10 ⁶ HI with LET=50MeVcm ² mg ⁻¹ deposit about 800 rd)	Negligible	Yes

^{\$} Energy here is only kinetic (for total particle energy, add the rest energy mc²)

*The equivalence is referred to "equivalent 1Mev neutrons", where the NIEL of "1MeV neutrons" is DEFINED to be 95 MeVmb. This explains why for 1MeV neutrons the equivalence is different than 1

To study further...

General material on radiation effects:

- The best source is the "archive of Radiation Effects Short Course Notebooks, 1980-2006" collecting the courses given at the IEEE NSREC conference (CD sold by IEEE)
- "Classic" books on the subject
 - "Ionizing radiation effects in MOS devices and circuits", edited by T.Ma and P.Dressendorfer, published by Wiley (2001), ISBN 978-0471848936
 - "Handbook of radiation effects", by A.Holmes-Siedle and L.Adams, published by Oxford University Press (2002), ISBN 978-0198507338
- Recent Books with good overview of all effects:
 - "Radiation effects on Embedded Systems", edited by R.Velazco, P.Fouillat, R.Reis, published by Springer (2007), ISBN 978-1-4020-5645-1
 - "Radiation effects and soft errors in integrated circuits and electronic devices", edited by R.Schrimpf and D.Fleetwood, published by World Scientific (2004), ISBN 981-238-940-7
- Best papers from the Nuclear and Space Radiation Effects Conference (NSREC) are published yearly in the IEEE TNS in the december special Issue

Specialized conferences:

- NSREC in the US, yearly in July
- RADECs in Europe, conference (1 week) or workshop (2-3 days) every year in September