Università di Roma Tor Vergata

Sistemi riconfigurabili e software radio per applicazioni satellitari

(parte 1)

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Motivations

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- Satellite on-board processing includes:
  - Telecom systems
  - Mass memory
- For long mission they require:
  - Flexibility
  - Reliability (Fault-Tolerance)
  - Reduced weight and power consumption
- Possible solutions are:
  - Use of Software Defined Radio *
  - Solid state mass memories **

* ESA Project: **Software Radio Based Regenerative Processor**
** ASI Project: Solid State Mass Memory for Space Applications

What is SDR and why in Space

"Software radio is an emerging technology thought to build flexible radio systems, multiservice, multistandard, multiband, reconfigurable and reprogrammable by software" *

SDR offers important benefits:

- global roaming, multi mode, multi band, multi standard capability
- complete programmability and reconfigurability to both multi-mode and multi-functional communication terminals and network nodes by using reprogrammable components (DSPs, FPGAs)

*** *E. Buracchini, CSELT,* The Software Radio Concept, pp. 138-143,**
IEEE Communications Magazine September 2000

Basic scheme

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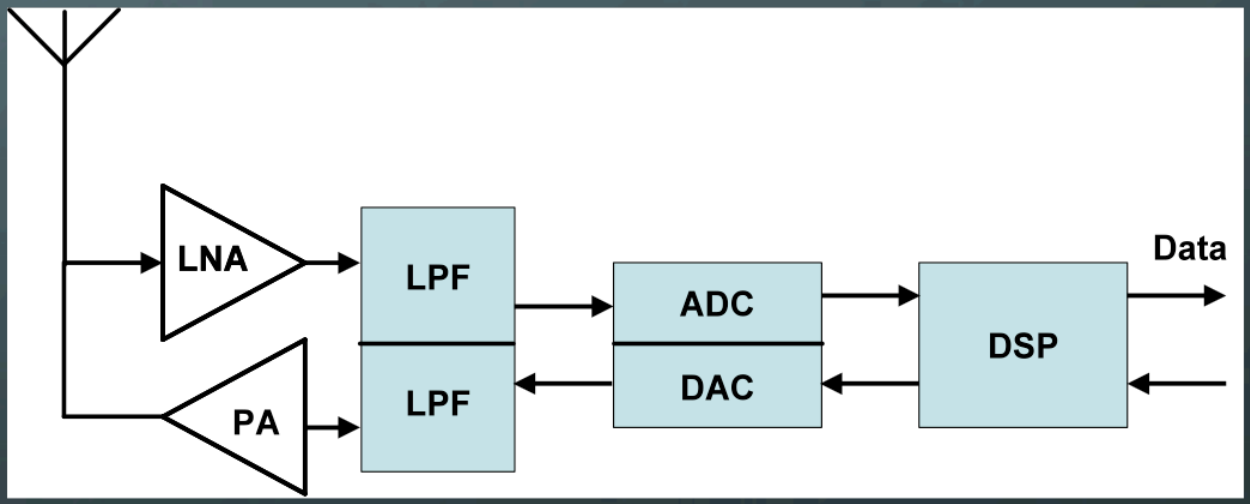
Enabling technique toward the software radio implementation:

Digital Signal Processing

In particular **its expansion toward the antenna**, i.e. to regions where analog signal processing is dominant.

Reprogrammable Hardware **platforms** where most of the analog signal processing is replaced by digital signal processing



DSR Feasibility

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Analog input stage limitations

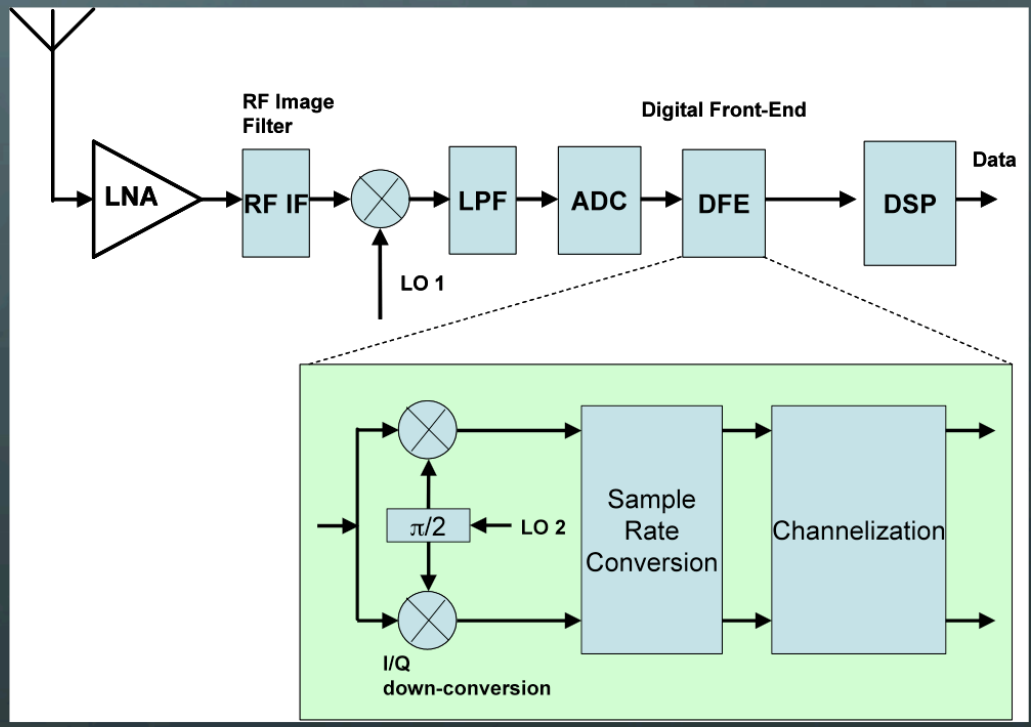
Very high performance receiver analog section (basically the LNA stage) characterized by large bandwidth and high linearity

ADC-DAC limitations

constraints are very critical for space applications where rad-hard components are mandatory !!!

POSSIBLE SOLUTIONS

Partial Band digitalization



SDR in space

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- Different operative modes *
  - *Full reconfiguration with new algorithms:*
    - *To implement a totally new signal processing architecture.*
    - *The signal path is interrupted and the communication service is suspended during the reconfiguration phase*
  - *Partial reconfiguration with new algorithms:*
    - *Only a portion of the reconfigurable device is involved in the reconfiguration and then the not affected portion continue the processing task.*
  - *Upgrade algorithms:*
    - *a limited portion of one or more signal processing algorithms is involved in the reconfiguration process; the nominal processing of the algorithm is affected during the reconfiguration time but this could not impact on the communication service*
  - *Parameters modification:*
    - *Possible if the parameters to be updated are stored in writable registers.*
    - *This very limited reconfiguration and does not affect the signal path at processor level though it may change some parameters in the end-to-end system.*
  - *Add-on algorithms:*
    - *This reconfiguration consists of adding one or more new algorithms to upgrade the functionalities of the processor to satisfy new requirements.*

* ESA Project: **Software Radio Based Regenerative Processor**

Hardware Devices

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- Depending on the characteristics of the processing we can use
  - Hardware processing (ASIC or FPGA)
  - Software processing (Microprocessors and DSPs)
- Use of techniques for Hardware/Software codes
- Fault-tolerant techniques must consider both these aspects
- It is possible to exploit the arithmetic characteristics of the processing

Electronic systems and space

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- Require fault-tolerance capability
- Different redundancy for hardware based systems
  - Hardware redundancy
  - Information redundancy
  - Time redundancy
- For software systems
  - Software redundancy
- For hardware and software systems
  - Mixed techniques

Hardware redudancy

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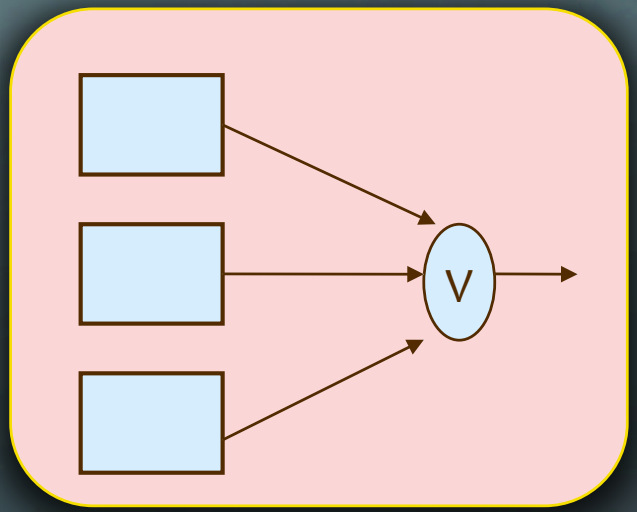
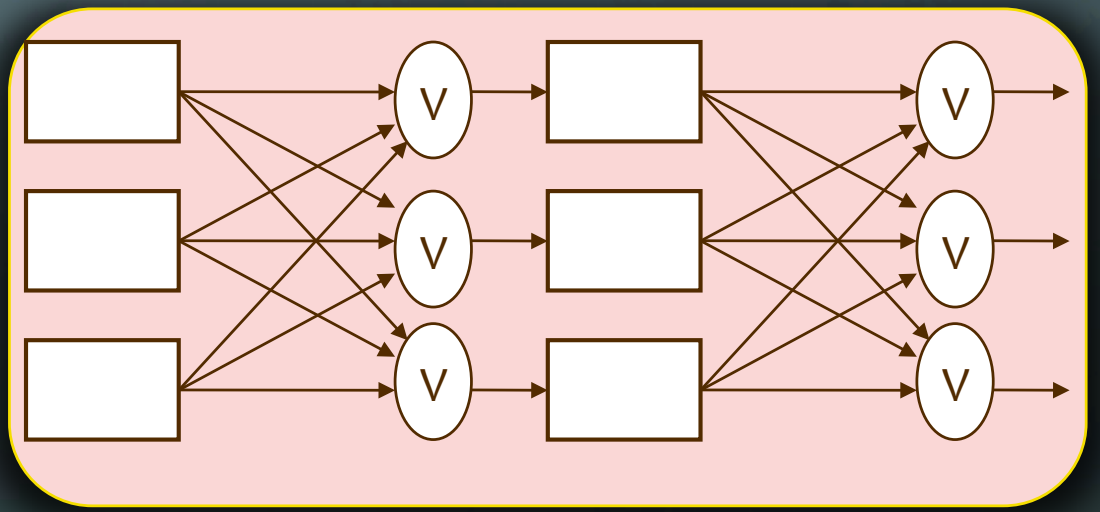
- Passive redudancy
  - NMR
- Also Multistage





Hardware redundancy active

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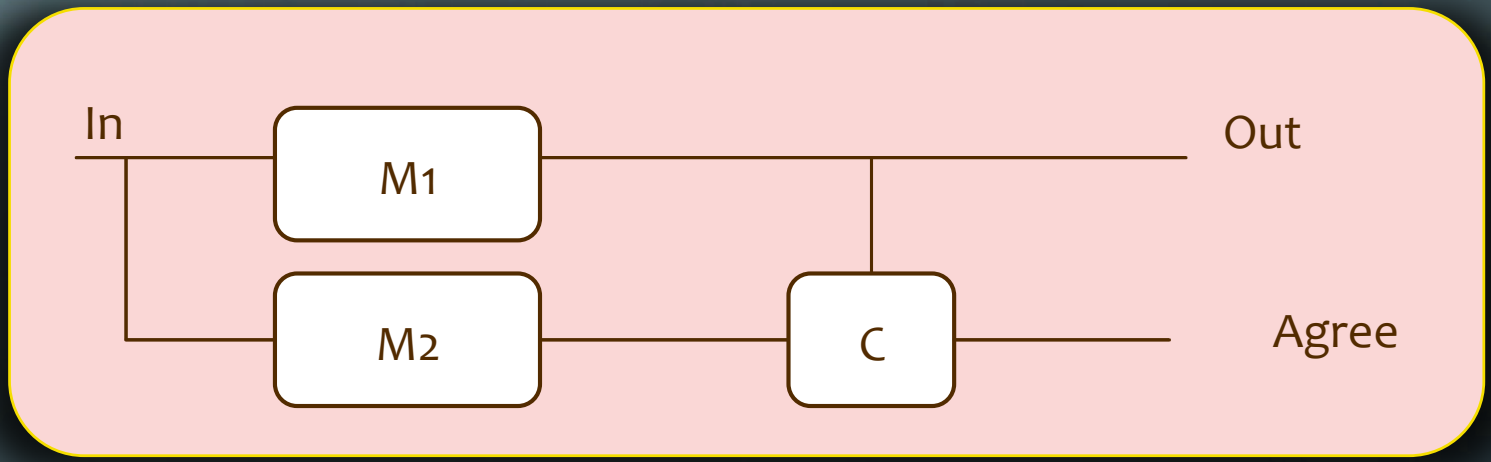
- Reduced redudancy level
- Only for error detection
- Error recovery requires active action (reconfiguration)



Hardware redundancy characteristics

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- Advantages
  - General purpose techniques
  - Applicable to blocks different grained
  - Passive redundancy don’t require reconfiguration
- Disadvantages
  - Very expensive redundancy
  - High power consumption
  - Low integration level

Information redundancy

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- Based on coding techniques derived from telecom techniques for data protection
- Based on the introduction of additional bits in the information word

Code are

- Systematic
- Non-systematic

Starting from m bit datawords to n=k+m bit codewords adding k check bits (systematic code)

Are able to perform

- Error detection
- Error detection and correction

Example: systematic

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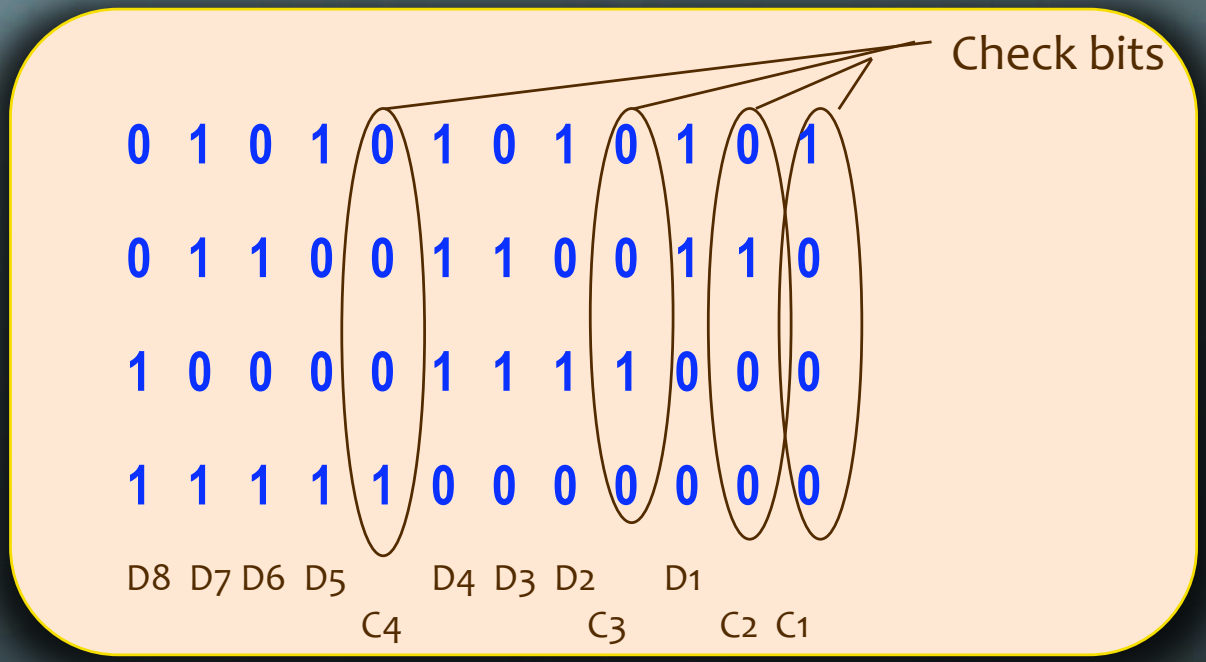
- Overlapped parity
- ECC code

m = data bits
k = parity bits



Computation of bits

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- Check bits

$C1 = D1 \oplus D2 \oplus D4 \oplus D5 \oplus D7$

$C2 = D1 \oplus D3 \oplus D4 \oplus D6 \oplus D7$

$C3 = D2 \oplus D3 \oplus D4 \oplus D8$

$C4 = D5 \oplus D6 \oplus D7 \oplus D8$

- Example
  - data = 1110 0001
  - compute check bits:

$C1 = 1 \oplus 0 \oplus 0 \oplus 0 \oplus 1 = 0$

$C2 = 1 \oplus 0 \oplus 0 \oplus 1 \oplus 1 = 1$

$C3 = 0 \oplus 0 \oplus 0 \oplus 1 = 1$

$C4 = 0 \oplus 1 \oplus 1 \oplus 1 = 1$

Error detection & correction

- Example
  - Dataword= 1110 0001 computed check bits = 1110
  - Received Codeword= 01100001 check bits = 1110
  - Receiver computed check bits

$$C1=1 \oplus 0 \oplus 0 \oplus 0 \oplus 1 = 0$$
$$C2=1 \oplus 0 \oplus 0 \oplus 1 \oplus 1 = 1$$
$$C3=0 \oplus 0 \oplus 0 \oplus 0 = 0$$
$$C4=0 \oplus 1 \oplus 1 \oplus 0 = 0$$

Syndrome: 1110 XOR 0010 = 1100 Bit 8 is wrong

Use of codes for h/w

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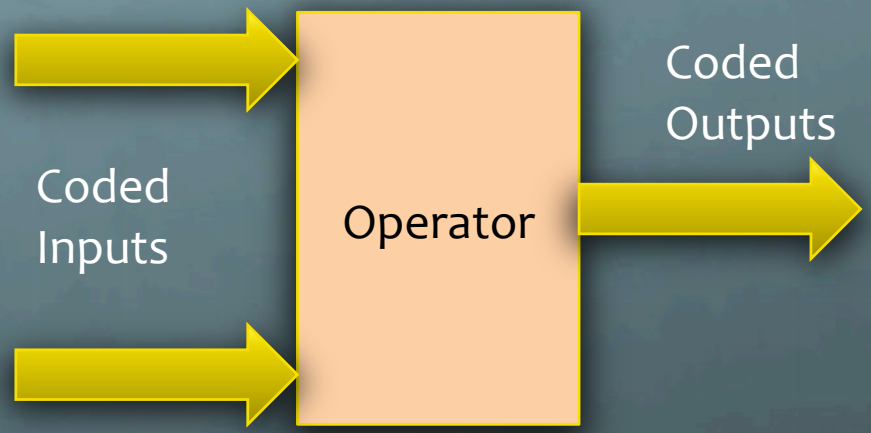
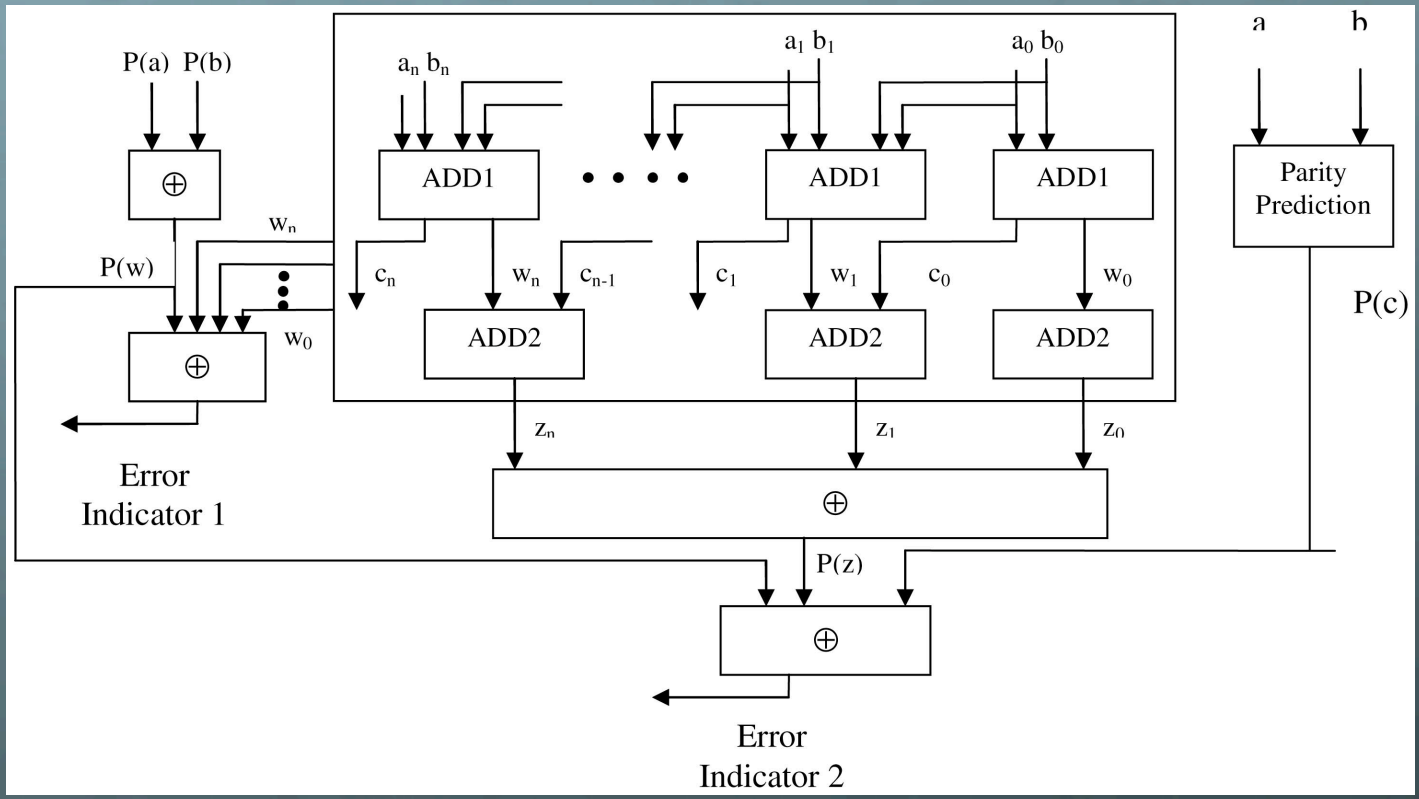


Properties of codes depend on the operators

- For DSP arithmetic codes are useful (for example RNS)

Example: Radix2 SD Adder



1. Parity Prediction, generates the value of P(c);
2. Error Indicator 1, checks P(W)= P(A) XOR P(B) and issues an error signal in case of a mismatch;
3. Error Indicator 2, checks P(Z)= P(C) XOR P(W)and issues an error signal in case of a mismatch;

Fault Localization, Error Correction, and Graceful Degradation in Radix 2 Signed Digit-Based Adders, IEEE TRANSACTIONS ON COMPUTERS, MAY 2006

Residue Number System

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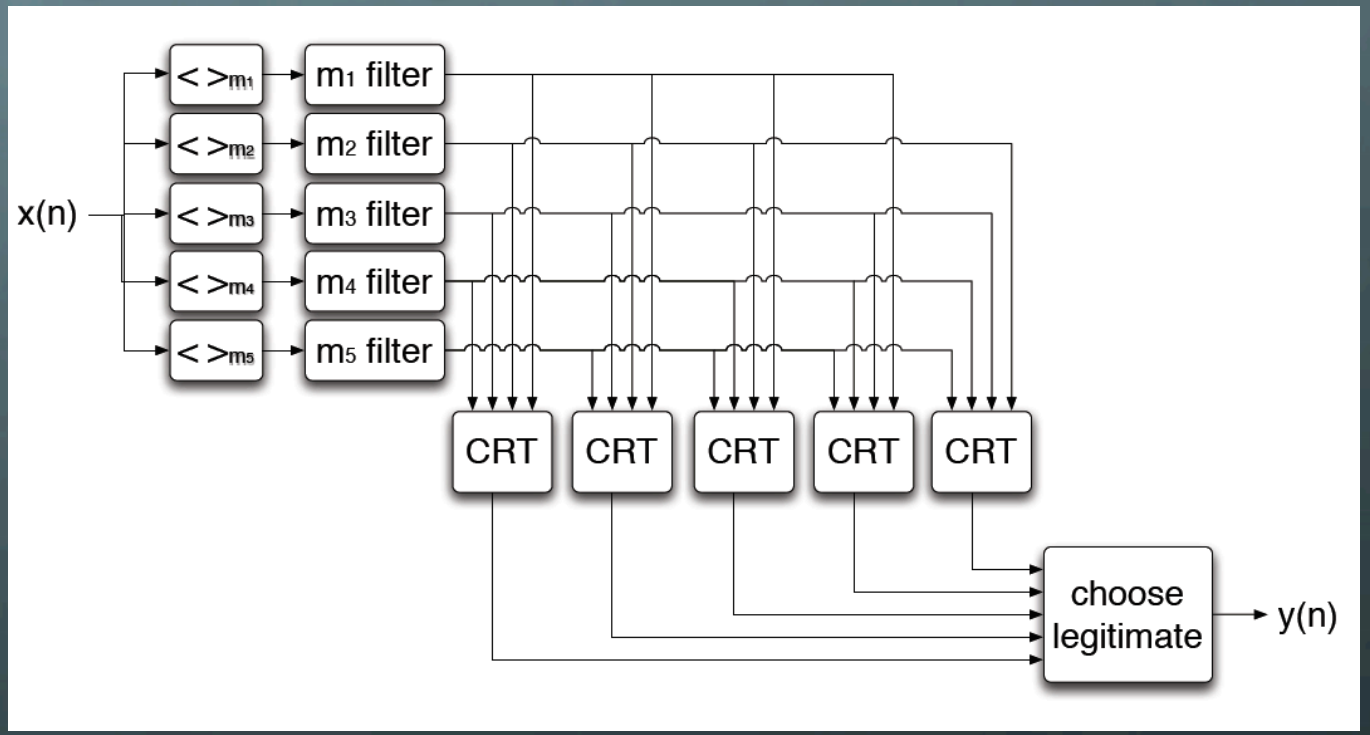
- N moduli (m_1 … m_N)
- $X_i = X \bmod m_i$ range $M = m_1 \times m_2 \times \ldots \times m_N$
- Legitimate range $M' < M$



A Novel Error Detection And Correction Technique for RNS based FIR Filters, IEEE Int. Symp. DFT 2008

Alternative Techniques

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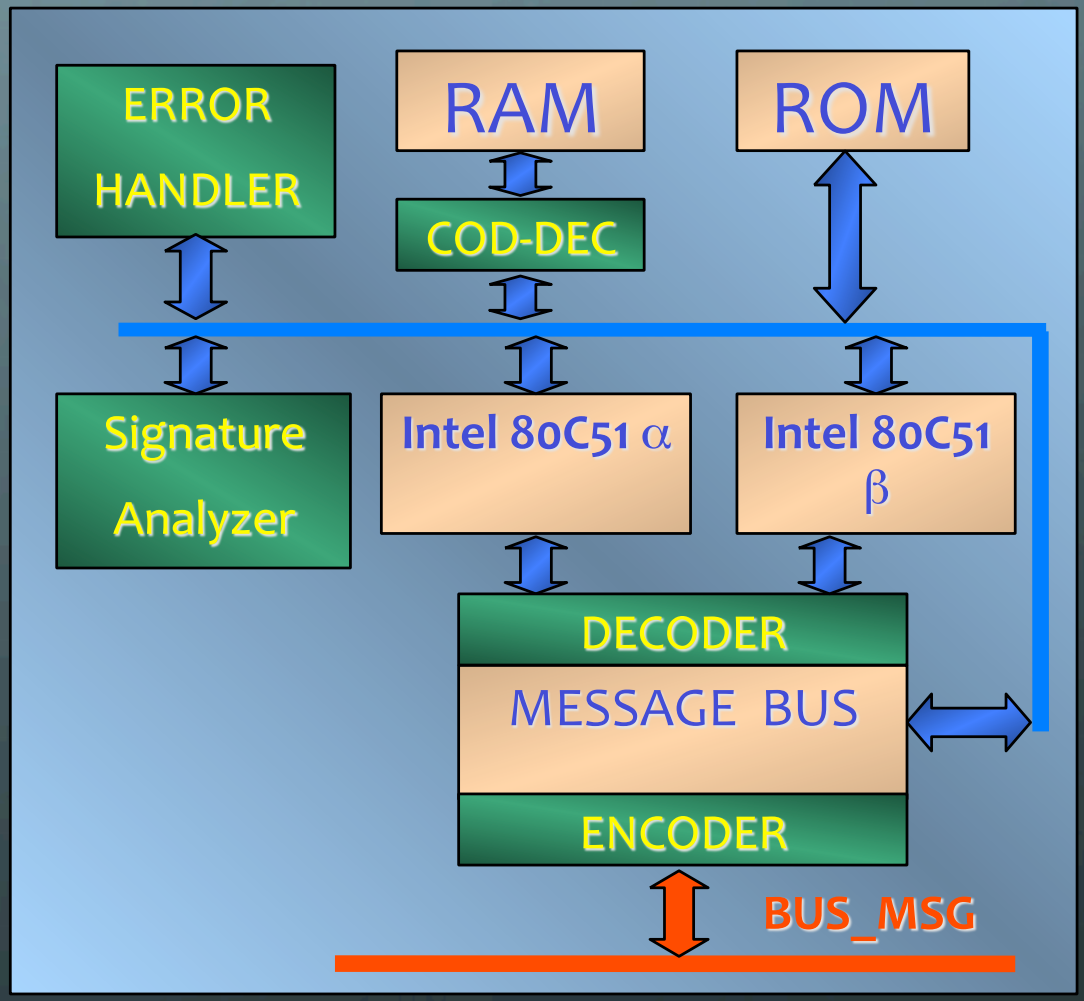
- **Fault-tolerant microcontroller**

- two μC
- Signature Analysis
- Data encoding
- Error handler



Signature analysis

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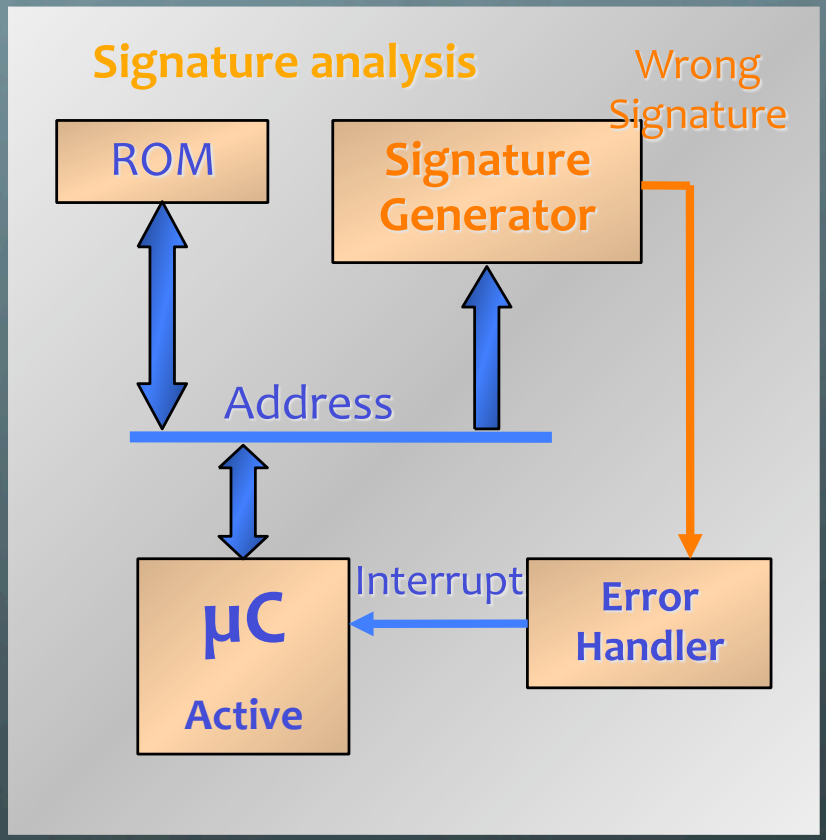

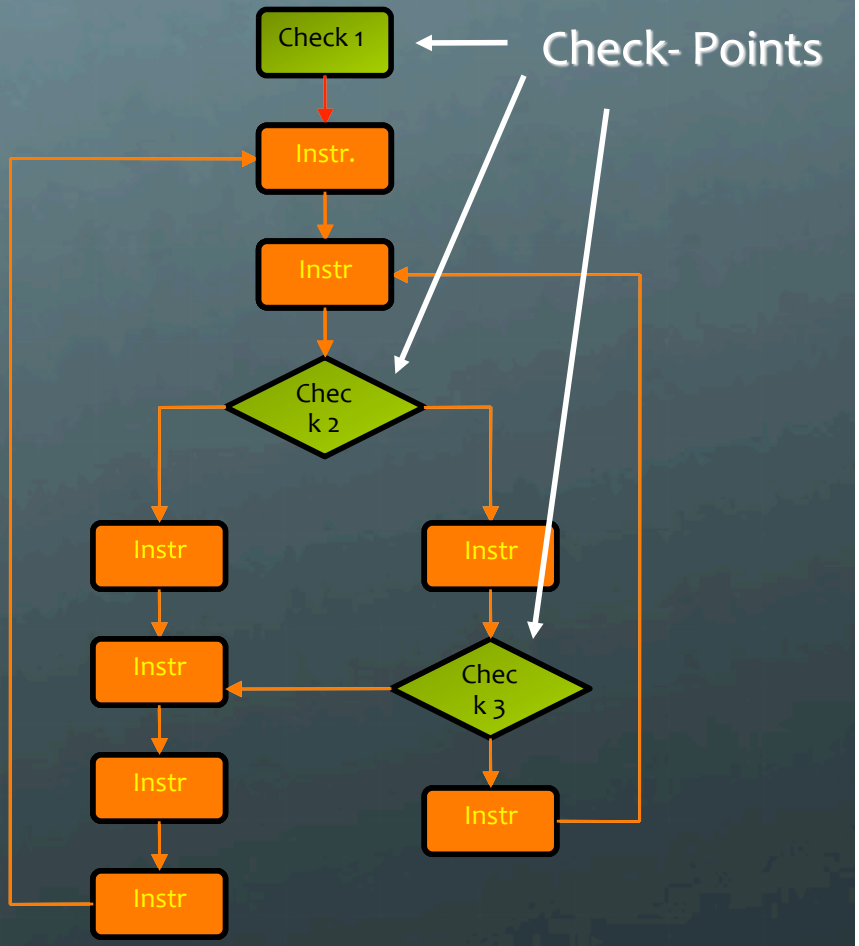

Structure Solid State Mass Memory

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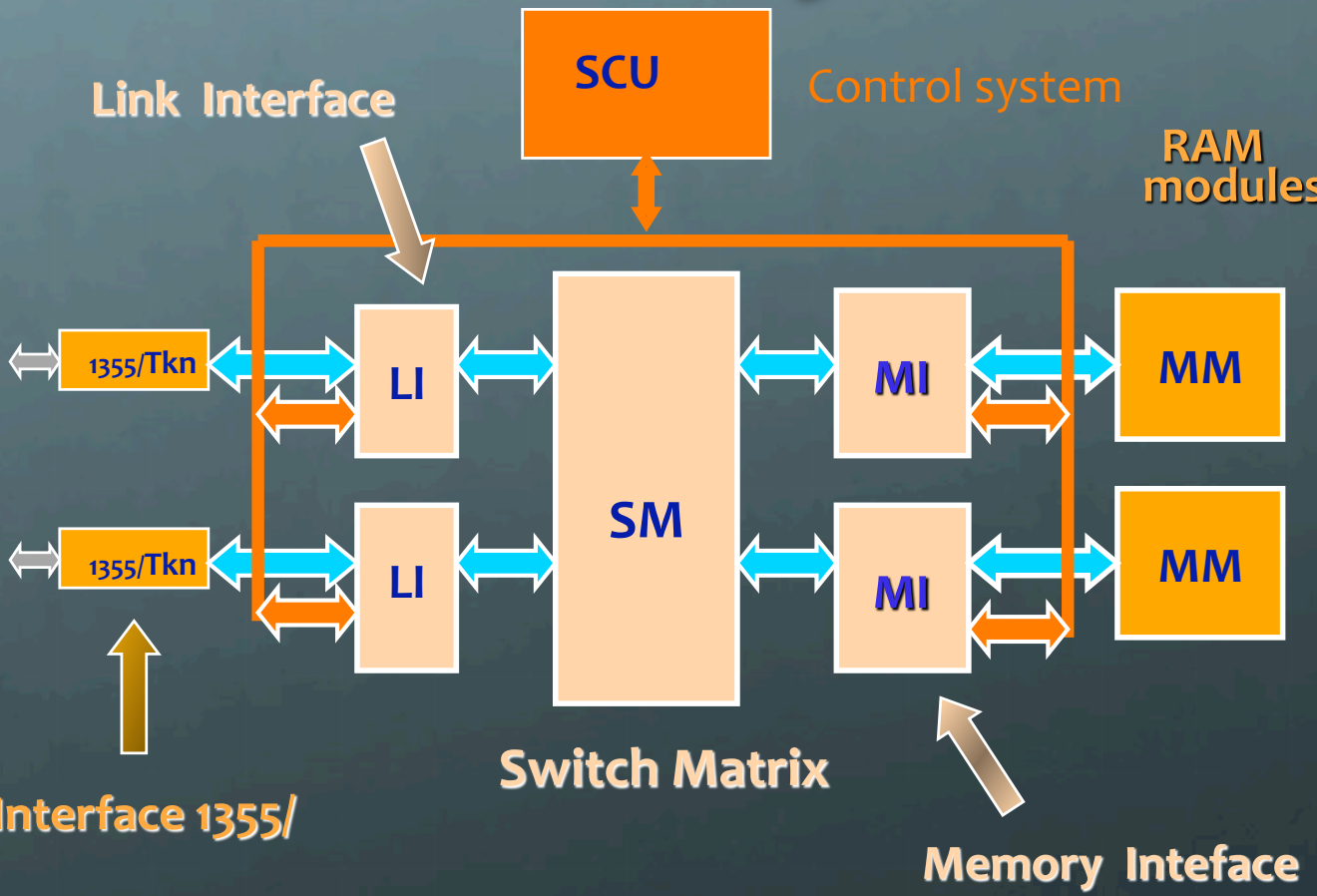
- Scalable Arch.
- Interf. 1355 DS-DE (Spacewire)
- Concurrent Accesso on memory modules
- Reconfiguration for faults
- Fault Tolerance



Implementation of F.T. blocks

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- SCU: F.T. Microcontroller
- Memory: Error detection and correction codes
- Interfaces based on FPGA: coding, TMR and configuration memory wash

Hardware implementation

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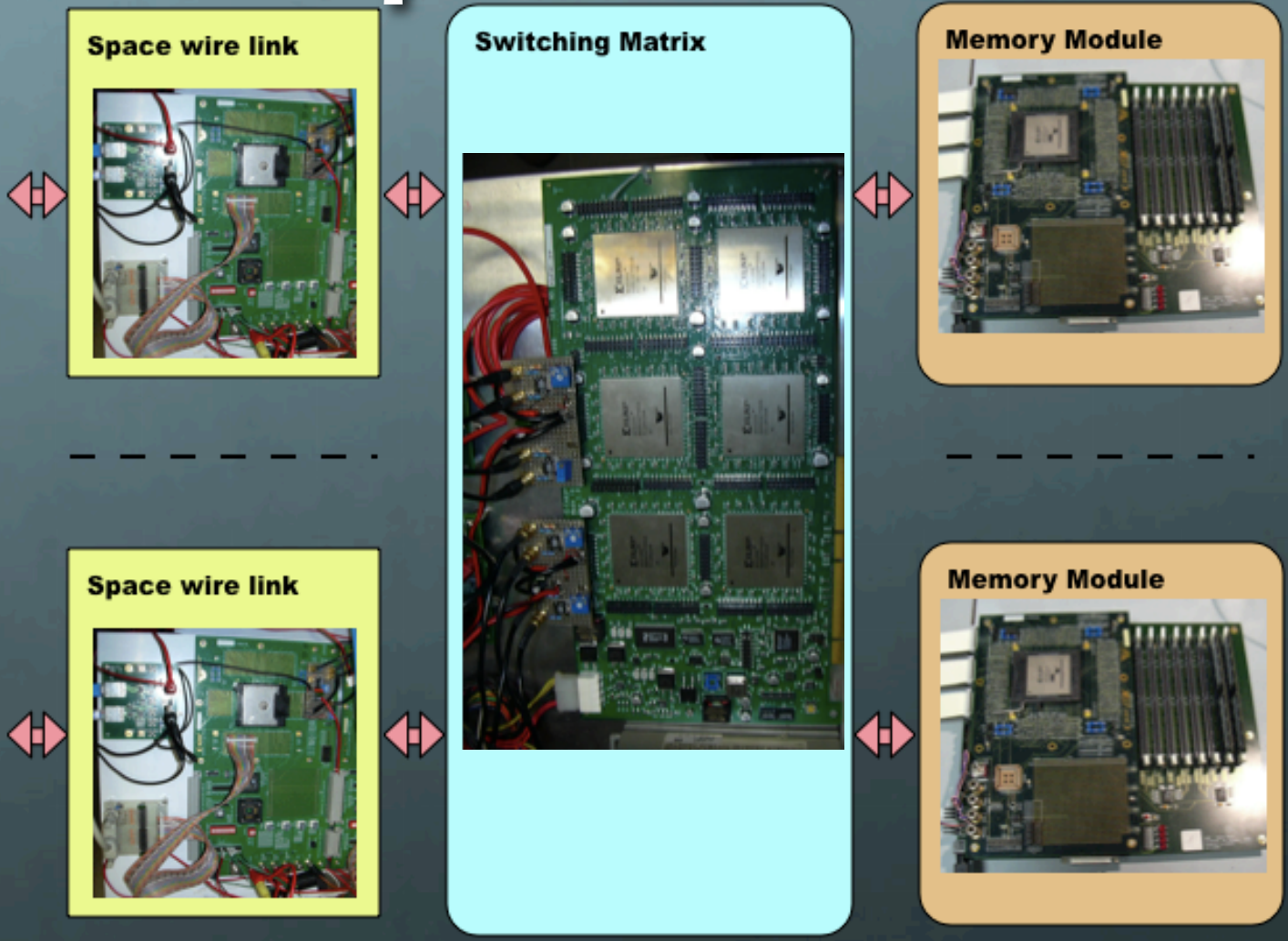

Conclusions

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- F.T. is very important in space systems based on COTS
- New technologies require new techniques
- Methodologies are strictly related to implemented functions
- Efficient solutions require mixing of techniques