Use of reconfigurable devices in space
Problems and possible solutions

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Goal

- To present the problems related to the use of re-programmable FPGAs in the space radioactive environment and to outline available solutions

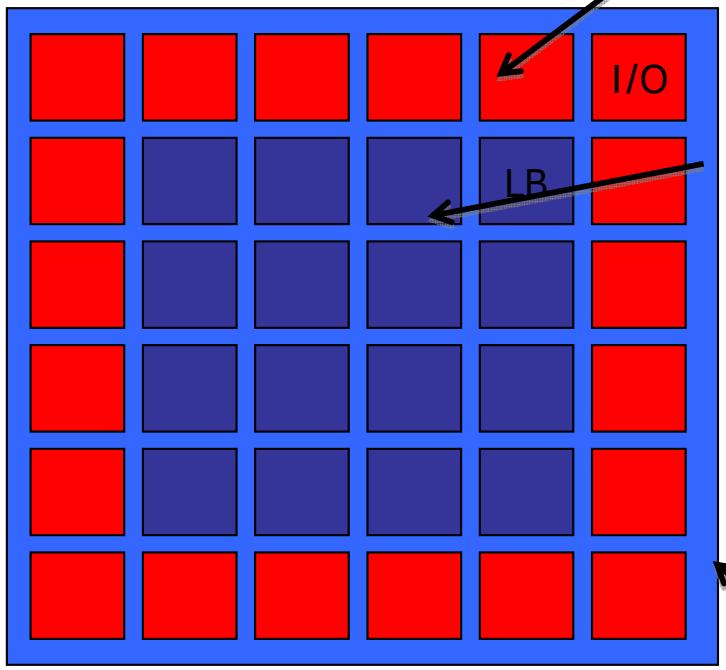
Outline

- Introduction
- The problem
- Mitigation techniques
- Conclusions

Introduction

- There is a growing interest for using re-programmable FPGA devices in space applications
  - Low-cost for low production volumes w.r.t. ASICs
  - Very short time-to-market
  - Higher versatility (to fix bugs, to extend functionalities)
  - Adaptability (reconfigurable computing)

FPGA Overview



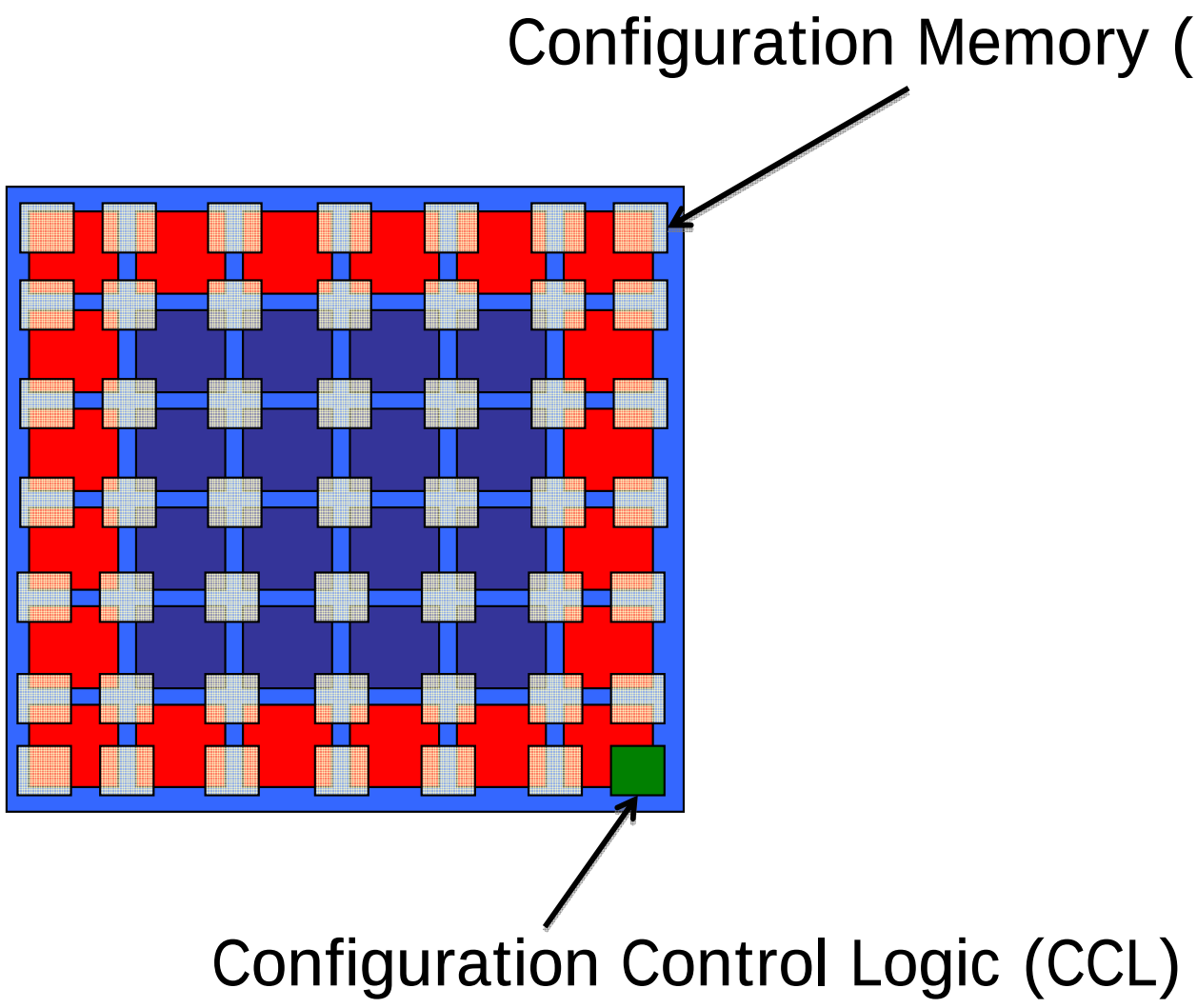
Input/Output (I/O)

Logic Block (LB):

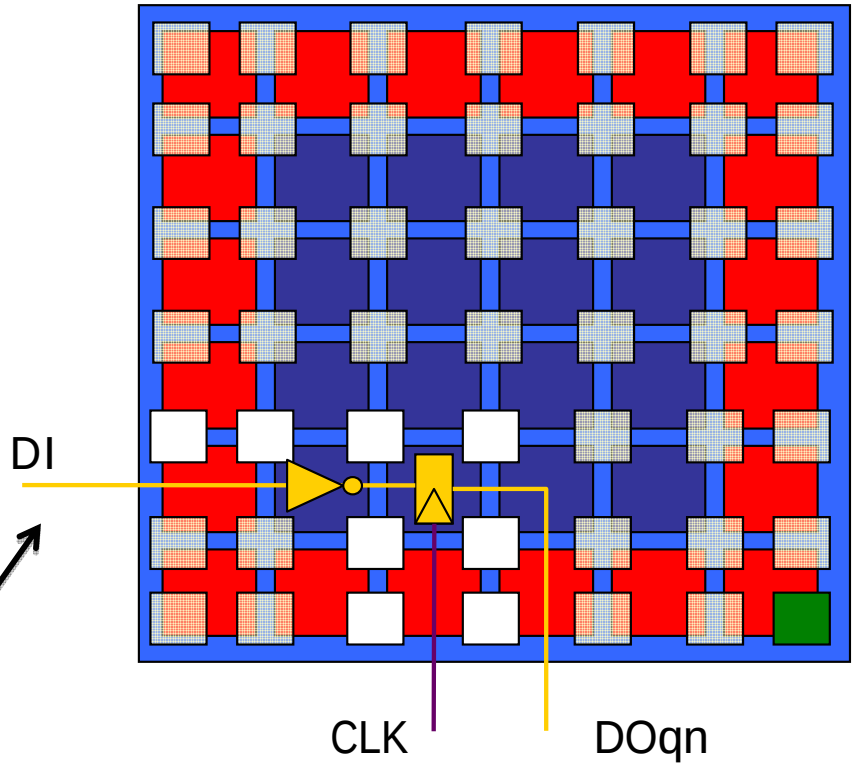
- LUT
- FF

Interconnection mesh (IM)

FPGA Overview



FPGA Overview



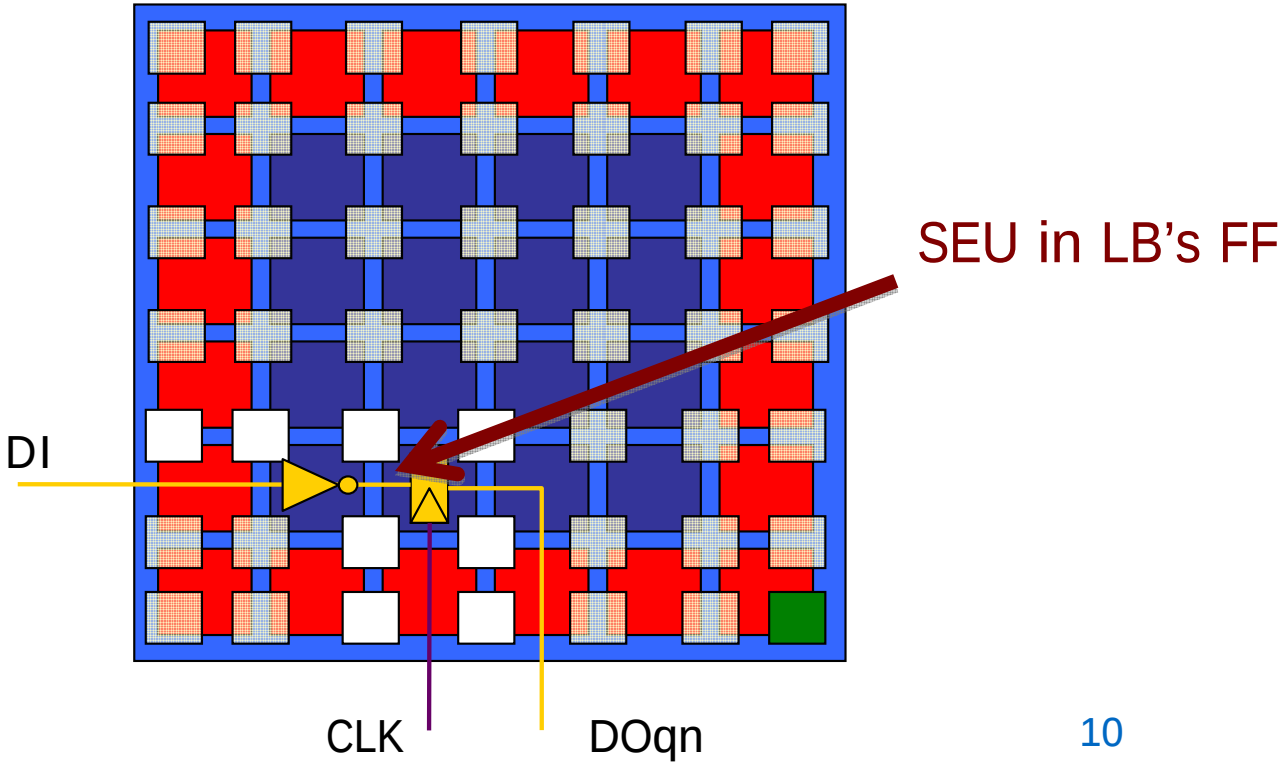
Values in the CM define how I/O, LB and IM are configured to implement a user circuit

Ionizing radiation vs FPGAs

- Ionizing radiation may result in:
  - Single Event Effect (SEE):
    - Transient, possibly persistent
    - Non destructive
  - Total Ionizing Dose Effect (TID):
    - Permanent
    - Non destructive
  - Single Event Latchup (SEL):
    - Permanent
    - Destructive

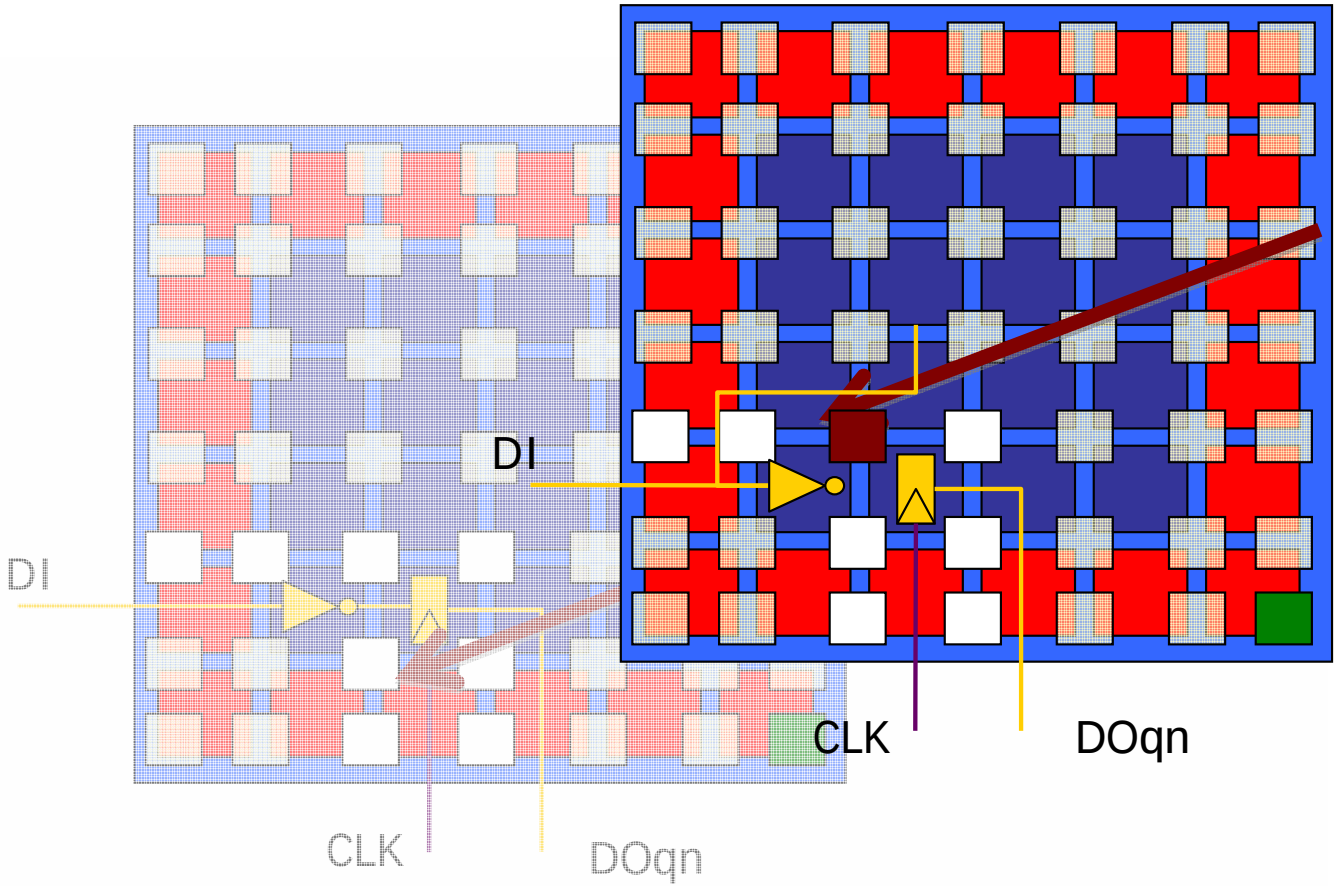
Ionizing radiation vs FPGAs

- SEE in FF



Ionizing radiation vs FPGAs

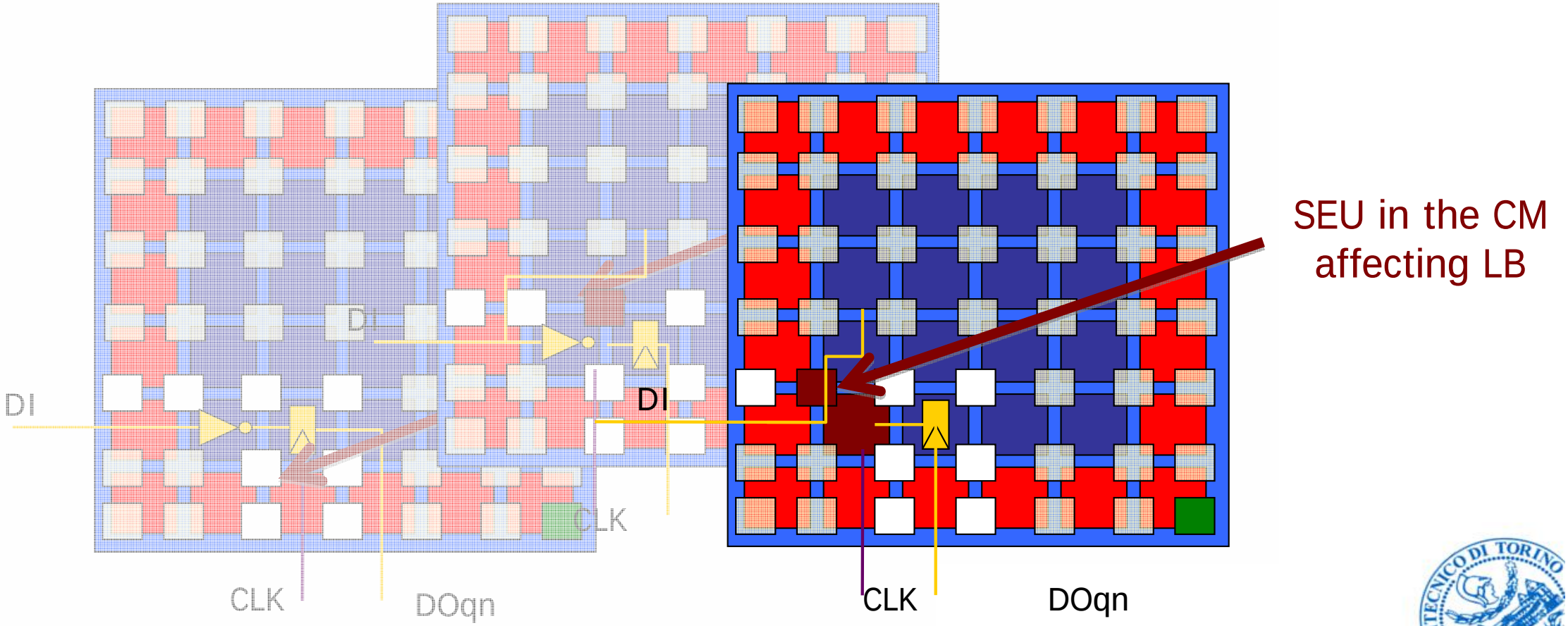
- SEE in CM



SEU in the CM affecting the routing

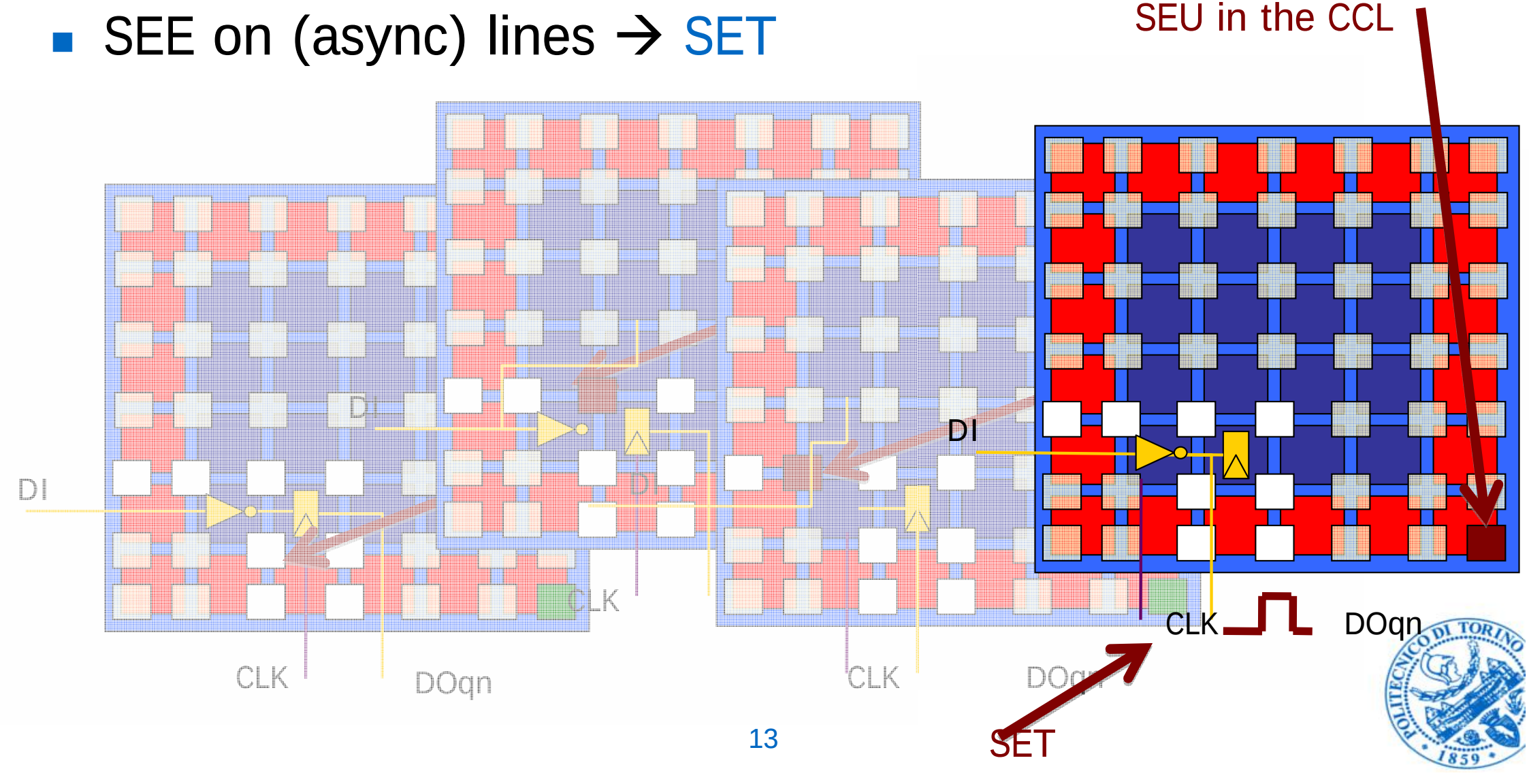
Ionizing radiation vs FPGAs

- SEE in CM



Ionizing radiation vs FPGAs

- SEE in CCL→ SEFI
- SEE on (async) lines → SET



Mitigation techniques

- Different solutions are available:
  - Single-chip HW redundancy
  - Multi-chip HW redundancy
  - Custom silicon design
  - Custom process design
- Selecting the mitigation technique is a difficult task as it has to consider:
  - The device cross section
  - The space environment the device aims at
  - The application the device is used in

Case study

- Commercial of the shelf:
  - Virtex 4 XC4VFX140
    - CM (SRAM) and process are standard
  - RT ProASIC3 RT3PE3000L
    - CM (Flash) and process are standard
- Radiation hardened:
  - Atmel ATF280E
    - CM (SRAM) is designed to be insensitive to SEE up to a certain LET
    - Silicon process is designed to be insensitive to TID/SEL up to a certain LET

Some figures

	Logic cells	I / O
Virtex 4 XC4VFX140	142,128	896
RT ProASIC3 RT3PE3000L	75,364	620
ATF280E	14,400	340

Some figures

	Logic cells	I/O
Virtex 4 XC4VFX140	142,128	896
RT ProASIC3 RT3PE3000L	75,364	620
ATF280E	14,400	340

At first sight it seems the clear winner, but raw numbers do not tell the whole story!

Some figures

	SEU in CM		SEU in FF		SET		SEL	TID	SEFI	
	LET_{Th}	σ_{Sat}/bit	LET_{Th}	σ_{Sat}/bit	LET_{Th}	σ_{Sat}/bit	LET_{Th}		LET_{Th}	σ_{Sat}
Virtex 4	< 1	$4x10^{-8}$	< 1	$4x10^{-8}$	?	?	> 90	300	< 1	$6x10^{-5}$
RT ProASIC3	> 96	0	6	$2x10^{-7}$	4	$2x10^{-6}$	> 96	15	?	?
ATF280E	> 30	$2x10^{-8}$	?	?	?	?	> 80	300	?	?

LET is expressed in MeVcm^2/mg

σ_{Sat} is expressed in cm^2/device or cm^2/bit

TID is krad (Si)

Some figures

Mitigation is likely to be needed for SEU in CM and FF, SET, and SEFI

	SEU in CM		SEU in FF		SET		SEL	TID	SEFI	
	LET_{Th}	σ_{Sat}/bit	LET_{Th}	σ_{Sat}/bit	LET_{Th}	σ_{Sat}/bit	LET_{Th}		LET_{Th}	σ_{Sat}
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LET is expressed in MeVcm^2/mg

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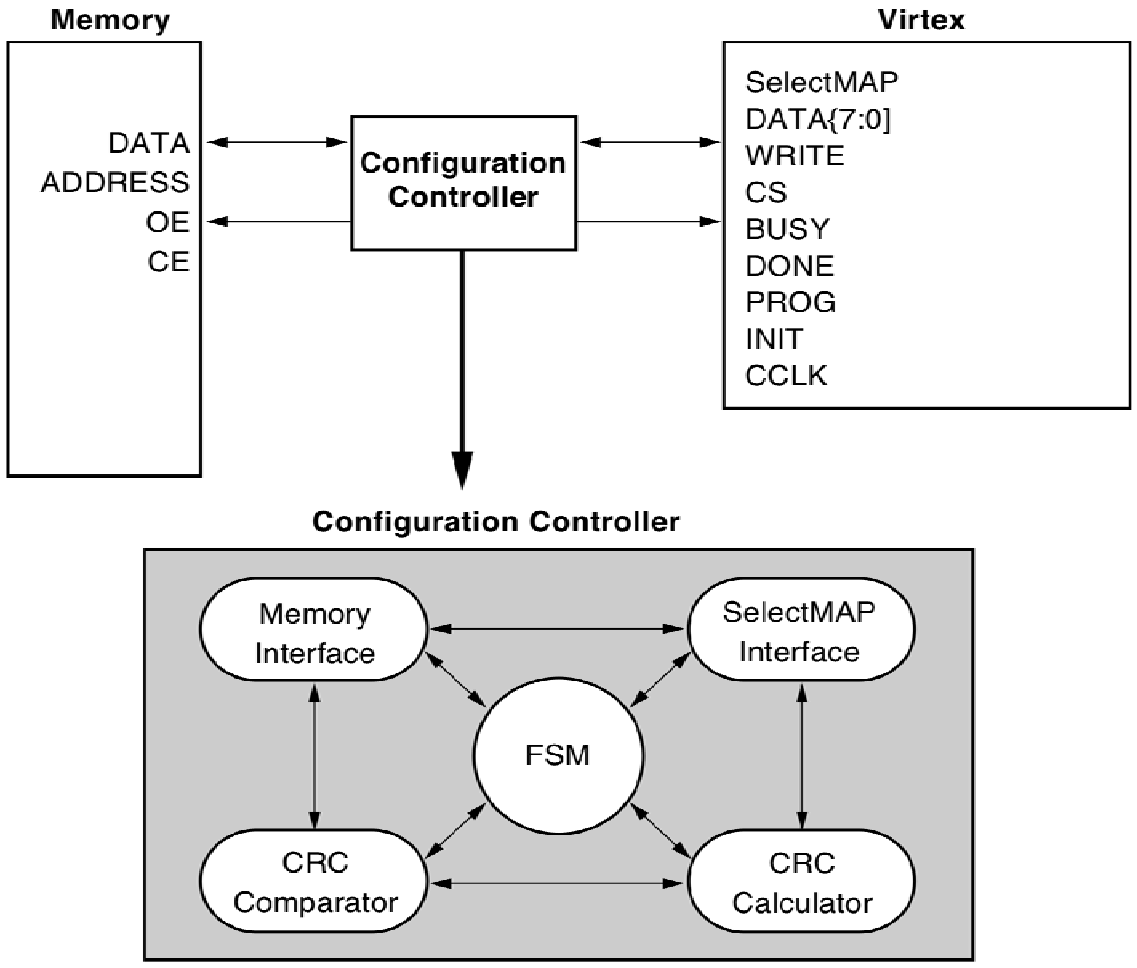
TID is krad (Si)

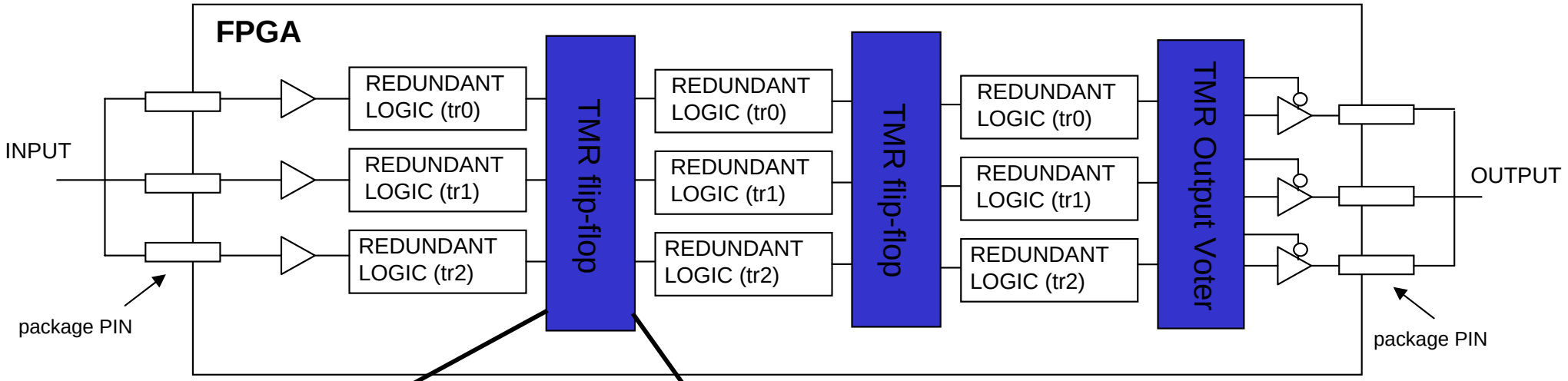
SEE mitigation techniques

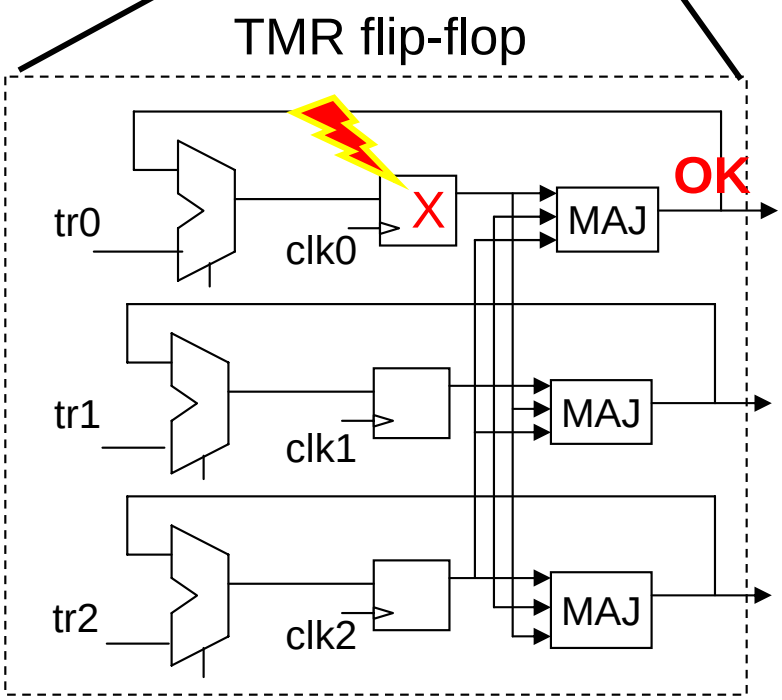
- SRAM-based CM:
  - SEE in the CM (SEU):
    - Masked using HW redundancy (TMR), and
    - Corrected using CM scrubbing
      - SEE in CM is persistent → re-programming is needed
  - SEE in the I/O and LB (SEU/SET):
    - Masked using in-chip hardware redundancy
  - SEE in CCL (SEFI):
    - Masked using chip-level hardware redundancy

CM scrubbing



TMR for SEE in CM/LB

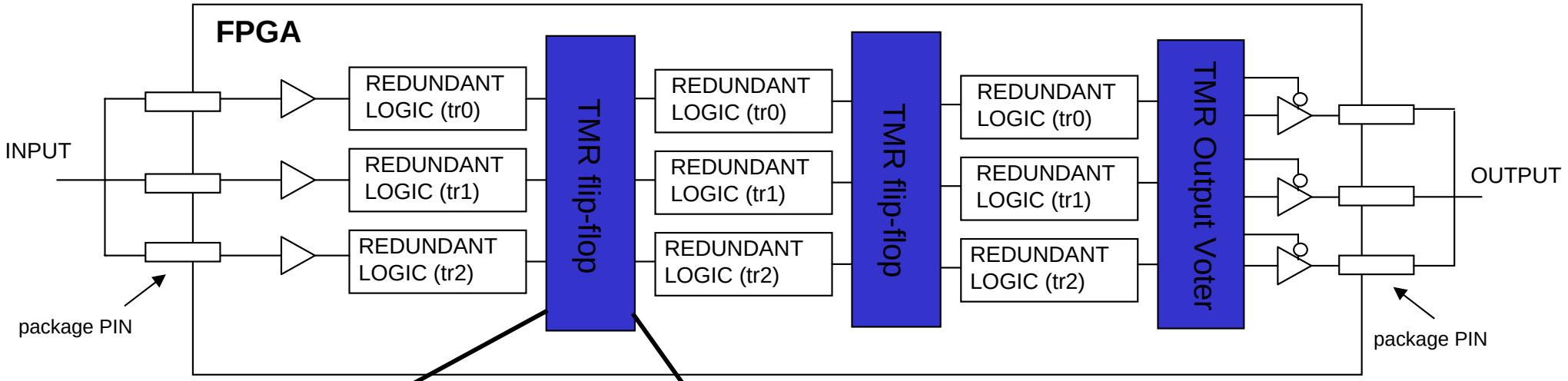


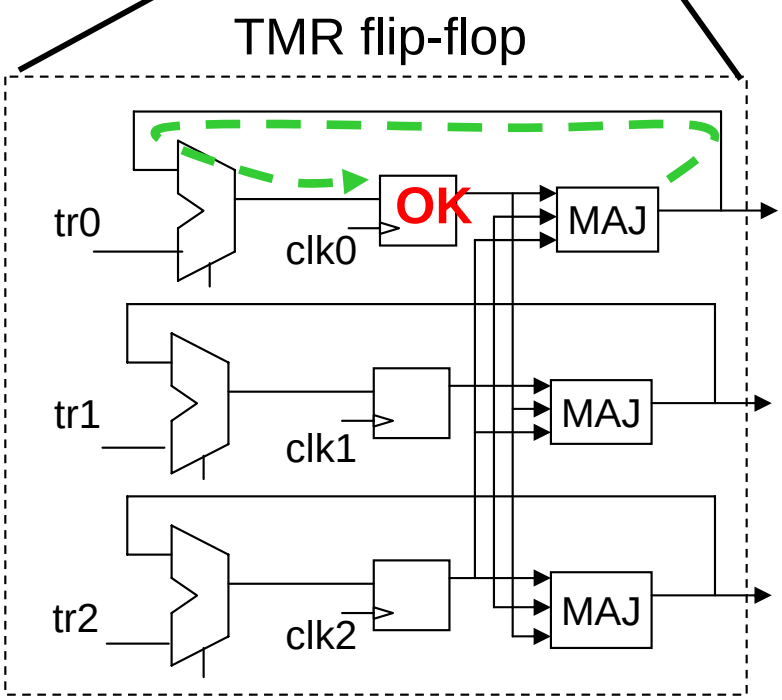


The recovery path is mandatory to correct the state of the flip-flops, specially in FSM.

R0	R1	R2	MAJ
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

TMR for SEE in CM/LB





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R0	R1	R2	MAJ
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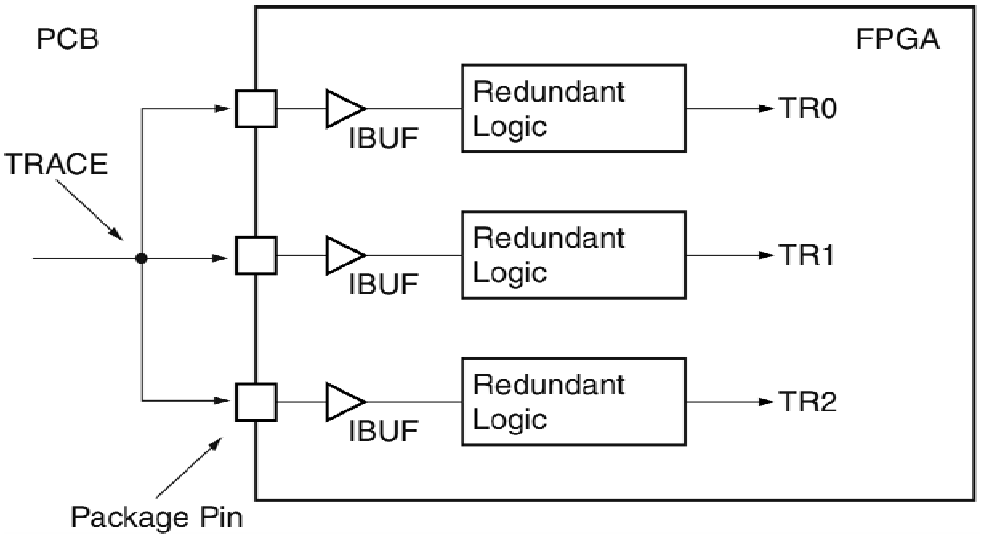
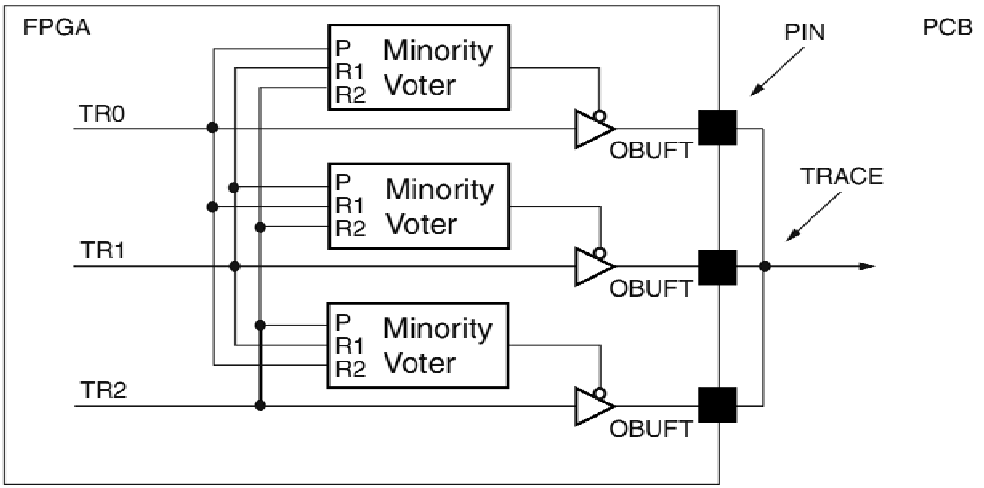
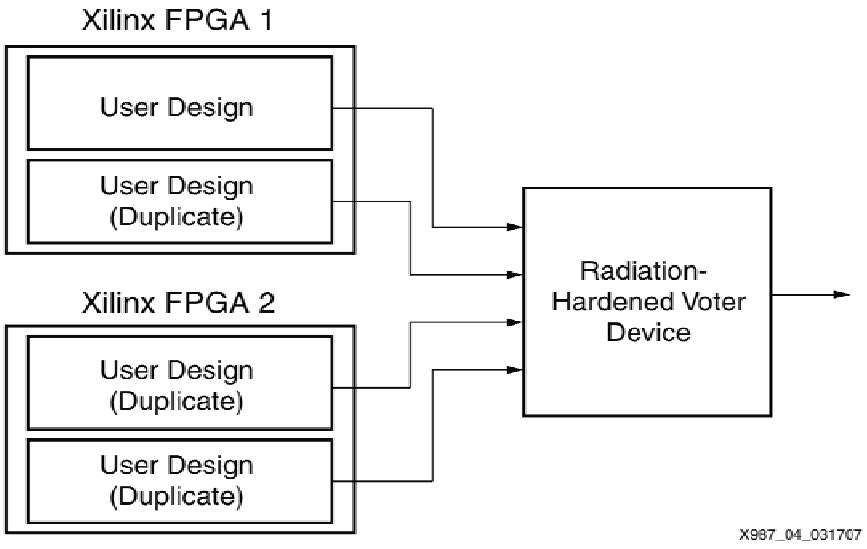
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

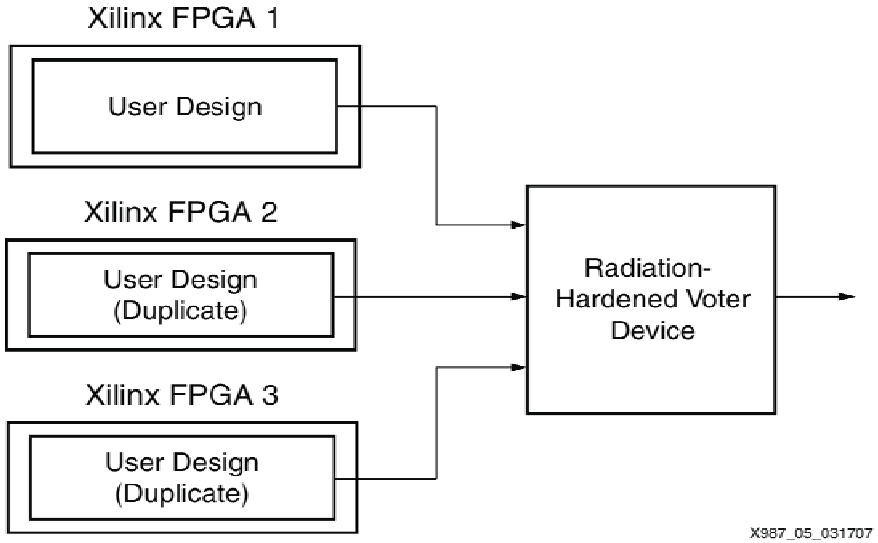
TMR SEE in CM/I/O





Redundancy for SEE in CCL





Applying SEE mitigation

- Requires design effort:
  - Manual design for scrubbing, and chip-level redundancy
  - Automated for in-chip redundancy:
    - X-TMR makes design mitigation
    - Care must be taken to place & route the design to preserve robust architecture
      - Problems with SEE in CM that provoke multiple errors in FPGA resources
- Correct cocktail of mitigation techniques should be selected considering the application, and the environment

Some figures

Mitigation is likely to be needed for SEU in FF, SET, and SEFI

	SEU in CM		SEU in FF		SET		SEL	TID	SEFI	
	LET_{Th}	σ_{Sat}/bit	LET_{Th}	σ_{Sat}/bit	LET_{Th}	σ_{Sat}/bit	LET_{Th}		LET_{Th}	σ_{Sat}
Virtex 4	< 1	$4x10^{-8}$	< 1	$4x10^{-8}$	?	?	> 90	300	< 1	$6x10^{-5}$
RT ProASIC3	> 96	0	6	$2x10^{-7}$	4	$2x10^{-6}$	> 96	15	?	?
ATF280E	> 30	$2x10^{-8}$	?	?	?	?	> 80	300	?	?

LET is expressed in MeVcm^2/mg

σ_{Sat} is expressed in cm^2/device or cm^2/bit

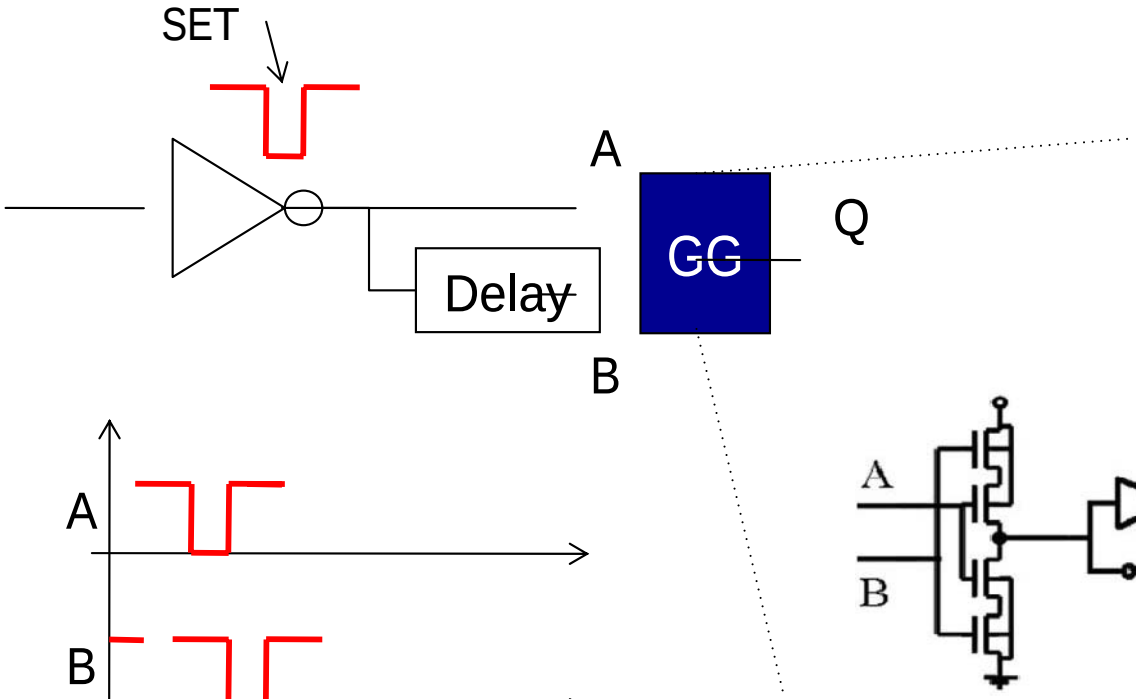
TID is krad (Si)

SEE mitigation techniques

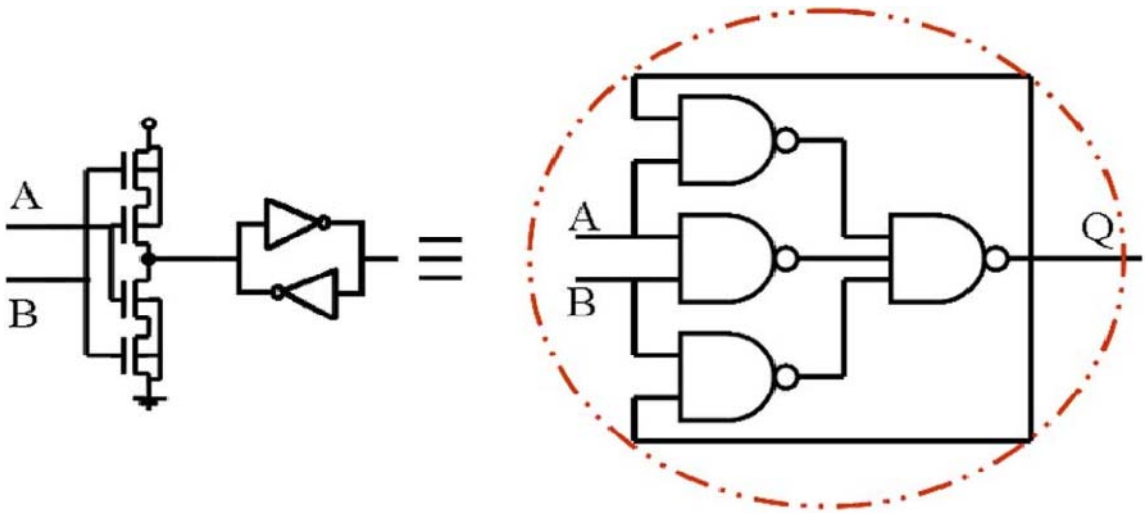
- Flash-based CM:
  - SEE in CM are not an issue
  - SEE in the I/O and LB (SEU/SET):
    - Masked using in-chip hardware redundancy
  - SEE in CCL (SEFI):
    - Likely to be masked using chip-level hardware redundancy

SEE in LB

- SEE in LB of Flash-based device can produce SET → time redundancy is used

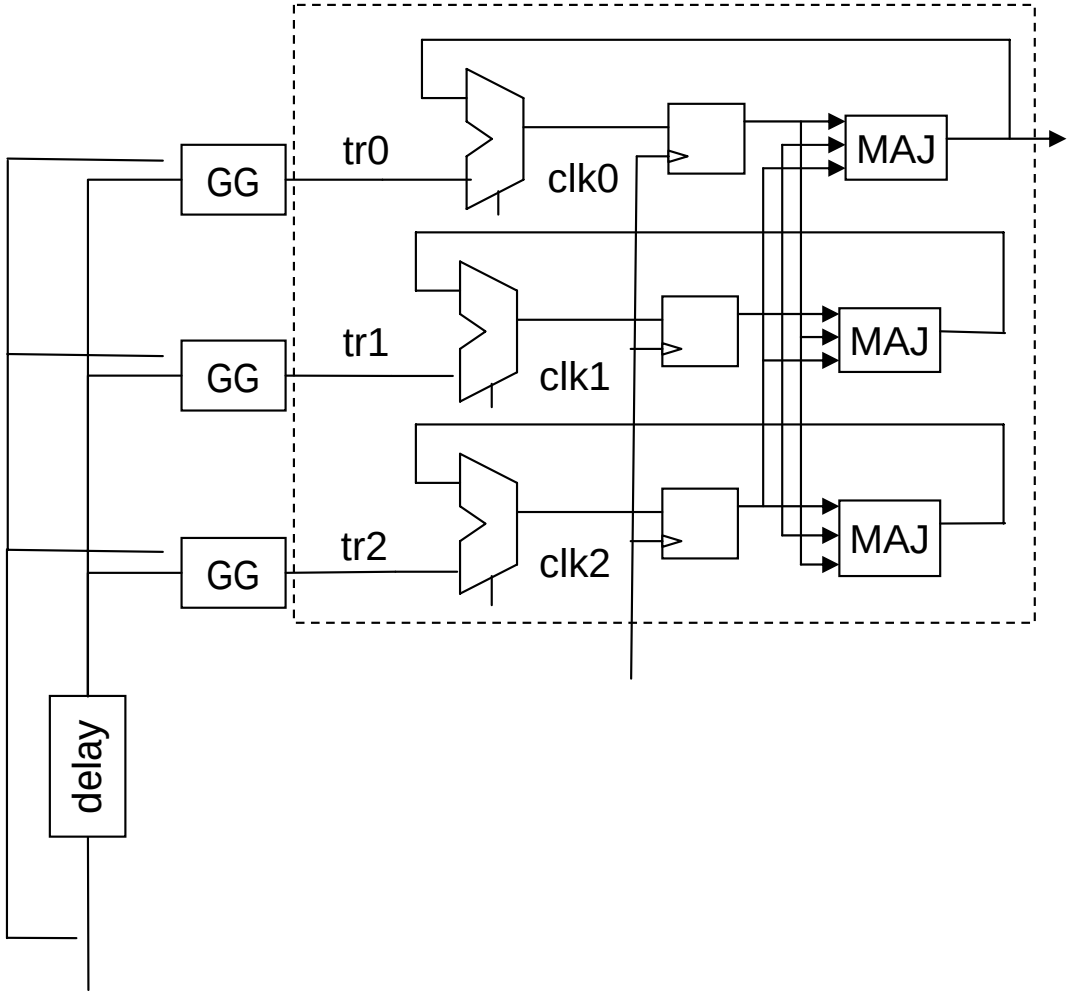


GG=Guardian Gate

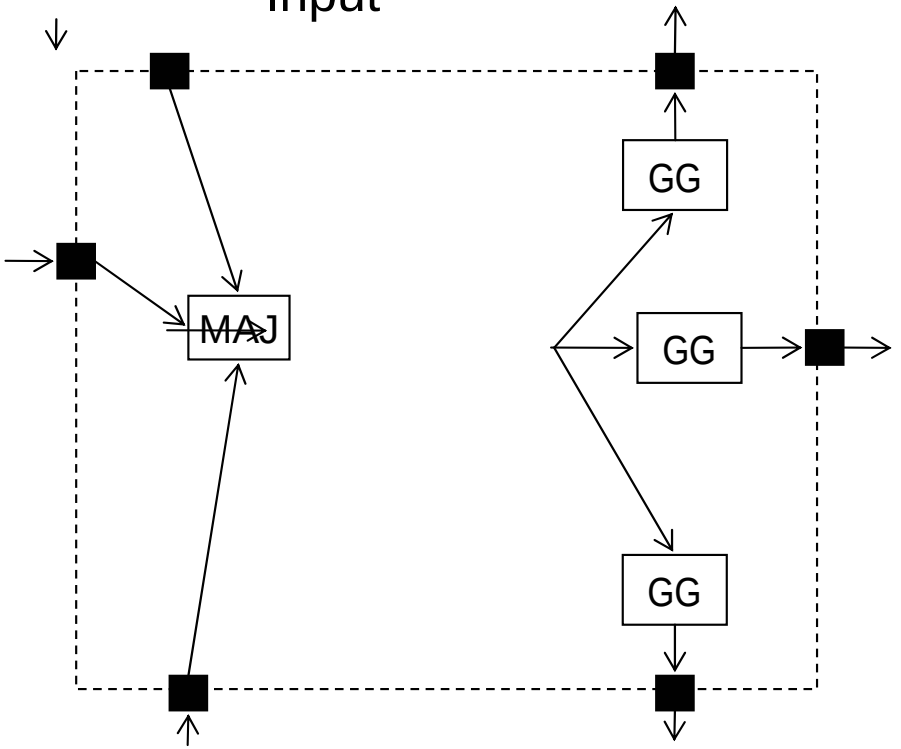


TMR for SEE in FF and I/O

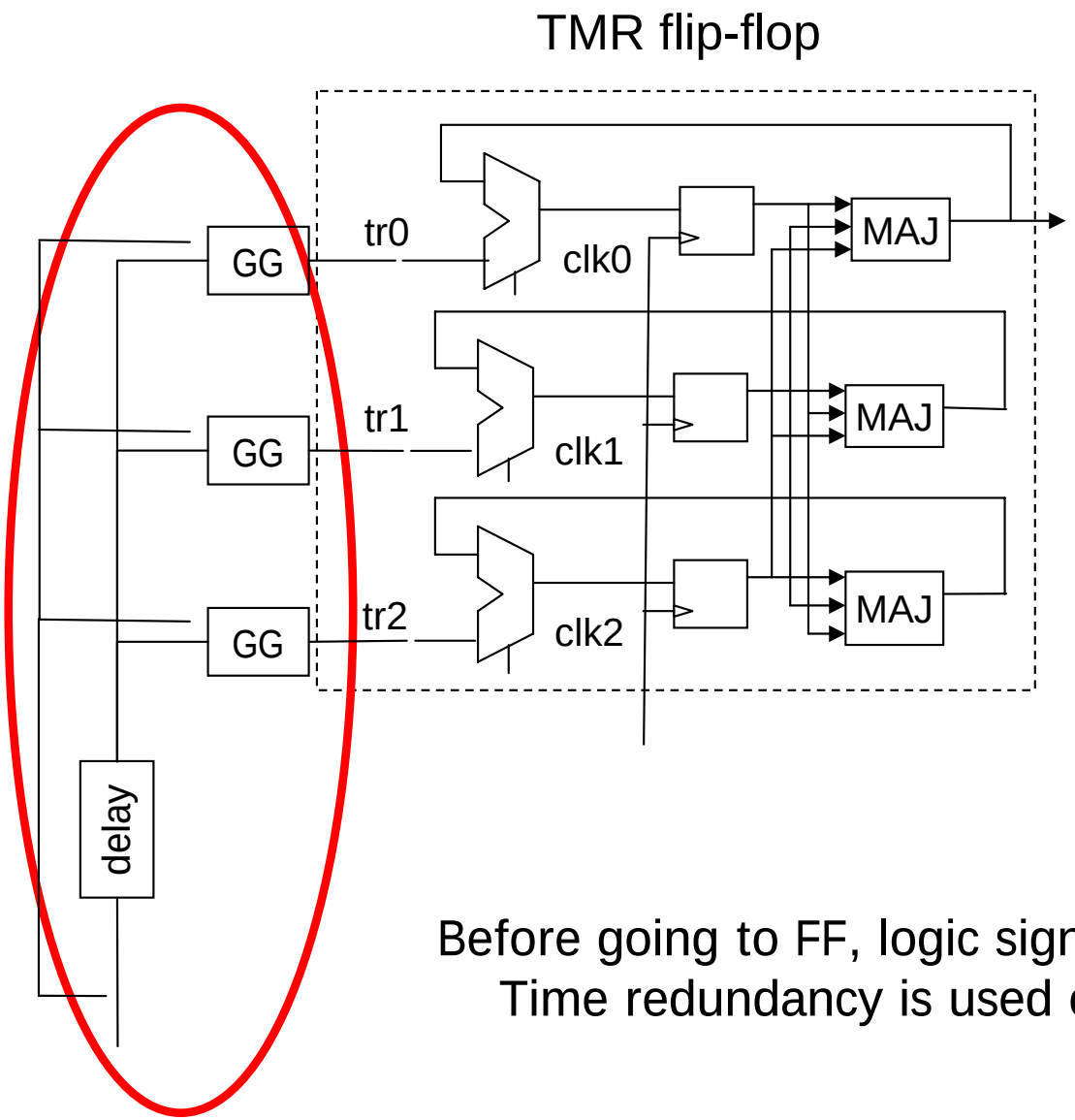
TMR flip-flop

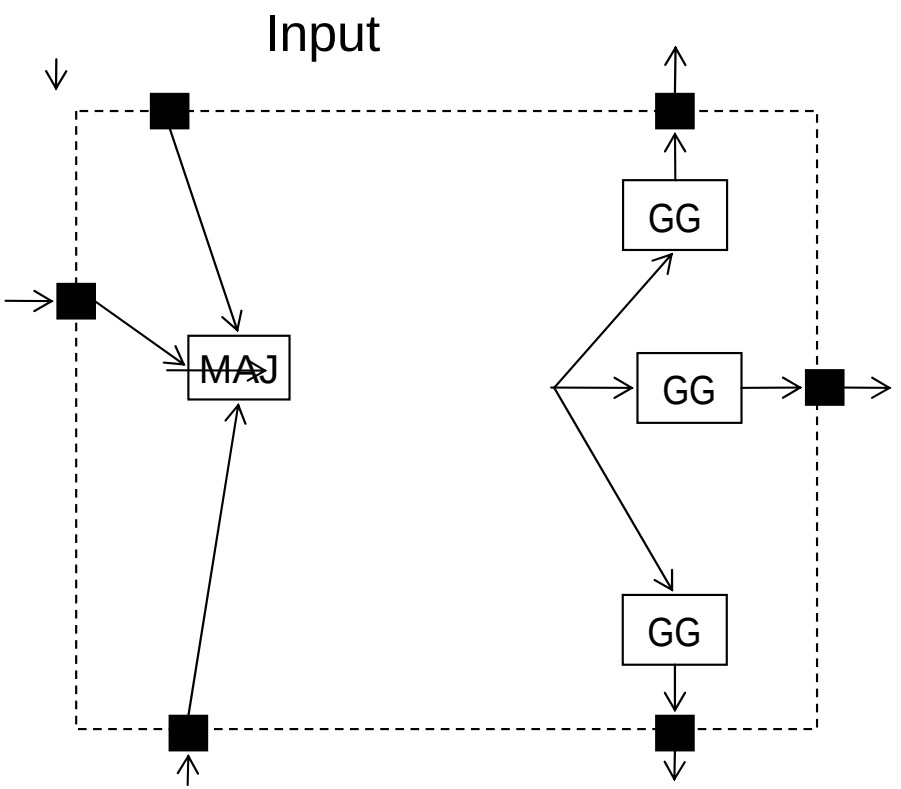


Input



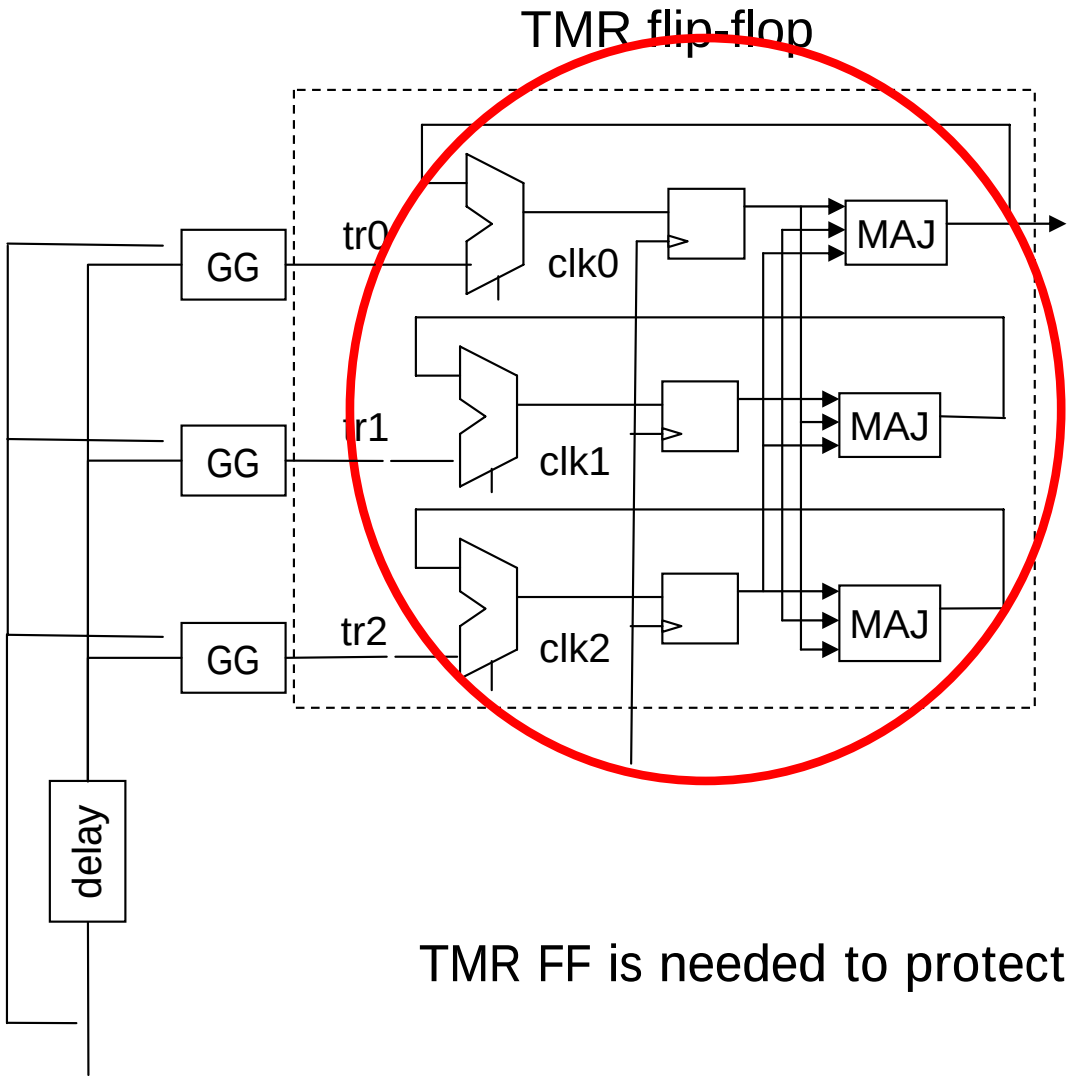
TMR for SEE in FF and I/O

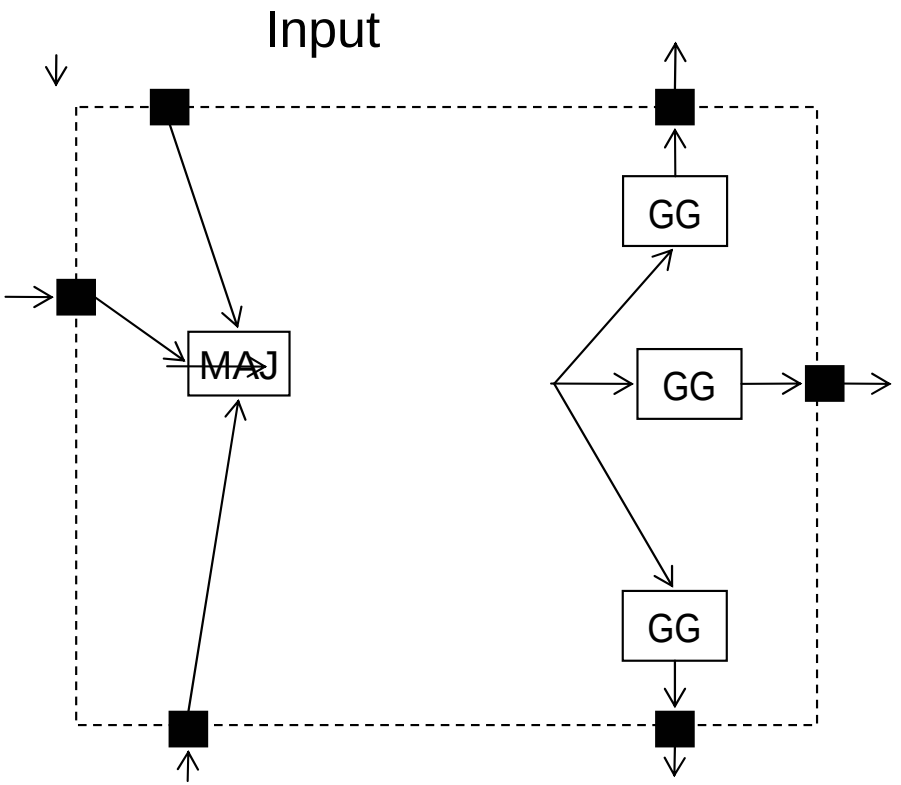




Before going to FF, logic signals are triplicated.
Time redundancy is used on each replica.

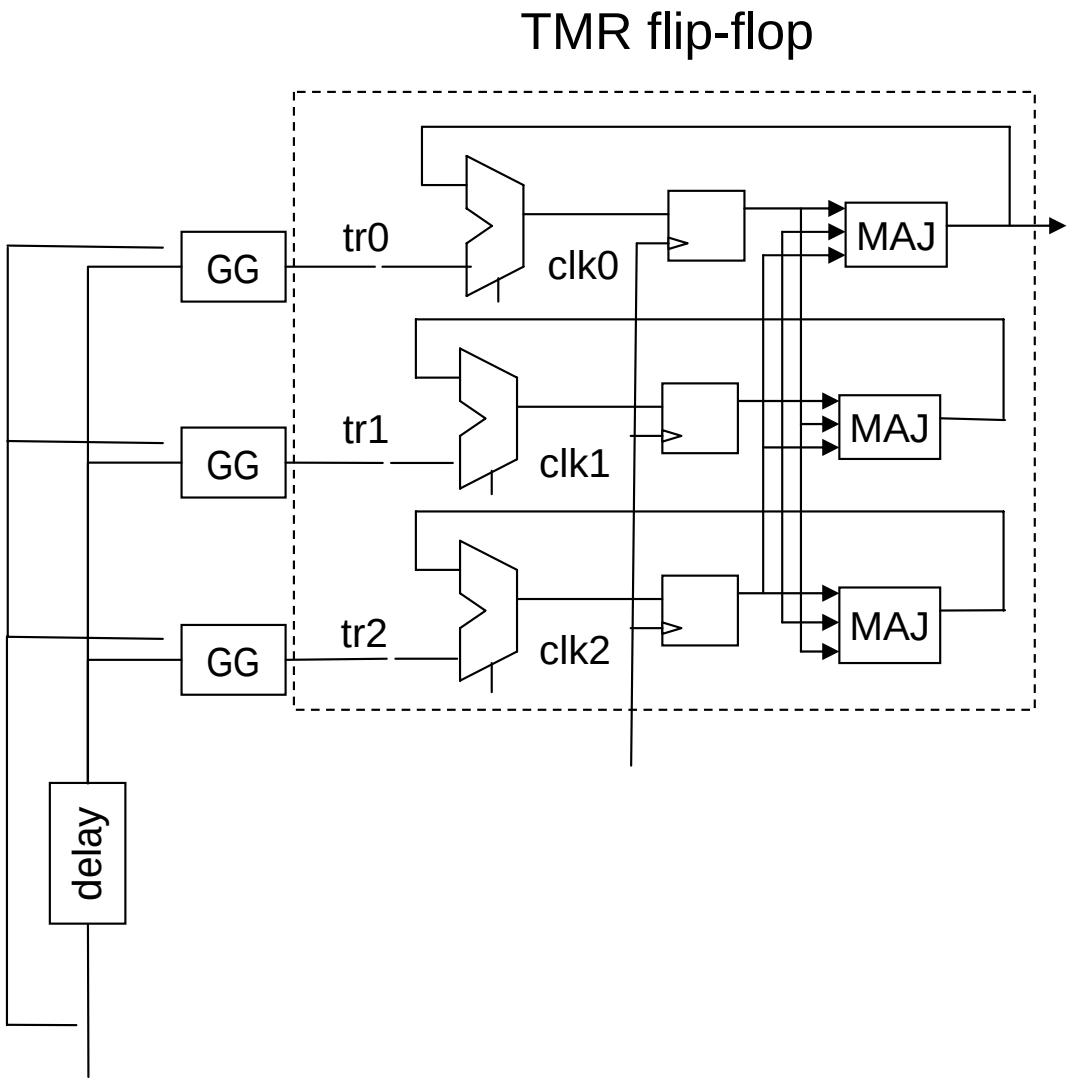
TMR for SEE in FF and I/O

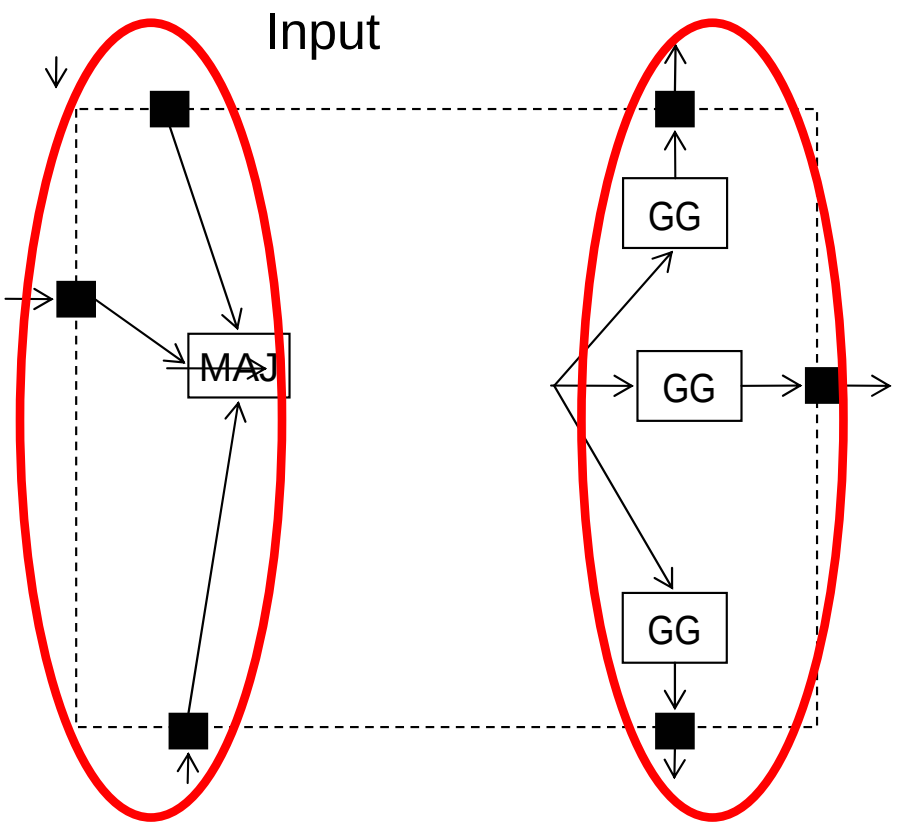




TMR FF is needed to protect against SEE in FF.

TMR for SEE in FF and I/O





I/O must be triplicated and three different I/O banks used.

Some figures

Minor mitigation is likely to be needed:
- CM scrubbing
- Device already includes CM checker

	SEU in CM		SEU in FF		SET		SEL	TID	SEFI	
	LET_{Th}	σ_{Sat}/bit	LET_{Th}	σ_{Sat}/bit	LET_{Th}	σ_{Sat}/bit	LET_{Th}		LET_{Th}	σ_{Sat}
Virtex 4	< 1	$4x10^{-8}$	< 1	$4x10^{-8}$	?	?	> 90	300	< 1	$6x10^{-5}$
RT ProASIC3	> 96	0	6	$2x10^{-7}$	4	$2x10^{-6}$	> 96	15	?	?
ATF280E	> 30	$2x10^{-8}$	?	?	?	?	> 80	300	?	?

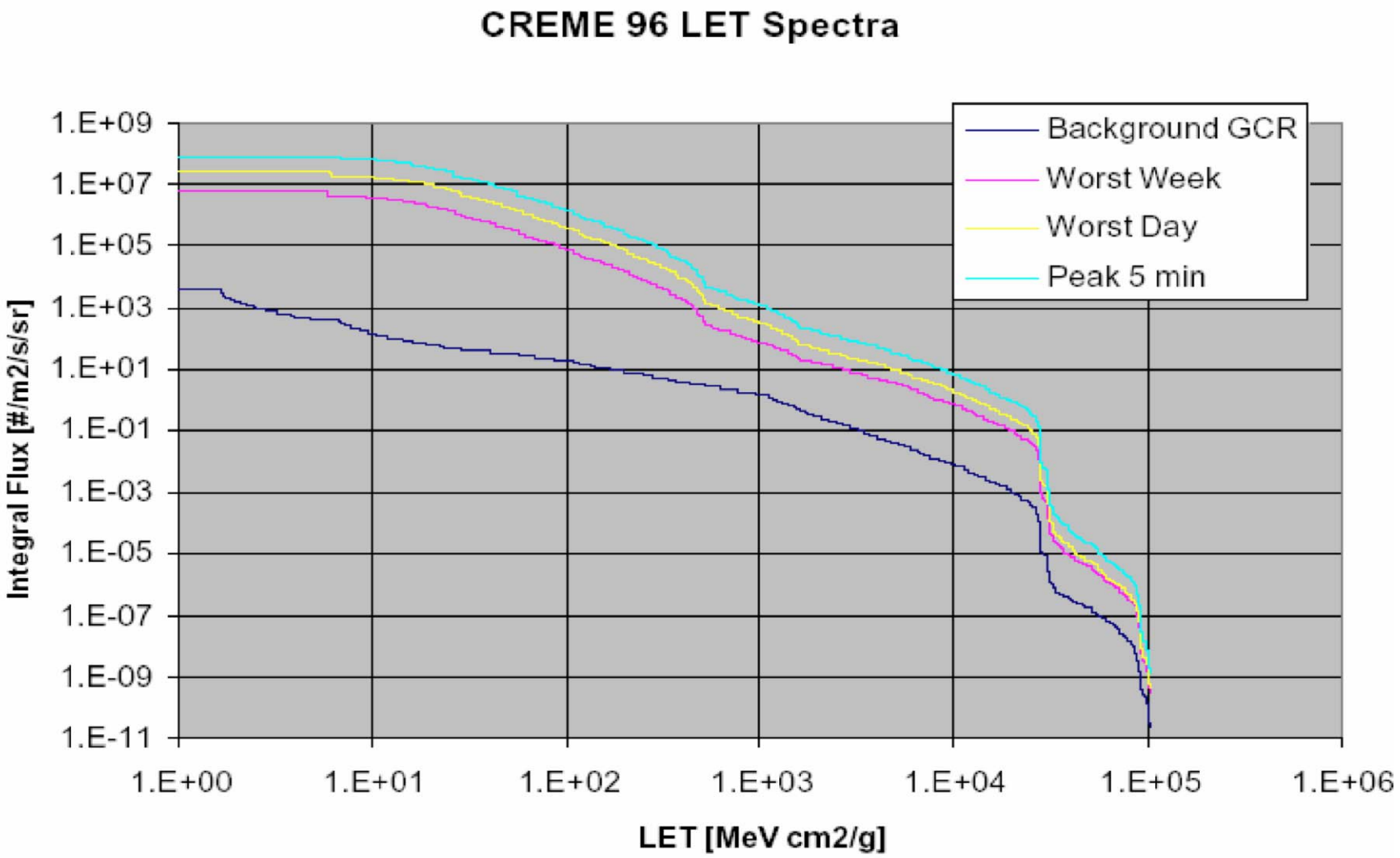
LET is expressed in MeVcm^2/mg

σ_{Sat} is expressed in cm^2/device or cm^2/bit

TID is krad (Si)

An application scenario

- GEO orbit (like GAIA, Herschel, Plank,...)



An application scenario

- SEE in CM

	LET_{Th}	σ_{Sat} [cm^2/bit]	LET	Background GCR flux [#/cm^2s]	Background GCR SEE rate [#/bit s]
Virtex 4	< 1	$4x10^{-8}$	0.76	$2.6x10^{-3}$	$1.04x10^{-10}$
RT ProASIC3	> 96	0	94.6	$3.5x10^{-13}$	0
ATF280E	> 30	$2x10^{-8}$	38.3	$4.8x10^{-10}$	$9.6x10^{-18}$

- Example:
  - Virtex 4 XC4VFX140 has 47,856,512 CM bits → Background GCR produces $4,98x10^{-3}$ SEU/s in CM (in worst day can be 49 SEU/s)
  - RT ProASIC3 is expected to have 0 SEU
  - ATF280E has about 4M bits→ $3,8x10^{-11}$ SEU/s

An application scenario

- Virtex 4:
  - $4{,}98 \times 10^{-3}$ SEU/s in CM → 1 SEU in CM every 3 minutes
  - Scrubbing is needed and TMR may be needed depending on the application
- RT ProASIC3 and ATF280E:
  - Nothing has to be done

An application scenario

- SEE in FF/SET

	LET_{Th}	σ_{Sat} [cm^2/bit]	LET	Background GCR flux [#/cm^2s]	Background GCR SEE rate [#/bit s]
Virtex 4	< 1	$4x10^{-8}$	0.76	$2.6x10^{-3}$	$1.04x10^{-10}$
RT ProASIC3	6	$2x10^{-7}$	6.27	$2.9x10^{-5}$	$5.8x10^{-12}$
ATF280E	?	?	?	?	?

- Example:
  - Virtex 4 XC4VFX140 has 126,336 FFs → Background GCR produces $1.31x10^{-5}$ SEU/s in FFs
  - RT ProASIC3 RT3PE3000L has 75,264 Tiles →Background GCR produces $4.36x10^{-7}$ SEU/s in FFs, and it is expected to give $4.36x10^{-6}$ SET/s

An application scenario

- Virtex 4:
  - 1.31×10^{-5} SEU/s in FF → 1 SEU in FF every 22 hours
  - TMR may be needed depending on the application
- RT ProASIC3:
  - 4.36×10^{-7} SEU/s in FFs → 1 SEU in FF every 27 days
  - 4.36×10^{-6} SET/s → 1 SET every 2.7 days
  - TMR FF and GG may be needed depending on the application
- ATF280E:
  - Nothing has to be done

An application scenario

- SEFI

	LET_{Th}	σ_{Sat} [cm^2]	LET	Background GCR flux [#/cm^2s]	Background GCR SEFI rate [#/s]
Virtex 4	< 1	$6x10^{-5}$	0.76	$2.6x10^{-3}$	$1.56x10^{-7}$
RT ProASIC3	?	?	?	?	?
ATF280E	?	?	?	?	?

1 SEFI every 74 days
Action to be taken depends on the application

Revising the resource figures

	No mitigation		TMR		Notes
	Logic cells	I/O	Logic cells	I/O	
Virtex 4 XC4VFX140	142,128	896	40,608	298	3.5x on logic cells, 3x on I/O
RT ProASIC3 RT3PE3000L	75,364	620	37,682	206	2x on logic cells, 3x on I/O
ATF280E	14,400	340	14,400	340	No overhead

Revising the resource figures

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Very similar figures.

Revising the resource figures

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ATF280E	14,400	340	14,400	340	No overhead

Very small device compared to the others, but good for I/O.

Conclusions

- Re-programmable devices are available for space use, but
- Their use is not trivial:
  - Mitigation is needed
  - A lot of design efforts are needed
  - A lot of validation efforts are needed
- There is not turn-key solution...

Conclusions

- Re-programmable devices are available for space use, but
- Their use is not trivial:
  - Mitigation is needed
  - A lot of design efforts are needed
  - A lot of validation efforts are needed
- There is not turn-key solution...and plenty of work for researchers